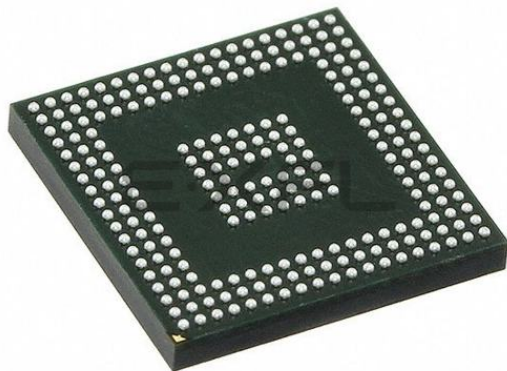




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	12800
Total RAM Bits	737280
Number of I/O	106
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	238-LFBGA, CSPBGA
Supplier Device Package	238-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a12t-2cpg236c

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

- A total of 200 mA per bank should not be exceeded.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 9](#).

Table 14: Networking Applications Interface Performances

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽¹⁾⁽²⁾

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Output Serializer/Deserializer Switching Characteristics

Table 21: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.44/−0.25	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.69/−0.13	0.73/−0.13	0.88/−0.13	0.60/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.31/−0.13	0.34/−0.13	0.39/−0.13	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/−0.15	ns
T _{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.83	0.92	1.11	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 22: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	3.22	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.00 ⁽¹⁾	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00 ⁽¹⁾	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	59.28	59.28	59.28	52.00	ns
IDELAY						
T _{IDELAYRESOLUTION}	IDELAY chain delay resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY	680.00	680.00	600.00	520.00	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.12/0.11	0.16/0.13	0.21/0.16	0.14/0.16	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.12/0.16	0.14/0.18	0.16/0.22	0.10/0.23	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.15/0.09	0.16/0.11	0.18/0.14	0.22/0.19	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 24: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T _{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T _{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T _{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T _{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T _{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T _{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T _{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T _{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T _{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.20	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.31	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.97/0.12	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.34/–0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.62/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 25: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.98	1.09	1.32	1.54	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	2.18	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.54/0.28	0.60/0.30	0.72/0.35	0.96/0.40	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.27/0.55	0.30/0.60	0.37/0.70	0.43/0.71	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/0.18	0.77/0.21	0.94/0.26	1.11/0.29	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.38/0.10	0.43/0.12	0.53/0.17	0.62/0.13	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.39/0.10	0.44/0.11	0.53/0.17	0.63/0.12	ns, Min
Clock CLK						
T _{MPW_LRAM}	Minimum pulse width	1.05	1.13	1.25	0.82	ns, Min
T _{MCP}	Minimum clock period	2.10	2.26	2.50	1.64	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 26: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	1.19	1.33	1.61	1.89	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.77	2.15	2.53	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	1.12	1.23	1.46	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.37/0.10	0.41/0.12	0.51/0.17	0.59/0.13	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.37/0.10	0.42/0.11	0.52/0.17	0.60/0.12	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.33/0.34	0.37/0.37	0.44/0.43	0.54/0.47	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.77	0.86	0.98	1.04	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 27: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.85	2.13	2.46	2.87	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.64	0.74	0.89	1.02	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.77	3.04	3.84	5.30	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.73	0.81	0.94	1.11	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with cascade (without output register) ⁽²⁾	2.61	2.88	3.30	3.76	ns, Max
	Clock CLK to DOUT output with cascade (with output register) ⁽⁴⁾	1.16	1.28	1.46	1.56	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.76	0.87	1.05	1.14	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.94	1.02	1.15	1.30	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	1.10	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	4.90	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	1.05	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.15	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.29	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKK_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.45/0.31	0.49/0.33	0.57/0.36	0.77/0.45	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.58/0.60	0.65/0.63	0.74/0.67	0.92/0.76	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.20/0.29	0.22/0.34	0.25/0.41	0.29/0.38	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.50/0.43	0.55/0.46	0.63/0.50	0.78/0.54	ns, Min
T _{RDCK_DI_ECCW} / T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.93/0.43	1.02/0.46	1.17/0.50	1.38/0.48	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	1.04/0.56	1.15/0.59	1.32/0.64	1.55/0.77	ns, Min
T _{RCKK_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	0.92/0.48	ns, Min
T _{RCKK_EN} /T _{RCKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.57/0.26	ns, Min
T _{RCKK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.40/0.19	ns, Min
T _{RCKK_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.41/0.07	ns, Min

PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3				
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 39: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7A100T	0.70	0.70	0.70	1.41	ns
		XC7A200T	0.69	0.69	0.69	1.47	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 40: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
T _{ICKOFCS}	Clock to out of I/O clock	5.01	5.61	6.64	7.34	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/−0.46	2.89/−0.46	3.34/−0.46	5.66/−0.52	ns
		XC7A200T	3.03/−0.50	3.27/−0.50	3.79/−0.50	6.66/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7A100T	2.44/−0.62	2.80/−0.62	3.36/−0.62	2.15/−0.49	ns
		XC7A200T	2.57/−0.63	2.94/−0.63	3.52/−0.63	2.32/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7A100T	2.78/−0.32	3.15/−0.32	3.78/−0.32	2.47/−0.60	ns
		XC7A200T	2.91/−0.33	3.29/−0.33	3.94/−0.33	2.64/−0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 47: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V _{CMOUTDC}	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R _{OUT}	Differential output resistance		–	100	–	Ω
V _{CMOUTAC}	Common mode output voltage: AC coupled		$1/2 V_{MGTAVTT}$			mV
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV _{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V _{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R _{IN}	Differential input resistance		–	100	–	Ω
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

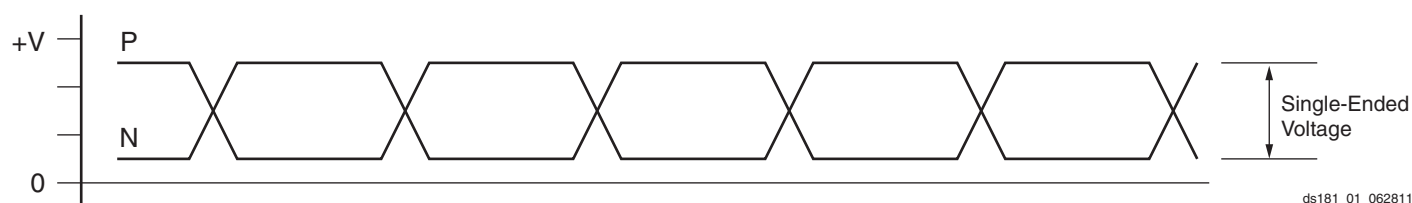


Figure 1: Single-Ended Peak-to-Peak Voltage

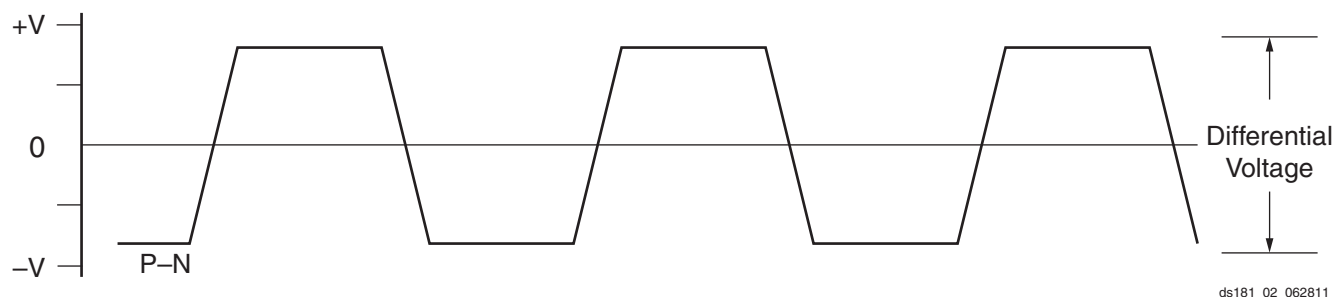


Figure 2: Differential Peak-to-Peak Voltage

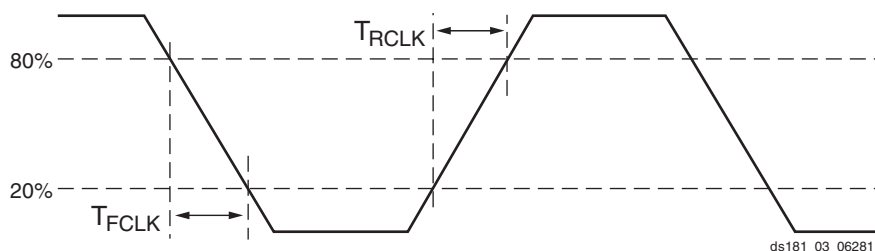


Figure 3: Reference Clock Timing Parameters

Table 52: GTP Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3×10^6	UI

Table 53: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{TXOUT}	TXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz

Notes:

1. Clocking must be implemented as described in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#).

Table 54: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTPTX}	Serial data rate range		0.500	–	F _{GTPMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	50	–	ps
T _{FTX}	TX fall time	20%–80%	–	50	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{6.6}	Total Jitter ⁽²⁾⁽³⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{3.2}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁴⁾	–	–	0.2	UI
DJ _{3.2}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.2L}	Total Jitter ⁽²⁾⁽³⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.32	UI
DJ _{3.2L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₅₀₀	Total Jitter ⁽²⁾⁽³⁾	500 Mb/s	–	–	0.1	UI
DJ ₅₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
- Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 55: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTPMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	5000	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.6}	Sinusoidal Jitter ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using $RXOUT_DIV = 1, 2, \text{ and } 4$.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 1.6 GHz and $RXOUT_DIV = 1$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 2$.
- PLL frequency at 2.5 GHz and $RXOUT_DIV = 4$.
- Composite jitter.

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: CEI-6G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

XADC Specifications

Table 62: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Unipolar operation	–	–	±8	LSBs
		Bipolar operation	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Table 63: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCCKD}	D[31:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCCKCS}	CSI_B setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCCK} /T _{SMCCCKW}	RDWR_B setup/hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICCF}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 64: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I _{FS}	V _{CCAUX} supply current	—	—	115	mA
t _j	Temperature range	15	—	125	°C

Notes:

- The FPGA must not be configured during eFUSE programming.

Date	Version	Description
09/20/12	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24. Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.
02/01/13	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOVBVDDP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCCK} and added the Internal Configuration Access Port section.