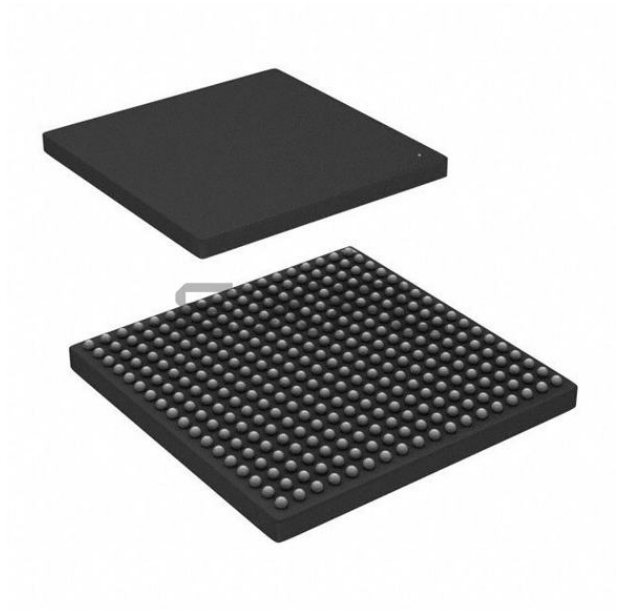

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1000 |
| Number of Logic Elements/Cells | 12800 |
| Total RAM Bits | 737280 |
| Number of I/O | 150 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 324-LFBGA, CSPBGA |
| Supplier Device Package | 324-CSPBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a12t-3csg325e |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. Configuration data is retained even if $V_{CCO}$ drops to 0V.
4. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
8. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.
9. Voltages are specified for the temperature range of $T_j$ = 0°C to +85°C.

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$(2) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$(3) | Battery supply current | – | – | 150 | nA |
| $R_{IN\_TERM}$(4) | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 8:* **SelectIO DC Input and Output Levels(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSTL_II_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.10 | –0.10 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 3 | Note 3 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note 4 | Note 4 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.7 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS33 | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVTTL | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | 2.400 | Note 5 | Note 5 |
| MOBILE_DDR | –0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.10 | –0.10 |
| PCI33_3 | –0.500 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.500 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 1.50 | –0.50 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.00 | –13.00 |
| SSTL135_R | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.90 | –8.90 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.00 | –13.00 |
| SSTL15_R | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.90 | –8.90 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.00 | –8.00 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.40 | –13.40 |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

*Table 12:* **Artix-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7A100T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |
| XC7A200T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 13:* **Artix-7 Device Production Software and Speed Specification Release**

| Device | Speed Grade | | | |
|---|---|---|---|---|
| | 1.0V | | | 0.9V |
| | -3 | -2/-2L | -1 | -2L |
| XC7A100T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |
| XC7A200T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |

**Notes:**
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

*Table 14:* **Networking Applications Interface Performances**

| Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 15:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

| Memory Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| **4:1 Memory Controllers** | | | | | |
| DDR3 | 1066 | 800 | 800 | 800 | Mb/s |
| DDR3L | 800 | 800 | 667 | 667 | Mb/s |
| DDR2 | 800 | 800 | 667 | 667 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 533 | Mb/s |
| **2:1 Memory Controllers** | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | 620 | Mb/s |
| DDR2 | 800 | 700 | 620 | 620 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).

## IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVTTL_S4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.80 | 3.93 | 4.18 | 4.41 | 4.37 | 4.59 | 5.01 | 5.06 | ns |
| LVTTL_S8 | 1.26 | 1.34 | 1.41 | 1.58 | 3.54 | 3.66 | 3.92 | 4.15 | 4.11 | 4.32 | 4.75 | 4.80 | ns |
| LVTTL_S12 | 1.26 | 1.34 | 1.41 | 1.58 | 3.52 | 3.65 | 3.90 | 4.13 | 4.09 | 4.31 | 4.73 | 4.78 | ns |
| LVTTL_S16 | 1.26 | 1.34 | 1.41 | 1.58 | 3.07 | 3.19 | 3.45 | 3.68 | 3.64 | 3.85 | 4.28 | 4.33 | ns |
| LVTTL_S24 | 1.26 | 1.34 | 1.41 | 1.58 | 3.29 | 3.41 | 3.67 | 3.90 | 3.86 | 4.07 | 4.50 | 4.55 | ns |
| LVTTL_F4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.26 | 3.38 | 3.64 | 3.86 | 3.83 | 4.04 | 4.46 | 4.51 | ns |
| LVTTL_F8 | 1.26 | 1.34 | 1.41 | 1.58 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVTTL_F12 | 1.26 | 1.34 | 1.41 | 1.58 | 2.73 | 2.85 | 3.10 | 3.33 | 3.29 | 3.51 | 3.93 | 3.98 | ns |
| LVTTL_F16 | 1.26 | 1.34 | 1.41 | 1.58 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVTTL_F24 | 1.26 | 1.34 | 1.41 | 1.58 | 2.52 | 2.65 | 2.90 | 3.22 | 3.09 | 3.31 | 3.73 | 3.87 | ns |
| LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| MINI_LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| BLVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.84 | 1.96 | 2.21 | 2.44 | 2.40 | 2.62 | 3.04 | 3.09 | ns |
| RSDS_25 (point to point) | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| PPDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.88 | 1.86 | 2.07 | 2.49 | 2.53 | ns |
| TMDS_33 | 0.73 | 0.81 | 0.88 | 0.90 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| PCI33_3 | 1.24 | 1.32 | 1.39 | 1.57 | 3.10 | 3.22 | 3.48 | 3.71 | 3.67 | 3.88 | 4.31 | 4.36 | ns |
| HSUL_12 | 0.67 | 0.75 | 0.82 | 0.87 | 1.80 | 1.93 | 2.18 | 2.41 | 2.37 | 2.59 | 3.01 | 3.06 | ns |
| DIFF_HSUL_12 | 0.68 | 0.76 | 0.83 | 0.88 | 1.80 | 1.93 | 2.18 | 2.21 | 2.37 | 2.59 | 3.01 | 2.86 | ns |
| HSTL_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.62 | 1.74 | 1.99 | 2.19 | 2.19 | 2.40 | 2.82 | 2.84 | ns |
| HSTL_II_S | 0.65 | 0.73 | 0.80 | 0.85 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| HSTL_I_18_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| HSTL_II_18_S | 0.66 | 0.75 | 0.81 | 0.87 | 1.41 | 1.54 | 1.79 | 1.97 | 1.98 | 2.20 | 2.62 | 2.62 | ns |
| DIFF_HSTL_I_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.59 | 1.71 | 1.96 | 2.13 | 2.15 | 2.37 | 2.79 | 2.78 | ns |
| DIFF_HSTL_II_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.51 | 1.63 | 1.88 | 2.07 | 2.08 | 2.29 | 2.71 | 2.72 | ns |
| DIFF_HSTL_I_18_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.96 | 1.95 | 2.17 | 2.59 | 2.61 | ns |
| DIFF_HSTL_II_18_S | 0.70 | 0.78 | 0.85 | 0.87 | 1.46 | 1.58 | 1.84 | 2.00 | 2.03 | 2.24 | 2.67 | 2.65 | ns |
| HSTL_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.10 | 1.22 | 1.48 | 1.69 | 1.67 | 1.88 | 2.31 | 2.34 | ns |

## Input/Output Logic Switching Characteristics

*Table 18:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK | 0.48/0.02 | 0.54/0.02 | 0.76/0.02 | 0.40/–0.07 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin setup/hold with respect to CLK | 0.60/0.01 | 0.70/0.01 | 1.13/0.01 | 0.88/–0.35 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin setup/hold with respect to CLK without Delay | 0.01/0.27 | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY) | 0.02/0.27 | 0.02/0.29 | 0.02/0.33 | 0.01/0.33 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.11 | 0.11 | 0.13 | 0.14 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY) | 0.11 | 0.12 | 0.14 | 0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.41 | 0.44 | 0.51 | 0.54 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) | 0.41 | 0.44 | 0.51 | 0.55 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.53 | 0.57 | 0.66 | 0.71 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out | 0.96 | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum pulse width, SR inputs | 0.61 | 0.72 | 0.72 | 0.68 | ns, Min |

*Table 19:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.67/–0.11 | 0.71/–0.11 | 0.84/–0.11 | 0.60/–0.18 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.10 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.37/0.21 | 0.44/0.21 | 0.80/0.21 | 0.62/–0.25 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.69/–0.14 | 0.73/–0.14 | 0.89/–0.14 | 0.60/–0.18 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.10 | ns |
| **Combinatorial** | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.83 | 0.96 | 1.16 | 1.36 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| $T_{RQ\_OLOGIC}$ | SR pin to OQ/TQ out | 0.72 | 0.80 | 0.95 | 1.12 | ns |
| $T_{GSRQ\_OLOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_OLOGIC}$ | Minimum pulse width, SR inputs | 0.64 | 0.74 | 0.74 | 0.68 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 20:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.14 | 0.02/0.15 | 0.02/0.17 | 0.02/0.21 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.45/–0.01 | 0.50/–0.01 | 0.72/–0.01 | 0.35/–0.11 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.10/0.33 | –0.10/0.36 | –0.10/0.40 | –0.17/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.03/0.19 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.12/0.12 | 0.14/0.14 | 0.17/0.17 | 0.19/0.19 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.53 | 0.54 | 0.66 | 0.67 | ns |
| **Propagation Delays** | | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.11 | 0.11 | 0.13 | 0.14 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

## Output Serializer/Deserializer Switching Characteristics

*Table 21:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.44/–0.25 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.60/–0.25 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.46/–0.25 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.15 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.70 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.54 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| **Combinatorial** | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.83 | 0.92 | 1.11 | 1.18 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

*Table 23:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **IO_FIFO Clock to Out Delays** | | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs | 0.55 | 0.60 | 0.68 | 0.81 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags | 0.55 | 0.61 | 0.77 | 0.55 | ns |
| **Setup/Hold** | | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK | 0.47/0.02 | 0.51/0.02 | 0.58/0.02 | 0.76/–0.05 | ns |
| $T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$ | WREN to WRCLK | 0.42/–0.01 | 0.47/–0.01 | 0.53/–0.01 | 0.70/–0.05 | ns |
| $T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK | 0.53/0.02 | 0.58/0.02 | 0.66/0.02 | 0.79/–0.02 | ns |
| **Minimum Pulse Width** | | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 266.67 | 200.00 | 200.00 | 200.00 | MHz |

## Block RAM and FIFO Switching Characteristics

*Table 27:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.85 | 2.13 | 2.46 | 2.87 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.64 | 0.74 | 0.89 | 1.02 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.77 | 3.04 | 3.84 | 5.30 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.73 | 0.81 | 0.94 | 1.11 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with cascade (without output register)[2] | 2.61 | 2.88 | 3.30 | 3.76 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register)[4] | 1.16 | 1.28 | 1.46 | 1.56 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.76 | 0.87 | 1.05 | 1.14 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.94 | 1.02 | 1.15 | 1.30 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.78 | 0.85 | 0.94 | 1.10 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register) | 2.56 | 2.81 | 3.55 | 4.90 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.68 | 0.76 | 0.89 | 1.05 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.75 | 0.88 | 1.07 | 1.15 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.84 | 0.93 | 1.08 | 1.29 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$ | ADDR inputs[8] | 0.45/0.31 | 0.49/0.33 | 0.57/0.36 | 0.77/0.45 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9] | 0.58/0.60 | 0.65/0.63 | 0.74/0.67 | 0.92/0.76 | ns, Min |
| $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode[9] | 0.20/0.29 | 0.22/0.34 | 0.25/0.41 | 0.29/0.38 | ns, Min |
| $T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.50/0.43 | 0.55/0.46 | 0.63/0.50 | 0.78/0.54 | ns, Min |
| $T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only[9] | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.38/0.48 | ns, Min |
| $T_{RDCK\_DI\_ECC\_FIFO}/T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode[9] | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.55/0.77 | ns, Min |
| $T_{RCCK\_INJECTBITERR}/T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.58/0.35 | 0.64/0.37 | 0.74/0.40 | 0.92/0.48 | ns, Min |
| $T_{RCCK\_EN}/T_{RCKC\_EN}$ | Block RAM enable (EN) input | 0.35/0.20 | 0.39/0.21 | 0.45/0.23 | 0.57/0.26 | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | 0.24/0.15 | 0.29/0.15 | 0.36/0.16 | 0.40/0.19 | ns, Min |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.29/0.07 | 0.32/0.07 | 0.35/0.07 | 0.41/0.07 | ns, Min |

## DSP48E1 Switching Characteristics

*Table 28:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.26/ 0.12 | 0.30/ 0.13 | 0.37/ 0.14 | 0.45/ 0.14 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.33/ 0.15 | 0.38/ 0.16 | 0.45/ 0.18 | 0.60/ 0.19 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.17/ 0.17 | 0.20/ 0.19 | 0.24/ 0.21 | 0.34/ 0.29 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.25/ 0.25 | 0.32/ 0.27 | 0.42/ 0.27 | 0.54/ 0.23 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.23/ 0.12 | 0.27/ 0.13 | 0.32/ 0.14 | 0.36/ 0.14 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.25/ 0.15 | 0.29/ 0.16 | 0.36/ 0.18 | 0.41/ 0.19 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/ –0.01 | 2.76/ –0.01 | 3.29/ –0.01 | 4.31/ –0.07 | ns |
| $T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$ | {A, D} input to AD register CLK | 1.29/ –0.02 | 1.48/ –0.02 | 1.76/ –0.02 | 2.29/ –0.27 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/ –0.28 | 4.60/ –0.28 | 5.48/ –0.28 | 6.95/ –0.48 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.93/ –0.73 | 4.50/ –0.73 | 5.35/ –0.73 | 6.73/ –1.68 | ns |
| $T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/ –0.28 | 1.98/ –0.28 | 2.35/ –0.28 | 2.80/ –0.48 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.54/ –0.26 | 1.76/ –0.26 | 2.10/ –0.26 | 2.54/ –0.45 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.32/ –0.15 | 1.51/ –0.15 | 1.80/ –0.15 | 2.13/ –0.25 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/ 0.06 | 0.42/ 0.08 | 0.52/ 0.11 | 0.64/ 0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.28/ 0.10 | 0.34/ 0.11 | 0.42/ 0.13 | 0.49/ 0.16 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.36/ –0.03 | 0.43/ –0.03 | 0.52/ –0.03 | 0.68/ 0.14 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.17/ 0.18 | 0.21/ 0.20 | 0.27/ 0.23 | 0.45/ 0.29 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.36/ 0.01 | 0.43/ 0.01 | 0.53/ 0.01 | 0.63/ 0.00 | ns |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of the RST Pins** | | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/ 0.11 | 0.46/ 0.13 | 0.55/ 0.15 | 0.63/ 0.40 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.07/ 0.10 | 0.08/ 0.11 | 0.09/ 0.12 | 0.13/ 0.11 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.44/ 0.07 | 0.50/ 0.08 | 0.59/ 0.09 | 0.67/ 0.08 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.21/ 0.22 | 0.23/ 0.24 | 0.27/ 0.28 | 0.28/ 0.35 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.27/ 0.01 | 0.30/ 0.01 | 0.35/ 0.01 | 0.43/ 0.00 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier | 3.79 | 4.35 | 5.18 | 6.61 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier | 3.72 | 4.26 | 5.07 | 6.41 | ns |
| $T_{DSPDO\_B\_P}$ | B input to P output not using multiplier | 1.53 | 1.75 | 2.08 | 2.48 | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output | 1.33 | 1.53 | 1.82 | 2.22 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.55 | 0.63 | 0.74 | 0.87 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier | 4.06 | 4.65 | 5.54 | 7.03 | ns |
| $T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$ | D input to CARRYCASCOUT output using multiplier | 3.97 | 4.54 | 5.40 | 6.81 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77 | 2.03 | 2.41 | 2.88 | ns |
| $T_{DSPDO\_C\_CARRYCASCOUT}$ | C input to CARRYCASCOUT output | 1.58 | 1.81 | 2.15 | 2.62 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | |
| $T_{DSPDO\_ACIN\_P\_MULT}$ | ACIN input to P output using multiplier | 3.65 | 4.19 | 5.00 | 6.40 | ns |
| $T_{DSPDO\_ACIN\_P}$ | ACIN input to P output not using multiplier | 1.37 | 1.57 | 1.88 | 2.44 | ns |
| $T_{DSPDO\_ACIN\_ACOUT}$ | ACIN input to ACOUT output | 0.38 | 0.44 | 0.53 | 0.63 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier | 3.90 | 4.47 | 5.33 | 6.79 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier | 1.61 | 1.85 | 2.21 | 2.84 | ns |
| $T_{DSPDO\_PCIN\_P}$ | PCIN input to P output | 1.11 | 1.28 | 1.52 | 1.82 | ns |
| $T_{DSPDO\_PCIN\_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output | 1.36 | 1.56 | 1.85 | 2.21 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK PREG to P output | 0.33 | 0.37 | 0.44 | 0.54 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_PREG}$ | CLK PREG to CARRYCASCOUT output | 0.52 | 0.59 | 0.69 | 0.84 | ns |

*Table 32:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| $T_{BHCCK\_CE}/T_{BHCKC\_CE}$ | CE pin setup and hold | 0.19/0.13 | 0.22/0.15 | 0.28/0.21 | 0.35/0.08 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 394.00 | MHz |

*Table 33:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $T_{DCD\_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7A100T | 0.27 | 0.33 | 0.36 | 0.48 | ns |
| | | XC7A200T | 0.40 | 0.48 | 0.54 | 0.69 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

*Table 34:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| MMCM_$F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| MMCM_$F_{MIN_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_$F_{MAX_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| MMCM_$F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |

*Table 34:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

## PLL Switching Characteristics

*Table 35:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $PLL\_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| $PLL\_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| $PLL\_F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| $PLL\_F_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| $PLL\_F_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $PLL\_T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $PLL\_T_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | |
| $PLL\_T_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $PLL\_T_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $PLL\_F_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| $PLL\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $PLL\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $PLL\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $PLL\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| $PLL\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| $T_{PLLDCK\_DADDR}$/ $T_{PLLCKD\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DI}/T_{PLLCKD\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DEN}$/ $T_{PLLCKD\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{PLLDCK\_DWE}$/ $T_{PLLCKD\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

*Table 44:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.31 | –0.38/1.46 | –0.38/1.76 | –0.16/1.89 | ns |

*Table 45:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

*Table 46:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7A100T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |
| | | XC7A200T | SBG484 | 111 | ps |
| | | | FBG484 | 109 | ps |
| | | | FBG676 | 121 | ps |
| | | | FFG1156 | 151 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# XADC Specifications

*Table 62:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±2 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Unipolar operation | – | – | ±8 | LSBs |
| | | Bipolar operation | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 70 | – | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |

*Table 63:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Internal Configuration Access Port** | | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{CCO}$ | DOUT clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | D[31:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B setup/hold | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 7.00 | 7.00 | 7.00 | 8.00 | ns, Max |
| $T_{SMCO}$ | D[31:00] clock to out in readback | 8.00 | 8.00 | 8.00 | 10.00 | ns, Max |
| $F_{RBCCK}$ | Readback frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI setup/hold | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output | 7.00 | 7.00 | 7.00 | 8.50 | ns, Max |
| $F_{TCK}$ | TCK frequency | 66.00 | 66.00 | 66.00 | 50.00 | MHz, Max |
| **BPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{BPICCO}$ (2) | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | 8.50 | 8.50 | 8.50 | 10.00 | ns, Max |
| $T_{BPIDCC}/T_{BPICCD}$ | D[15:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| **SPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{SPIDCC}/T_{SPICCD}$ | D[03:00] setup/hold | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | ns, Min |
| $T_{SPICCM}$ | MOSI clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

*Table 64:* **eFUSE Programming Conditions** (1)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $t_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

| Date | Version | Description |
|---|---|---|
| 09/20/12 | 1.4 | In Table 1, updated the descriptions, changed $V_{IN}$ and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet.<br>Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and $T_{CINCK}/T_{CKCIN}$ from Table 24.Changed $F_{PFDMAX}$ conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated $T_{POR}$. |
| 02/01/13 | 1.5 | Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications.<br>Revised $I_{DCIN}$ and $I_{DCOUT}$ and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46.<br>Updated $D_{VPPIN}$ in Table 47. Updated $V_{IDIFF}$ in Table 48. Removed $T_{LOCK}$ and $T_{PHASE}$ and revised $F_{GCLK}$ in Table 51. Updated $T_{DLOCK}$ in Table 52. Updated Table 53. In Table 54, updated $T_{RTX}$, $T_{FTX}$, $V_{TXOOBVDPP}$, and revised Note 1 through Note 7. In Table 55, updated $RX_{SST}$ and $RX_{PPMTOL}$ and revised Note 4 through Note 7. In Table 60, revised and added Note 1.<br>Revised the maximum external channel input ranges in Table 62. In Table 63, revised $F_{MCCK}$ and added the Internal Configuration Access Port section. |