



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	16825
Number of Logic Elements/Cells	215360
Total RAM Bits	13455360
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a200t-1fbg676c

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.10	-0.10
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.7	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.10	-0.10
PCI33_3	-0.500	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.50	-0.50
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.00	-13.00
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.90	-8.90
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.00	-13.00
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.90	-8.90
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.00	-8.00
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.40	-13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see [UG471](#): 7 Series FPGAs SelectIO Resources User Guide.

Table 9: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO}-0.405$	$V_{CCO}-0.300$	$V_{CCO}-0.190$	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \bar{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	-0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	-0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	-13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	-8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	-13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	-8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	-8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	-13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 12](#) correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: Artix-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 13](#) lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: Artix-7 Device Production Software and Speed Specification Release

Device	Speed Grade		
	1.0V		0.9V
	-3	-2/-2L	-1
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 9](#).

Table 14: Networking Applications Interface Performances

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽¹⁾⁽²⁾

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Input/Output Logic Switching Characteristics

Table 18: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.40/−0.07	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/−0.35	ns
T _{IDOCK} /T _{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
T _{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T _{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.68	ns, Min

Table 19: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/−0.11	0.71/−0.11	0.84/−0.11	0.60/−0.18	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/−0.10	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/−0.25	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/−0.14	0.73/−0.14	0.89/−0.14	0.60/−0.18	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/−0.10	ns
Combinatorial						
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
T _{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
T _{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.68	ns, Min

Table 23: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.81	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.55	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.76/−0.05	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.42/−0.01	0.47/−0.01	0.53/−0.01	0.70/−0.05	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.79/−0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

CLB Switching Characteristics

Table 24: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T _{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T _{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T _{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T _{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T _{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T _{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T _{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T _{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T _{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.20	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.31	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.97/0.12	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.34/–0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.62/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

Block RAM and FIFO Switching Characteristics

Table 27: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.85	2.13	2.46	2.87	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.64	0.74	0.89	1.02	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.77	3.04	3.84	5.30	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.73	0.81	0.94	1.11	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with cascade (without output register) ⁽²⁾	2.61	2.88	3.30	3.76	ns, Max
	Clock CLK to DOUT output with cascade (with output register) ⁽⁴⁾	1.16	1.28	1.46	1.56	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.76	0.87	1.05	1.14	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.94	1.02	1.15	1.30	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	1.10	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	4.90	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	1.05	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.15	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.29	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKCK_ADDRA} /T _{RCKKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.45/0.31	0.49/0.33	0.57/0.36	0.77/0.45	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.58/0.60	0.65/0.63	0.74/0.67	0.92/0.76	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.20/0.29	0.22/0.34	0.25/0.41	0.29/0.38	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.50/0.43	0.55/0.46	0.63/0.50	0.78/0.54	ns, Min
T _{RDCK_DI_ECCW} / T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.93/0.43	1.02/0.46	1.17/0.50	1.38/0.48	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	1.04/0.56	1.15/0.59	1.32/0.64	1.55/0.77	ns, Min
T _{RCKCK_INJECTBITERR} / T _{RCKKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	0.92/0.48	ns, Min
T _{RCKCK_EN} /T _{RCKKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.57/0.26	ns, Min
T _{RCKCK_REGCE} /T _{RCKKC_REGCE}	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.40/0.19	ns, Min
T _{RCKCK_RSTREG} /T _{RCKKC_RSTREG}	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.41/0.07	ns, Min

PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3				
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 36: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7A100T	5.14	5.74	6.72	7.64	ns
		XC7A200T	5.47	6.11	7.16	8.10	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 37: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7A100T	5.38	6.01	7.02	7.96	ns
		XC7A200T	6.17	6.89	8.05	9.05	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 38: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7A100T	0.89	0.94	0.96	1.81	ns
		XC7A200T	0.90	0.97	1.01	1.86	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 39: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFFLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7A100T	0.70	0.70	0.70	1.41	ns
		XC7A200T	0.69	0.69	0.69	1.47	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 40: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
T _{ICKOFCS}	Clock to out of I/O clock	5.01	5.61	6.64	7.34	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/−0.46	2.89/−0.46	3.34/−0.46	5.66/−0.52	ns
		XC7A200T	3.03/−0.50	3.27/−0.50	3.79/−0.50	6.66/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7A100T	2.44/−0.62	2.80/−0.62	3.36/−0.62	2.15/−0.49	ns
		XC7A200T	2.57/−0.63	2.94/−0.63	3.52/−0.63	2.32/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7A100T	2.78/−0.32	3.15/−0.32	3.78/−0.32	2.47/−0.60	ns
		XC7A200T	2.91/−0.33	3.29/−0.33	3.94/−0.33	2.64/−0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 47: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		$1/2 V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

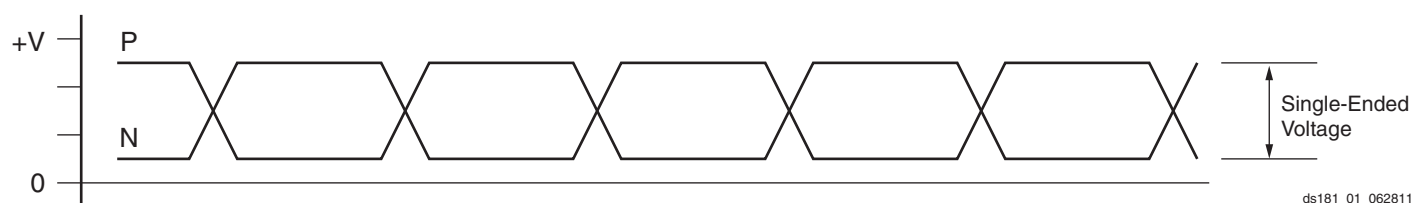


Figure 1: Single-Ended Peak-to-Peak Voltage

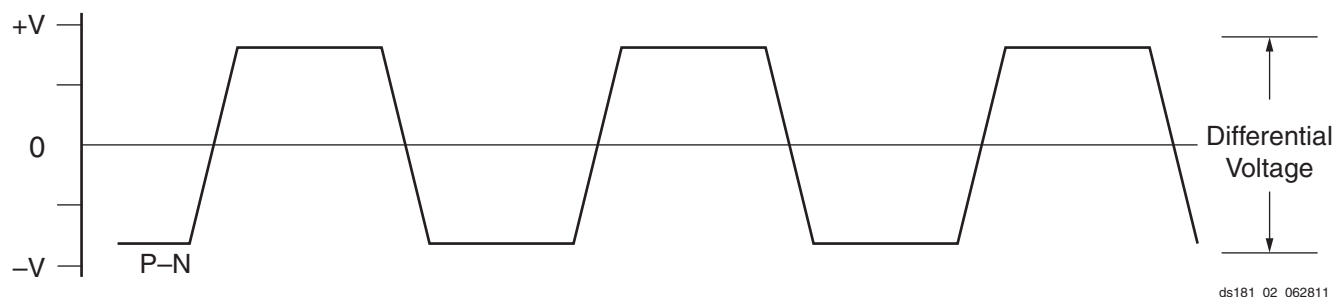


Figure 2: Differential Peak-to-Peak Voltage

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 48: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further information.

Table 49: GTP Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1		-2L		
			Package Type								
			FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	
F _{GTPMAX}	Maximum GTP transceiver data rate		6.6	5.4	6.6	5.4	3.75	3.75	3.75	3.75	Gb/s
F _{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F _{GTPRANGE}	PLL line rate range	1	3.2–6.6		3.2–6.6		3.2–3.75		3.2–3.75		Gb/s
		2	1.6–3.3		1.6–3.3		1.6–3.2		1.6–3.2		Gb/s
		4	0.8–1.65		0.8–1.65		0.8–1.6		0.8–1.6		Gb/s
		8	0.5–0.825		0.5–0.825		0.5–0.8		0.5–0.8		Gb/s
F _{GTPPLL} RANGE	GTP transceiver PLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz

Table 50: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTPDRPCLK}	GTPDRPCLK maximum frequency	175	175	156	125	MHz

Table 51: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range		60	–	660	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	20% – 80%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Table 62: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference⁽⁵⁾						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted. On-chip reference variation is $\pm 1\%$.

Configuration Switching Characteristics

Table 63: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5.00	5.00	5.00	5.00	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 11 . Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13 . Added $MMCM_T_{FBDELAY}$ while adding $MMCM_$ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35 . In Table 36 through Table 43 , updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46 .
02/13/12	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1 . In Table 2 , revised V_{CCO} for the 3.3V HR I/O banks and updated T_j . Updated the notes in Table 5 . Added MGTAVCC and MGTAVTT power supply ramp times to Table 7 . Rearranged Table 8 , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10 . Revised the specifications in Table 11 . Revised V_{IN} in Table 47 . Updated the eFUSE Programming Conditions section and removed the endurance table. Added the table. Revised F_{TXIN} and F_{RXIN} in Table 53 . Revised I_{CCADC} and updated Note 1 in Table 62 . Revised DDR LVDS transmitter data width in Table 14 . Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63 . Updated Note 1 in Table 33 .
06/01/12	1.3	Reorganized entire data sheet including adding Table 40 and Table 44 . Updated T_{SOL} in Table 1 . Updated I_{BATT} and added R_{IN_TERM} to Table 3 . Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8 , updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 10 . Updated V_{OL} in Table 11 . Updated Table 14 and removed notes 2 and 3. Updated Table 15 . Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 27 , updated Reset Delays section including Note 10 and Note 11 . In Table 53 , replaced F_{TXOUT} with F_{GLK} . Updated many of the XADC specifications in Table 62 and added Note 2 . Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 63 to Table 34 and Table 35 .

Date	Version	Description
09/20/12	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24. Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.
02/01/13	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOVBVDDP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCKK} and added the Internal Configuration Access Port section.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.