AMD Xilinx - XC7A200T-1SBG484C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	16825
Number of Logic Elements/Cells	215360
Total RAM Bits	13455360
Number of I/O	285
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, FCBGA
Supplier Device Package	484-FCBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a200t-1sbg484c

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
8. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.
9. Voltages are specified for the temperature range of T_j = 0°C to +85°C.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}(2)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}(3)	Battery supply current	–	–	150	nA
R_{IN_TERM}(4)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices	44	60	83	Ω

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	61.7
V_{CCO} + 0.50	100	–0.50	25.8
V_{CCO} + 0.55	100	–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.500	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the LVDS_25 standard in the HR I/O banks.

Table 11: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in v1.07 from the 14.4/2012.4 device pack for ISE® Design Suite14.4 and Vivado® Design Suite 2012.4 for the -3, -2, -2L (1.0V), and -1 speed grades and v1.05 from the 14.4/2012.4 device pack for the -2L (0.9V) speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: **Artix-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: **Artix-7 Device Production Software and Speed Specification Release**

Device	Speed Grade			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Input/Output Logic Switching Characteristics

Table 18: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.40/–0.07	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/–0.35	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.68	ns, Min

Table 19: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.60/–0.18	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/–0.10	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/–0.25	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.60/–0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/–0.10	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.68	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 21: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.44/–0.25	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	0.60/–0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	0.46/–0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/–0.15	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/–0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.83	0.92	1.11	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 23: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.55	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.76/–0.05	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	0.70/–0.05	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.79/–0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

CLB Switching Characteristics

Table 24: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.20	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.31	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.97/0.12	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.34/–0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.62/0.05	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	2.22	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	363.77	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	310.08	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	210.44	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	191.28	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	150.13	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	140.10	MHz

Table 39: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7A100T	0.70	0.70	0.70	1.41	ns
		XC7A200T	0.69	0.69	0.69	1.47	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 40: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
$T_{ICKOFCS}$	Clock to out of I/O clock	5.01	5.61	6.64	7.34	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/–0.46	2.89/–0.46	3.34/–0.46	5.66/–0.52	ns
		XC7A200T	3.03/–0.50	3.27/–0.50	3.79/–0.50	6.66/–0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7A100T	2.44/–0.62	2.80/–0.62	3.36/–0.62	2.15/–0.49	ns
		XC7A200T	2.57/–0.63	2.94/–0.63	3.52/–0.63	2.32/–0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7A100T	2.78/–0.32	3.15/–0.32	3.78/–0.32	2.47/–0.60	ns
		XC7A200T	2.91/–0.33	3.29/–0.33	3.94/–0.33	2.64/–0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock	–0.38/1.31	–0.38/1.46	–0.38/1.76	–0.16/1.89	ns

Table 45: **Sample Window**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling error at receiver pins(1)	0.59	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.35	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 46: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7A100T	CSG324	113	ps
			FTG256	120	ps
			FGG484	144	ps
			FGG676	153	ps
		XC7A200T	SBG484	111	ps
			FBG484	109	ps
			FBG676	121	ps
			FFG1156	151	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

Table 47: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		1/2 $V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG482: *7 Series FPGAs GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

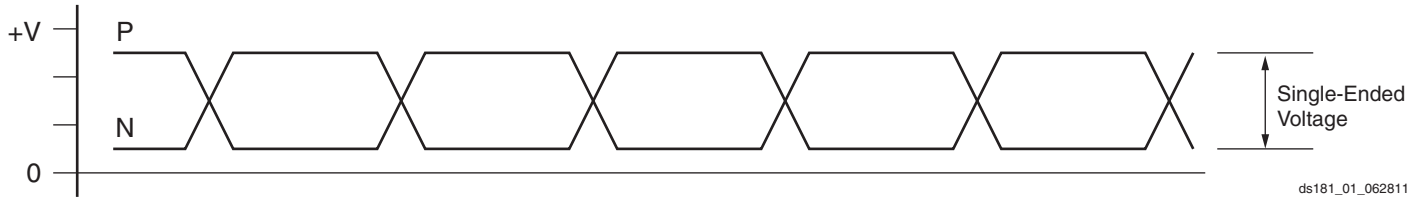

Figure 1: **Single-Ended Peak-to-Peak Voltage**

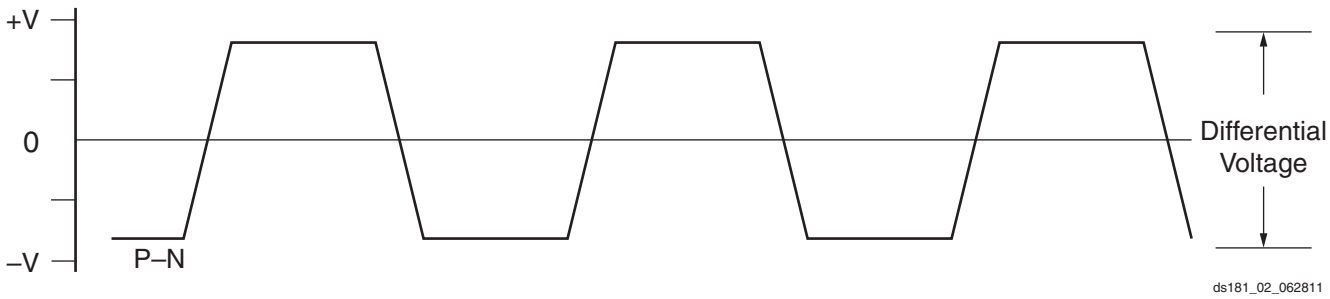

Figure 2: **Differential Peak-to-Peak Voltage**

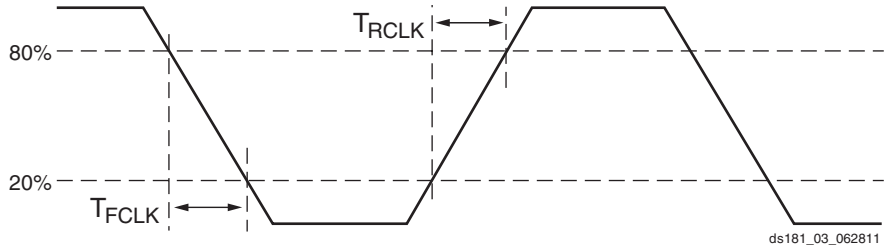

Figure 3: **Reference Clock Timing Parameters**

Table 52: **GTP Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3×10^6	UI

Table 53: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{TXOUT}	TXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz

Notes:

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the UG482: *7 Series FPGAs GTP Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: **PCI Express Protocol Characteristics(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: **CEI-6G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 63: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F_{RBCCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching						
T_{BPICCO} (2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

Table 64: **eFUSE Programming Conditions** (1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.