# AMD Xilinx - XC7A200T-2FBG676I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 16825 |
| Number of Logic Elements/Cells | 215360 |
| Total RAM Bits | 13455360 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BBGA, FCBGA |
| Supplier Device Package | 676-FCBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a200t-2fbg676i |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies (6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies (6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applied to DC signals.
5. For maximum undershoot and overshoot AC specifications, see Table 4.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$ | Internal supply voltage | 0.95 | 1.00 | 1.05 | V |
| | For -2L (0.9V) devices: internal supply voltage | 0.87 | 0.90 | 0.93 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$ | Block RAM supply voltage | 0.95 | 1.00 | 1.05 | V |
| $V_{CCO}$(3)(4) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| $V_{IN}$(5) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage for $V_{REF}$ and differential I/O standards | –0.20 | – | 2.625 | V |
| $I_{IN}$(6) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(7) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTP Transceiver** | | | | | |
| $V_{MGTAVCC}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver circuits | 0.97 | 1.0 | 1.03 | V |
| $V_{MGTAVTT}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.40 | 100 | –0.40 | 100 |
| $V_{CCO}$ + 0.45 | 100 | –0.45 | 61.7 |
| $V_{CCO}$ + 0.50 | 100 | –0.50 | 25.8 |
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7A100T | 155 | 155 | 155 | 108 | mA |
| | | XC7A200T | 328 | 328 | 328 | 232 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 5 | 5 | 5 | 5 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7A100T | 36 | 36 | 36 | 36 | mA |
| | | XC7A200T | 73 | 73 | 73 | 73 | mA |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 11 | 11 | 11 | 11 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Table 6 shows the minimum current, in addition to $I_{CCQ}$, that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after $V_{CCINT}$ is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

*Table 6:* **Power-On Current for Artix-7 Devices(1)**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|
| | Typ(2) | Typ(2) | Typ(2) | Typ(2) | |
| XC7A100T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A200T | $I_{CCINTQ}$ + 340 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 80 | mA |

**Notes:**

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$ | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$ | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ | $T_J = 100°C$(1) | – | 500 | ms |
| | | $T_J = 85°C$(1) | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |

**Notes:**

1. Based on 240,000 power cycles with nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with worst case $V_{CCO}$ of 3.465V.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 8:* **SelectIO DC Input and Output Levels(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSTL_II_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.10 | –0.10 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 3 | Note 3 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note 4 | Note 4 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.7 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS33 | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVTTL | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | 2.400 | Note 5 | Note 5 |
| MOBILE_DDR | –0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.10 | –0.10 |
| PCI33_3 | –0.500 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.500 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 1.50 | –0.50 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.00 | –13.00 |
| SSTL135_R | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.90 | –8.90 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.00 | –13.00 |
| SSTL15_R | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.90 | –8.90 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.00 | –8.00 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.40 | –13.40 |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

*Table 12:* **Artix-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7A100T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |
| XC7A200T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 13:* **Artix-7 Device Production Software and Speed Specification Release**

| Device | Speed Grade | | | |
|---|---|---|---|---|
| | 1.0V | | | 0.9V |
| | -3 | -2/-2L | -1 | -2L |
| XC7A100T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |
| XC7A200T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |

**Notes:**
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

*Table 14:* **Networking Applications Interface Performances**

| Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 15:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

| Memory Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| **4:1 Memory Controllers** | | | | | |
| DDR3 | 1066 | 800 | 800 | 800 | Mb/s |
| DDR3L | 800 | 800 | 667 | 667 | Mb/s |
| DDR2 | 800 | 800 | 667 | 667 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 533 | Mb/s |
| **2:1 Memory Controllers** | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | 620 | Mb/s |
| DDR2 | 800 | 700 | 620 | 620 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| HSTL_II_F | 0.65 | 0.73 | 0.80 | 0.85 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| HSTL_I_18_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.13 | 1.26 | 1.51 | 1.72 | 1.70 | 1.92 | 2.34 | 2.37 | ns |
| HSTL_II_18_F | 0.66 | 0.75 | 0.81 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_HSTL_I_F | 0.68 | 0.76 | 0.83 | 0.85 | 1.18 | 1.30 | 1.56 | 1.77 | 1.75 | 1.96 | 2.39 | 2.42 | ns |
| DIFF_HSTL_II_F | 0.68 | 0.76 | 0.83 | 0.85 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| DIFF_HSTL_I_18_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| DIFF_HSTL_II_18_F | 0.70 | 0.78 | 0.85 | 0.87 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| LVCMOS33_S4 | 1.26 | 1.34 | 1.41 | 1.62 | 3.80 | 3.93 | 4.18 | 4.41 | 4.37 | 4.59 | 5.01 | 5.06 | ns |
| LVCMOS33_S8 | 1.26 | 1.34 | 1.41 | 1.62 | 3.52 | 3.65 | 3.90 | 4.13 | 4.09 | 4.31 | 4.73 | 4.78 | ns |
| LVCMOS33_S12 | 1.26 | 1.34 | 1.41 | 1.62 | 3.09 | 3.21 | 3.46 | 3.69 | 3.65 | 3.87 | 4.29 | 4.34 | ns |
| LVCMOS33_S16 | 1.26 | 1.34 | 1.41 | 1.62 | 3.40 | 3.52 | 3.77 | 4.00 | 3.97 | 4.18 | 4.60 | 4.65 | ns |
| LVCMOS33_F4 | 1.26 | 1.34 | 1.41 | 1.62 | 3.26 | 3.38 | 3.64 | 3.86 | 3.83 | 4.04 | 4.46 | 4.51 | ns |
| LVCMOS33_F8 | 1.26 | 1.34 | 1.41 | 1.62 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVCMOS33_F12 | 1.26 | 1.34 | 1.41 | 1.62 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVCMOS33_F16 | 1.26 | 1.34 | 1.41 | 1.62 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVCMOS25_S4 | 1.12 | 1.20 | 1.27 | 1.43 | 3.13 | 3.26 | 3.51 | 3.72 | 3.70 | 3.91 | 4.34 | 4.37 | ns |
| LVCMOS25_S8 | 1.12 | 1.20 | 1.27 | 1.43 | 2.88 | 3.01 | 3.26 | 3.49 | 3.45 | 3.67 | 4.09 | 4.14 | ns |
| LVCMOS25_S12 | 1.12 | 1.20 | 1.27 | 1.43 | 2.48 | 2.60 | 2.85 | 3.08 | 3.05 | 3.26 | 3.68 | 3.73 | ns |
| LVCMOS25_S16 | 1.12 | 1.20 | 1.27 | 1.43 | 2.82 | 2.94 | 3.20 | 3.43 | 3.39 | 3.60 | 4.03 | 4.08 | ns |
| LVCMOS25_F4 | 1.12 | 1.20 | 1.27 | 1.43 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVCMOS25_F8 | 1.12 | 1.20 | 1.27 | 1.43 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS25_F12 | 1.12 | 1.20 | 1.27 | 1.43 | 2.16 | 2.29 | 2.54 | 2.77 | 2.73 | 2.95 | 3.37 | 3.42 | ns |
| LVCMOS25_F16 | 1.12 | 1.20 | 1.27 | 1.43 | 2.01 | 2.13 | 2.39 | 2.61 | 2.58 | 2.79 | 3.21 | 3.26 | ns |
| LVCMOS18_S4 | 0.74 | 0.83 | 0.89 | 0.94 | 1.62 | 1.74 | 1.99 | 2.19 | 2.19 | 2.40 | 2.82 | 2.84 | ns |
| LVCMOS18_S8 | 0.74 | 0.83 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS18_S12 | 0.74 | 0.83 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS18_S16 | 0.74 | 0.83 | 0.89 | 0.94 | 1.52 | 1.65 | 1.90 | 2.13 | 2.09 | 2.31 | 2.73 | 2.78 | ns |
| LVCMOS18_S24 | 0.74 | 0.83 | 0.89 | 0.94 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS18_F4 | 0.74 | 0.83 | 0.89 | 0.94 | 1.45 | 1.57 | 1.82 | 2.05 | 2.01 | 2.23 | 2.65 | 2.70 | ns |
| LVCMOS18_F8 | 0.74 | 0.83 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.29 | 2.25 | 2.46 | 2.89 | 2.94 | ns |
| LVCMOS18_F12 | 0.74 | 0.83 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.29 | 2.25 | 2.46 | 2.89 | 2.94 | ns |
| LVCMOS18_F16 | 0.74 | 0.83 | 0.89 | 0.94 | 1.40 | 1.52 | 1.77 | 2.00 | 1.97 | 2.18 | 2.60 | 2.65 | ns |
| LVCMOS18_F24 | 0.74 | 0.83 | 0.89 | 0.94 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS15_S4 | 0.77 | 0.86 | 0.93 | 0.98 | 2.05 | 2.18 | 2.43 | 2.50 | 2.62 | 2.84 | 3.26 | 3.15 | ns |
| LVCMOS15_S8 | 0.77 | 0.86 | 0.93 | 0.98 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS15_S12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 2.19 | 2.15 | 2.37 | 2.79 | 2.84 | ns |
| LVCMOS15_S16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 2.19 | 2.15 | 2.37 | 2.79 | 2.84 | ns |

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.98 | 1.85 | 1.97 | 2.23 | 2.27 | 2.42 | 2.63 | 3.06 | 2.92 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.98 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.35 | 1.47 | 1.73 | 1.96 | 1.92 | 2.13 | 2.56 | 2.61 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.08 | 2.57 | 2.69 | 2.95 | 3.18 | 3.14 | 3.35 | 3.78 | 3.83 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.08 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.79 | 1.91 | 2.17 | 2.40 | 2.36 | 2.57 | 2.99 | 3.05 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.08 | 1.98 | 2.10 | 2.35 | 2.58 | 2.54 | 2.76 | 3.18 | 3.23 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.08 | 1.54 | 1.66 | 1.92 | 2.15 | 2.11 | 2.32 | 2.75 | 2.80 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.38 | 1.51 | 1.76 | 1.97 | 1.95 | 2.16 | 2.59 | 2.62 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.80 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.67 | 1.79 | 2.04 | 2.24 | 2.23 | 2.45 | 2.87 | 2.89 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.31 | 1.43 | 1.68 | 1.91 | 1.87 | 2.09 | 2.51 | 2.56 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.68 | 1.80 | 2.06 | 2.24 | 2.25 | 2.46 | 2.89 | 2.89 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.94 | 1.95 | 2.17 | 2.59 | 2.59 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.80 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.72 | 1.69 | 1.90 | 2.32 | 2.37 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.23 | 1.35 | 1.60 | 1.80 | 1.79 | 2.01 | 2.43 | 2.45 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.79 | 1.78 | 1.99 | 2.42 | 2.44 | ns |

Table 17 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 17:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.19 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.30 | ns |

## Output Serializer/Deserializer Switching Characteristics

*Table 21:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.44/–0.25 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.60/–0.25 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.46/–0.25 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.15 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.70 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.54 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| **Combinatorial** | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.83 | 0.92 | 1.11 | 1.18 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

*Table 23:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **IO_FIFO Clock to Out Delays** | | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs | 0.55 | 0.60 | 0.68 | 0.81 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags | 0.55 | 0.61 | 0.77 | 0.55 | ns |
| **Setup/Hold** | | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK | 0.47/0.02 | 0.51/0.02 | 0.58/0.02 | 0.76/–0.05 | ns |
| $T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$ | WREN to WRCLK | 0.42/–0.01 | 0.47/–0.01 | 0.53/–0.01 | 0.70/–0.05 | ns |
| $T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK | 0.53/0.02 | 0.58/0.02 | 0.66/0.02 | 0.79/–0.02 | ns |
| **Minimum Pulse Width** | | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 266.67 | 200.00 | 200.00 | 200.00 | MHz |

## CLB Switching Characteristics

*Table 24:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.10 | 0.11 | 0.13 | 0.15 | ns, Max |
| $T_{ILO\_2}$ | An – Dn LUT address to AMUX/CMUX | 0.27 | 0.30 | 0.36 | 0.41 | ns, Max |
| $T_{ILO\_3}$ | An – Dn LUT address to BMUX_A | 0.42 | 0.46 | 0.55 | 0.65 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.94 | 1.05 | 1.27 | 1.51 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.62 | 0.69 | 0.84 | 1.01 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.58 | 0.66 | 0.83 | 0.98 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.60 | 0.68 | 0.82 | 0.98 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.68 | 0.75 | 0.90 | 1.08 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.51 | 0.57 | 0.69 | 0.82 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.62 | 0.69 | 0.82 | 0.99 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.42 | 0.48 | 0.58 | 0.69 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.53 | 0.59 | 0.71 | 0.86 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.52 | 0.58 | 0.70 | 0.84 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.40 | 0.44 | 0.53 | 0.62 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.47 | 0.53 | 0.66 | 0.73 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{AS}/T_{AH}$ | $A_N$ – $D_N$ input to CLK on A – D flip-flops | 0.07/0.12 | 0.09/0.14 | 0.11/0.18 | 0.11/0.20 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | $A_X$ – $D_X$ input to CLK on A – D flip-flops | 0.06/0.19 | 0.07/0.21 | 0.09/0.26 | 0.09/0.31 | ns, Min |
| | $A_X$ – $D_X$ input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08 | 0.66/0.09 | 0.81/0.11 | 0.97/0.12 | ns, Min |
| $T_{CECK\_CLB}/T_{CKCE\_CLB}$ | CE input to CLK on A – D flip-flops | 0.15/0.00 | 0.17/0.00 | 0.21/0.01 | 0.34/–0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | 0.38/0.03 | 0.43/0.04 | 0.53/0.05 | 0.62/0.05 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 0.95 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.53 | 0.59 | 0.71 | 0.83 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.70 | 0.83 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412 | 1286 | 1098 | 1098 | MHz |

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 25:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs | 0.98 | 1.09 | 1.32 | 1.54 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 1.37 | 1.53 | 1.86 | 2.18 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK | 0.54/0.28 | 0.60/0.30 | 0.72/0.35 | 0.96/0.40 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock | 0.27/0.55 | 0.30/0.60 | 0.37/0.70 | 0.43/0.71 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.69/0.18 | 0.77/0.21 | 0.94/0.26 | 1.11/0.29 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock | 0.38/0.10 | 0.43/0.12 | 0.53/0.17 | 0.62/0.13 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK | 0.39/0.10 | 0.44/0.11 | 0.53/0.17 | 0.63/0.12 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_LRAM}$ | Minimum pulse width | 1.05 | 1.13 | 1.25 | 0.82 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 2.10 | 2.26 | 2.50 | 1.64 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 26:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.19 | 1.33 | 1.61 | 1.89 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.58 | 1.77 | 2.15 | 2.53 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 1.12 | 1.23 | 1.46 | 1.68 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS\_SHFREG}/T_{WH\_SHFREG}$ | WE input | 0.37/0.10 | 0.41/0.12 | 0.51/0.17 | 0.59/0.13 | ns, Min |
| $T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$ | CE input to CLK | 0.37/0.10 | 0.42/0.11 | 0.52/0.17 | 0.60/0.12 | ns, Min |
| $T_{DS\_SHFREG}/T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.33/0.34 | 0.37/0.37 | 0.44/0.43 | 0.54/0.47 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.77 | 0.86 | 0.98 | 1.04 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

*Table 34:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

## Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 36:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region) | XC7A100T | 5.14 | 5.74 | 6.72 | 7.64 | ns |
| | | XC7A200T | 5.47 | 6.11 | 7.16 | 8.10 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 37:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region) | XC7A100T | 5.38 | 6.01 | 7.02 | 7.96 | ns |
| | | XC7A200T | 6.17 | 6.89 | 8.05 | 9.05 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 38:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM. | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM | XC7A100T | 0.89 | 0.94 | 0.96 | 1.81 | ns |
| | | XC7A200T | 0.90 | 0.97 | 1.01 | 1.86 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 41:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7A100T | 2.69/–0.46 | 2.89/–0.46 | 3.34/–0.46 | 5.66/–0.52 | ns |
| | | XC7A200T | 3.03/–0.50 | 3.27/–0.50 | 3.79/–0.50 | 6.66/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

*Table 42:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7A100T | 2.44/–0.62 | 2.80/–0.62 | 3.36/–0.62 | 2.15/–0.49 | ns |
| | | XC7A200T | 2.57/–0.63 | 2.94/–0.63 | 3.52/–0.63 | 2.32/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 43:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7A100T | 2.78/–0.32 | 3.15/–0.32 | 3.78/–0.32 | 2.47/–0.60 | ns |
| | | XC7A200T | 2.91/–0.33 | 3.29/–0.33 | 3.94/–0.33 | 2.64/–0.63 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

# GTP Transceiver Specifications

## GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

*Table 47:* **GTP Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | | 1/2 $V_{MGTAVTT}$ | | | mV |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages) | | – | – | 10 | ps |
| | Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages) | | – | – | 12 | ps |
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 150 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | –200 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG482: *7 Series FPGAs GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

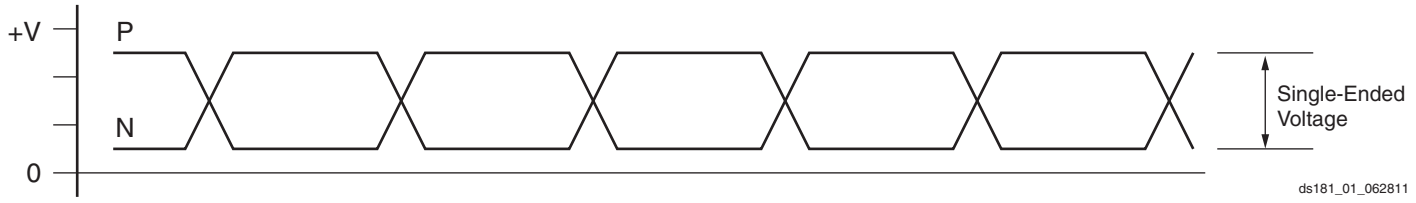


*Figure 1:* **Single-Ended Peak-to-Peak Voltage**

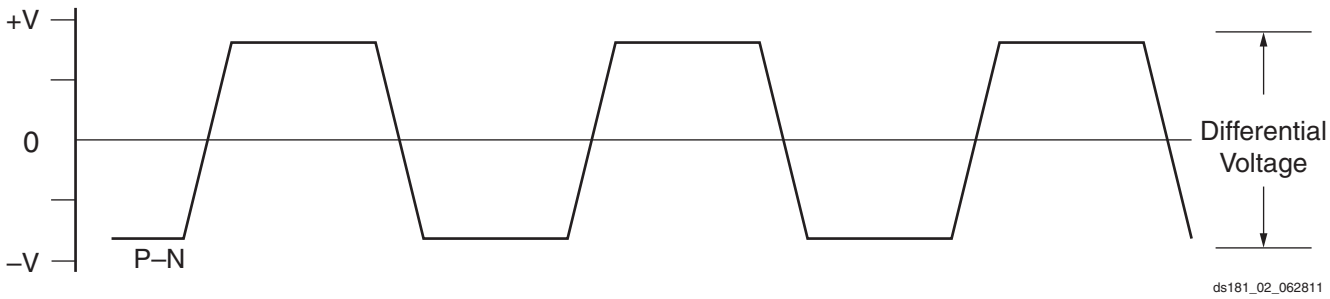


*Figure 2:* **Differential Peak-to-Peak Voltage**

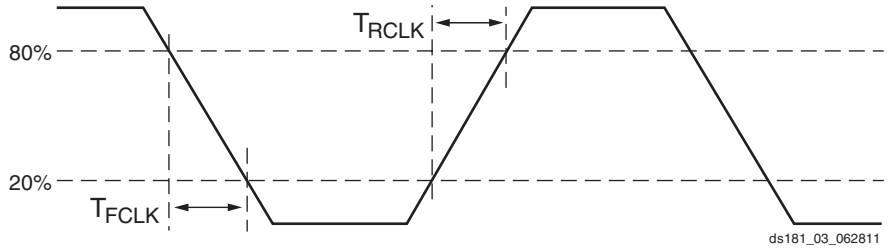


*Figure 3:* **Reference Clock Timing Parameters**

*Table 52:* **GTP Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time. | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | $2.3 \times 10^6$ | UI |

*Table 53:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

## GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the UG482: *7 Series FPGAs GTP Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

*Table 56:* **Gigabit Ethernet Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **Gigabit Ethernet Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| **Gigabit Ethernet Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

*Table 57:* **XAUI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **XAUI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| **XAUI Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

*Table 58:* **PCI Express Protocol Characteristics(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **PCI Express Transmitter Jitter Generation** | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI |
| **PCI Express Receiver High Frequency Jitter Tolerance** | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI |
| PCI Express Gen 2(2) | Receiver inherent timing error | 5000 | 0.40 | – | UI |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI |

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

*Table 59:* **CEI-6G Protocol Characteristics**

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|---|---|---|---|---|
| **CEI-6G Transmitter Jitter Generation** | | | | | |
| Total transmitter jitter(1) | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| **CEI-6G Receiver High Frequency Jitter Tolerance** | | | | | |
| Total receiver jitter tolerance(1) | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

*Table 60:* **CPRI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **CPRI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| **CPRI Receiver Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2(1) | 0.60 | – | UI |
| | 6144.0(1) | 0.60 | – | UI |

**Notes:**

1. Tested to CEI-6G-SR.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 61:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK2}$ | User clock 2 maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

*Table 63:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Internal Configuration Access Port** | | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{CCO}$ | DOUT clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | D[31:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B setup/hold | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 7.00 | 7.00 | 7.00 | 8.00 | ns, Max |
| $T_{SMCO}$ | D[31:00] clock to out in readback | 8.00 | 8.00 | 8.00 | 10.00 | ns, Max |
| $F_{RBCCK}$ | Readback frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI setup/hold | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output | 7.00 | 7.00 | 7.00 | 8.50 | ns, Max |
| $F_{TCK}$ | TCK frequency | 66.00 | 66.00 | 66.00 | 50.00 | MHz, Max |
| **BPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{BPICCO}$ (2) | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | 8.50 | 8.50 | 8.50 | 10.00 | ns, Max |
| $T_{BPIDCC}/T_{BPICCD}$ | D[15:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| **SPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{SPIDCC}/T_{SPICCD}$ | D[03:00] setup/hold | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | ns, Min |
| $T_{SPICCM}$ | MOSI clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

*Table 64:* **eFUSE Programming Conditions** (1)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $t_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.