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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	16825
Number of Logic Elements/Cells	215360
Total RAM Bits	13455360
Number of I/O	285
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a200t-l2fbg484e

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system consult [UG483](#), 7 Series FPGAs PCB Design and Pin Planning Guide.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
8. Each voltage listed requires the filter circuit described in [UG482](#): 7 Series FPGAs GTP Transceiver User Guide.
9. Voltages are specified for the temperature range of $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	μA
$C_{IN}^{(2)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 3.3\text{V}$	90	–	330	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 2.5\text{V}$	68	–	250	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.8\text{V}$	34	–	220	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.5\text{V}$	23	–	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.2\text{V}$	12	–	120	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3\text{V}$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8\text{V}$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
$I_{BATT}^{(3)}$	Battery supply current	–	–	150	nA
$R_{IN_TERM}^{(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices	44	60	83	Ω

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.10	-0.10
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.7	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.10	-0.10
PCI33_3	-0.500	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.50	-0.50
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.00	-13.00
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.90	-8.90
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.00	-13.00
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.90	-8.90
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.00	-8.00
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.40	-13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see [UG471](#): 7 Series FPGAs SelectIO Resources User Guide.

LVDS DC Specifications (LVDS_25)

See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information on the LVDS_25 standard in the HR I/O banks.

Table 11: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in v1.07 from the 14.4/2012.4 device pack for ISE® Design Suite 14.4 and Vivado® Design Suite 2012.4 for the -3, -2, -2L (1.0V), and -1 speed grades and v1.05 from the 14.4/2012.4 device pack for the -2L (0.9V) speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 12](#) correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: Artix-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-2L (0.9V)		-3, -2, -2L (1.0V), -1
XC7A200T	-2L (0.9V)		-3, -2, -2L (1.0V), -1

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 13](#) lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: Artix-7 Device Production Software and Speed Specification Release

Device	Speed Grade		
	1.0V		0.9V
	-3	-2/-2L	-1
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07		

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 9](#).

Table 14: Networking Applications Interface Performances

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽¹⁾⁽²⁾

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_II_F	0.65	0.73	0.80	0.85	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
HSTL_I_18_F	0.67	0.75	0.82	0.87	1.13	1.26	1.51	1.72	1.70	1.92	2.34	2.37	ns
HSTL_II_18_F	0.66	0.75	0.81	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.85	1.18	1.30	1.56	1.77	1.75	1.96	2.39	2.42	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.85	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
LVC MOS33_S4	1.26	1.34	1.41	1.62	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVC MOS33_S8	1.26	1.34	1.41	1.62	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVC MOS33_S12	1.26	1.34	1.41	1.62	3.09	3.21	3.46	3.69	3.65	3.87	4.29	4.34	ns
LVC MOS33_S16	1.26	1.34	1.41	1.62	3.40	3.52	3.77	4.00	3.97	4.18	4.60	4.65	ns
LVC MOS33_F4	1.26	1.34	1.41	1.62	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVC MOS33_F8	1.26	1.34	1.41	1.62	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS33_F12	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS33_F16	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS25_S4	1.12	1.20	1.27	1.43	3.13	3.26	3.51	3.72	3.70	3.91	4.34	4.37	ns
LVC MOS25_S8	1.12	1.20	1.27	1.43	2.88	3.01	3.26	3.49	3.45	3.67	4.09	4.14	ns
LVC MOS25_S12	1.12	1.20	1.27	1.43	2.48	2.60	2.85	3.08	3.05	3.26	3.68	3.73	ns
LVC MOS25_S16	1.12	1.20	1.27	1.43	2.82	2.94	3.20	3.43	3.39	3.60	4.03	4.08	ns
LVC MOS25_F4	1.12	1.20	1.27	1.43	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS25_F8	1.12	1.20	1.27	1.43	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS25_F12	1.12	1.20	1.27	1.43	2.16	2.29	2.54	2.77	2.73	2.95	3.37	3.42	ns
LVC MOS25_F16	1.12	1.20	1.27	1.43	2.01	2.13	2.39	2.61	2.58	2.79	3.21	3.26	ns
LVC MOS18_S4	0.74	0.83	0.89	0.94	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
LVC MOS18_S8	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S12	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S16	0.74	0.83	0.89	0.94	1.52	1.65	1.90	2.13	2.09	2.31	2.73	2.78	ns
LVC MOS18_S24	0.74	0.83	0.89	0.94	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVC MOS18_F4	0.74	0.83	0.89	0.94	1.45	1.57	1.82	2.05	2.01	2.23	2.65	2.70	ns
LVC MOS18_F8	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F12	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F16	0.74	0.83	0.89	0.94	1.40	1.52	1.77	2.00	1.97	2.18	2.60	2.65	ns
LVC MOS18_F24	0.74	0.83	0.89	0.94	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVC MOS15_S4	0.77	0.86	0.93	0.98	2.05	2.18	2.43	2.50	2.62	2.84	3.26	3.15	ns
LVC MOS15_S8	0.77	0.86	0.93	0.98	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVC MOS15_S12	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns
LVC MOS15_S16	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns

Input/Output Logic Switching Characteristics

Table 18: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.40/−0.07	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/−0.35	ns
T _{IDOCK} /T _{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
T _{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T _{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.68	ns, Min

Table 19: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/−0.11	0.71/−0.11	0.84/−0.11	0.60/−0.18	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/−0.10	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/−0.25	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/−0.14	0.73/−0.14	0.89/−0.14	0.60/−0.18	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/−0.10	ns
Combinatorial						
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
T _{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
T _{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.68	ns, Min

DSP48E1 Switching Characteristics

Table 28: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.25/ 0.25	0.32/ 0.27	0.42/ 0.27	0.54/ 0.23	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A,B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B} input to M register CLK using multiplier	2.40/ −0.01	2.76/ −0.01	3.29/ −0.01	4.31/ −0.07	ns
T _{DSPDCK_{A,B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.29/ −0.02	1.48/ −0.02	1.76/ −0.02	2.29/ −0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A,B}_PREG_MULT} / T _{DSPCKD_{A,B}_PREG_MULT}	{A, B} input to P register CLK using multiplier	4.02/ −0.28	4.60/ −0.28	5.48/ −0.28	6.95/ −0.48	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.93/ −0.73	4.50/ −0.73	5.35/ −0.73	6.73/ −1.68	ns
T _{DSPDCK_{A,B}_PREG} / T _{DSPCKD_{A,B}_PREG}	A or B input to P register CLK not using multiplier	1.73/ −0.28	1.98/ −0.28	2.35/ −0.28	2.80/ −0.48	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.54/ −0.26	1.76/ −0.26	2.10/ −0.26	2.54/ −0.45	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.32/ −0.15	1.51/ −0.15	1.80/ −0.15	2.13/ −0.25	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.36/ −0.03	0.43/ −0.03	0.52/ −0.03	0.68/ 0.14	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Clock Buffers and Networks

Table 29: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCKCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCCCK_S}/T_{BCKCK_S}^{(1)}$	S pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCKKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.10	0.14	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	394.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCKCK_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKKO_O} values.

Table 30: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.11	1.26	1.54	1.56	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 31: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.76	0.99	1.24	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.34	0.39	0.52	0.72	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.81	0.85	1.09	0.96	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 32: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{\text{BHCKO_O}}$	BUFH delay from I to O	0.10	0.11	0.13	0.16	ns
$T_{\text{BHCK_CE}}/T_{\text{BHCK_CE}}$	CE pin setup and hold	0.19/0.13	0.22/0.15	0.28/0.21	0.35/0.08	ns
Maximum Frequency						
$F_{\text{MAX_BUFH}}$	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	394.00	MHz

Table 33: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
$T_{\text{DCD_CLK}}$	Global clock tree duty-cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global clock tree skew ⁽²⁾	XC7A100T	0.27	0.33	0.36	0.48	ns
		XC7A200T	0.40	0.48	0.54	0.69	ns
$T_{\text{DCD_BUFIO}}$	I/O clock tree duty cycle distortion	All	0.14	0.14	0.14	0.14	ns
$T_{\text{BUFIOSKEW}}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
$T_{\text{DCD_BUFR}}$	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 34: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$\text{MMCM_F}_{\text{INMAX}}$	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
$\text{MMCM_F}_{\text{INMIN}}$	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
$\text{MMCM_F}_{\text{INJITTER}}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
$\text{MMCM_F}_{\text{INDUTY}}$	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
$\text{MMCM_F}_{\text{MIN_PSCLK}}$	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
$\text{MMCM_F}_{\text{MAX_PSCLK}}$	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
$\text{MMCM_F}_{\text{VCOMIN}}$	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
$\text{MMCM_F}_{\text{VCOMAX}}$	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz

PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3				
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/−0.46	2.89/−0.46	3.34/−0.46	5.66/−0.52	ns
		XC7A200T	3.03/−0.50	3.27/−0.50	3.79/−0.50	6.66/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

Table 42: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7A100T	2.44/−0.62	2.80/−0.62	3.36/−0.62	2.15/−0.49	ns
		XC7A200T	2.57/−0.63	2.94/−0.63	3.52/−0.63	2.32/−0.53	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7A100T	2.78/−0.32	3.15/−0.32	3.78/−0.32	2.47/−0.60	ns
		XC7A200T	2.91/−0.33	3.29/−0.33	3.94/−0.33	2.64/−0.63	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 47: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		$1/2 V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

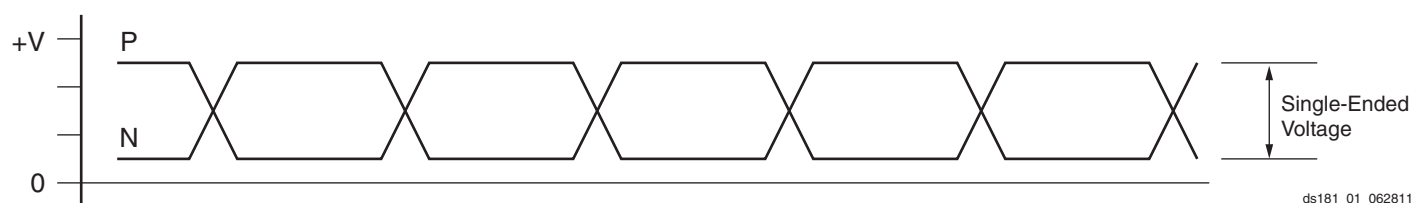


Figure 1: Single-Ended Peak-to-Peak Voltage

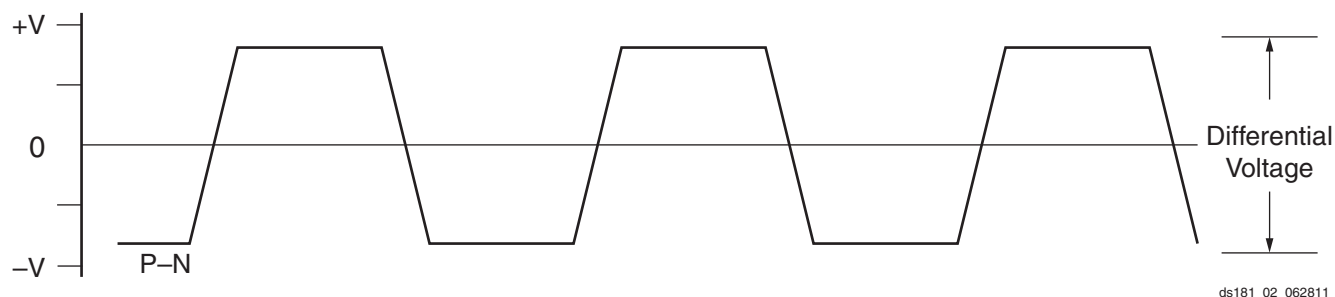


Figure 2: Differential Peak-to-Peak Voltage

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 48: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further information.

Table 49: GTP Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1		-2L		
			Package Type								
			FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	
F _{GTPMAX}	Maximum GTP transceiver data rate		6.6	5.4	6.6	5.4	3.75	3.75	3.75	3.75	Gb/s
F _{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F _{GTPRANGE}	PLL line rate range	1	3.2–6.6		3.2–6.6		3.2–3.75		3.2–3.75		Gb/s
		2	1.6–3.3		1.6–3.3		1.6–3.2		1.6–3.2		Gb/s
		4	0.8–1.65		0.8–1.65		0.8–1.6		0.8–1.6		Gb/s
		8	0.5–0.825		0.5–0.825		0.5–0.8		0.5–0.8		Gb/s
F _{GTPPLL} RANGE	GTP transceiver PLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz

Table 50: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTPDRPCLK}	GTPDRPCLK maximum frequency	175	175	156	125	MHz

Table 51: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range		60	–	660	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	20% – 80%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: CEI-6G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Table 62: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference⁽⁵⁾						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal $V_{REFP} = 1.25\text{V}$ and $V_{REFN} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted. On-chip reference variation is $\pm 1\%$.

Configuration Switching Characteristics

Table 63: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5.00	5.00	5.00	5.00	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Table 63: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCCKD}	D[31:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCCKCS}	CSI_B setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCCK} /T _{SMCCCKW}	RDWR_B setup/hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICCF}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 64: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I _{FS}	V _{CCAUX} supply current	—	—	115	mA
t _j	Temperature range	15	—	125	°C

Notes:

- The FPGA must not be configured during eFUSE programming.