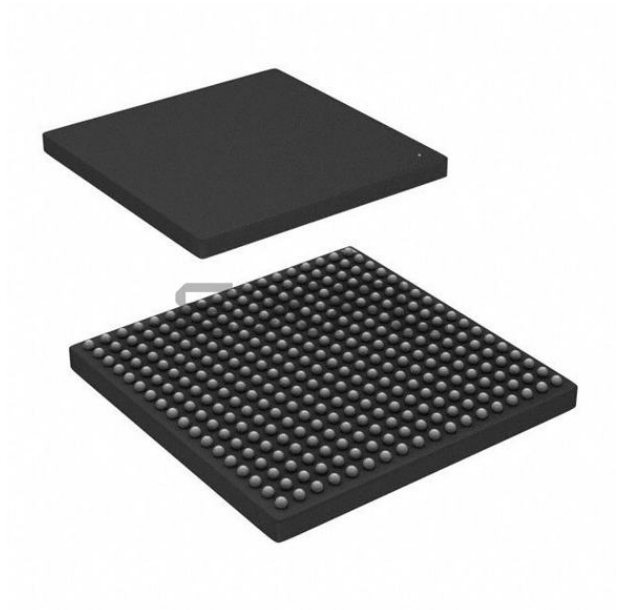

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1825 |
| Number of Logic Elements/Cells | 23360 |
| Total RAM Bits | 1658880 |
| Number of I/O | 150 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 324-LFBGA, CSPBGA |
| Supplier Device Package | 324-CSPBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a25t-l2csg325e |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies (6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies (6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applied to DC signals.
5. For maximum undershoot and overshoot AC specifications, see Table 4.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$ | Internal supply voltage | 0.95 | 1.00 | 1.05 | V |
| | For -2L (0.9V) devices: internal supply voltage | 0.87 | 0.90 | 0.93 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$ | Block RAM supply voltage | 0.95 | 1.00 | 1.05 | V |
| $V_{CCO}$(3)(4) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| $V_{IN}$(5) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage for $V_{REF}$ and differential I/O standards | –0.20 | – | 2.625 | V |
| $I_{IN}$(6) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(7) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTP Transceiver** | | | | | |
| $V_{MGTAVCC}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver circuits | 0.97 | 1.0 | 1.03 | V |
| $V_{MGTAVTT}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. Configuration data is retained even if $V_{CCO}$ drops to 0V.
4. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
8. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.
9. Voltages are specified for the temperature range of $T_j$ = 0°C to +85°C.

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$(2) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$(3) | Battery supply current | – | – | 150 | nA |
| $R_{IN\_TERM}$(4) | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS_25)

See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the LVDS_25 standard in the HR I/O banks.

*Table 11:* **LVDS_25 DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.300 | 1.200 | 1.425 | V |

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in v1.07 from the 14.4/2012.4 device pack for ISE® Design Suite14.4 and Vivado® Design Suite 2012.4 for the -3, -2, -2L (1.0V), and -1 speed grades and v1.05 from the 14.4/2012.4 device pack for the -2L (0.9V) speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

***Advance Product Specification***

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

***Preliminary Product Specification***

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

***Production Product Specification***

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

*Table 12:* **Artix-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7A100T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |
| XC7A200T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 13:* **Artix-7 Device Production Software and Speed Specification Release**

| Device | Speed Grade | | | |
|---|---|---|---|---|
| | 1.0V | | | 0.9V |
| | -3 | -2/-2L | -1 | -2L |
| XC7A100T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |
| XC7A200T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |

**Notes:**
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

*Table 14:* **Networking Applications Interface Performances**

| Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 15:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

| Memory Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| **4:1 Memory Controllers** | | | | | |
| DDR3 | 1066 | 800 | 800 | 800 | Mb/s |
| DDR3L | 800 | 800 | 667 | 667 | Mb/s |
| DDR2 | 800 | 800 | 667 | 667 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 533 | Mb/s |
| **2:1 Memory Controllers** | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | 620 | Mb/s |
| DDR2 | 800 | 700 | 620 | 620 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).

## IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVTTL_S4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.80 | 3.93 | 4.18 | 4.41 | 4.37 | 4.59 | 5.01 | 5.06 | ns |
| LVTTL_S8 | 1.26 | 1.34 | 1.41 | 1.58 | 3.54 | 3.66 | 3.92 | 4.15 | 4.11 | 4.32 | 4.75 | 4.80 | ns |
| LVTTL_S12 | 1.26 | 1.34 | 1.41 | 1.58 | 3.52 | 3.65 | 3.90 | 4.13 | 4.09 | 4.31 | 4.73 | 4.78 | ns |
| LVTTL_S16 | 1.26 | 1.34 | 1.41 | 1.58 | 3.07 | 3.19 | 3.45 | 3.68 | 3.64 | 3.85 | 4.28 | 4.33 | ns |
| LVTTL_S24 | 1.26 | 1.34 | 1.41 | 1.58 | 3.29 | 3.41 | 3.67 | 3.90 | 3.86 | 4.07 | 4.50 | 4.55 | ns |
| LVTTL_F4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.26 | 3.38 | 3.64 | 3.86 | 3.83 | 4.04 | 4.46 | 4.51 | ns |
| LVTTL_F8 | 1.26 | 1.34 | 1.41 | 1.58 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVTTL_F12 | 1.26 | 1.34 | 1.41 | 1.58 | 2.73 | 2.85 | 3.10 | 3.33 | 3.29 | 3.51 | 3.93 | 3.98 | ns |
| LVTTL_F16 | 1.26 | 1.34 | 1.41 | 1.58 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVTTL_F24 | 1.26 | 1.34 | 1.41 | 1.58 | 2.52 | 2.65 | 2.90 | 3.22 | 3.09 | 3.31 | 3.73 | 3.87 | ns |
| LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| MINI_LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| BLVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.84 | 1.96 | 2.21 | 2.44 | 2.40 | 2.62 | 3.04 | 3.09 | ns |
| RSDS_25 (point to point) | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| PPDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.88 | 1.86 | 2.07 | 2.49 | 2.53 | ns |
| TMDS_33 | 0.73 | 0.81 | 0.88 | 0.90 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| PCI33_3 | 1.24 | 1.32 | 1.39 | 1.57 | 3.10 | 3.22 | 3.48 | 3.71 | 3.67 | 3.88 | 4.31 | 4.36 | ns |
| HSUL_12 | 0.67 | 0.75 | 0.82 | 0.87 | 1.80 | 1.93 | 2.18 | 2.41 | 2.37 | 2.59 | 3.01 | 3.06 | ns |
| DIFF_HSUL_12 | 0.68 | 0.76 | 0.83 | 0.88 | 1.80 | 1.93 | 2.18 | 2.21 | 2.37 | 2.59 | 3.01 | 2.86 | ns |
| HSTL_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.62 | 1.74 | 1.99 | 2.19 | 2.19 | 2.40 | 2.82 | 2.84 | ns |
| HSTL_II_S | 0.65 | 0.73 | 0.80 | 0.85 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| HSTL_I_18_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| HSTL_II_18_S | 0.66 | 0.75 | 0.81 | 0.87 | 1.41 | 1.54 | 1.79 | 1.97 | 1.98 | 2.20 | 2.62 | 2.62 | ns |
| DIFF_HSTL_I_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.59 | 1.71 | 1.96 | 2.13 | 2.15 | 2.37 | 2.79 | 2.78 | ns |
| DIFF_HSTL_II_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.51 | 1.63 | 1.88 | 2.07 | 2.08 | 2.29 | 2.71 | 2.72 | ns |
| DIFF_HSTL_I_18_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.96 | 1.95 | 2.17 | 2.59 | 2.61 | ns |
| DIFF_HSTL_II_18_S | 0.70 | 0.78 | 0.85 | 0.87 | 1.46 | 1.58 | 1.84 | 2.00 | 2.03 | 2.24 | 2.67 | 2.65 | ns |
| HSTL_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.10 | 1.22 | 1.48 | 1.69 | 1.67 | 1.88 | 2.31 | 2.34 | ns |

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| HSTL_II_F | 0.65 | 0.73 | 0.80 | 0.85 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| HSTL_I_18_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.13 | 1.26 | 1.51 | 1.72 | 1.70 | 1.92 | 2.34 | 2.37 | ns |
| HSTL_II_18_F | 0.66 | 0.75 | 0.81 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_HSTL_I_F | 0.68 | 0.76 | 0.83 | 0.85 | 1.18 | 1.30 | 1.56 | 1.77 | 1.75 | 1.96 | 2.39 | 2.42 | ns |
| DIFF_HSTL_II_F | 0.68 | 0.76 | 0.83 | 0.85 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| DIFF_HSTL_I_18_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| DIFF_HSTL_II_18_F | 0.70 | 0.78 | 0.85 | 0.87 | 1.21 | 1.33 | 1.59 | 1.77 | 1.78 | 1.99 | 2.42 | 2.42 | ns |
| LVCMOS33_S4 | 1.26 | 1.34 | 1.41 | 1.62 | 3.80 | 3.93 | 4.18 | 4.41 | 4.37 | 4.59 | 5.01 | 5.06 | ns |
| LVCMOS33_S8 | 1.26 | 1.34 | 1.41 | 1.62 | 3.52 | 3.65 | 3.90 | 4.13 | 4.09 | 4.31 | 4.73 | 4.78 | ns |
| LVCMOS33_S12 | 1.26 | 1.34 | 1.41 | 1.62 | 3.09 | 3.21 | 3.46 | 3.69 | 3.65 | 3.87 | 4.29 | 4.34 | ns |
| LVCMOS33_S16 | 1.26 | 1.34 | 1.41 | 1.62 | 3.40 | 3.52 | 3.77 | 4.00 | 3.97 | 4.18 | 4.60 | 4.65 | ns |
| LVCMOS33_F4 | 1.26 | 1.34 | 1.41 | 1.62 | 3.26 | 3.38 | 3.64 | 3.86 | 3.83 | 4.04 | 4.46 | 4.51 | ns |
| LVCMOS33_F8 | 1.26 | 1.34 | 1.41 | 1.62 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVCMOS33_F12 | 1.26 | 1.34 | 1.41 | 1.62 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVCMOS33_F16 | 1.26 | 1.34 | 1.41 | 1.62 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVCMOS25_S4 | 1.12 | 1.20 | 1.27 | 1.43 | 3.13 | 3.26 | 3.51 | 3.72 | 3.70 | 3.91 | 4.34 | 4.37 | ns |
| LVCMOS25_S8 | 1.12 | 1.20 | 1.27 | 1.43 | 2.88 | 3.01 | 3.26 | 3.49 | 3.45 | 3.67 | 4.09 | 4.14 | ns |
| LVCMOS25_S12 | 1.12 | 1.20 | 1.27 | 1.43 | 2.48 | 2.60 | 2.85 | 3.08 | 3.05 | 3.26 | 3.68 | 3.73 | ns |
| LVCMOS25_S16 | 1.12 | 1.20 | 1.27 | 1.43 | 2.82 | 2.94 | 3.20 | 3.43 | 3.39 | 3.60 | 4.03 | 4.08 | ns |
| LVCMOS25_F4 | 1.12 | 1.20 | 1.27 | 1.43 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVCMOS25_F8 | 1.12 | 1.20 | 1.27 | 1.43 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS25_F12 | 1.12 | 1.20 | 1.27 | 1.43 | 2.16 | 2.29 | 2.54 | 2.77 | 2.73 | 2.95 | 3.37 | 3.42 | ns |
| LVCMOS25_F16 | 1.12 | 1.20 | 1.27 | 1.43 | 2.01 | 2.13 | 2.39 | 2.61 | 2.58 | 2.79 | 3.21 | 3.26 | ns |
| LVCMOS18_S4 | 0.74 | 0.83 | 0.89 | 0.94 | 1.62 | 1.74 | 1.99 | 2.19 | 2.19 | 2.40 | 2.82 | 2.84 | ns |
| LVCMOS18_S8 | 0.74 | 0.83 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS18_S12 | 0.74 | 0.83 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.79 | 2.75 | 2.96 | 3.39 | 3.44 | ns |
| LVCMOS18_S16 | 0.74 | 0.83 | 0.89 | 0.94 | 1.52 | 1.65 | 1.90 | 2.13 | 2.09 | 2.31 | 2.73 | 2.78 | ns |
| LVCMOS18_S24 | 0.74 | 0.83 | 0.89 | 0.94 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS18_F4 | 0.74 | 0.83 | 0.89 | 0.94 | 1.45 | 1.57 | 1.82 | 2.05 | 2.01 | 2.23 | 2.65 | 2.70 | ns |
| LVCMOS18_F8 | 0.74 | 0.83 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.29 | 2.25 | 2.46 | 2.89 | 2.94 | ns |
| LVCMOS18_F12 | 0.74 | 0.83 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.29 | 2.25 | 2.46 | 2.89 | 2.94 | ns |
| LVCMOS18_F16 | 0.74 | 0.83 | 0.89 | 0.94 | 1.40 | 1.52 | 1.77 | 2.00 | 1.97 | 2.18 | 2.60 | 2.65 | ns |
| LVCMOS18_F24 | 0.74 | 0.83 | 0.89 | 0.94 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS15_S4 | 0.77 | 0.86 | 0.93 | 0.98 | 2.05 | 2.18 | 2.43 | 2.50 | 2.62 | 2.84 | 3.26 | 3.15 | ns |
| LVCMOS15_S8 | 0.77 | 0.86 | 0.93 | 0.98 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS15_S12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 2.19 | 2.15 | 2.37 | 2.79 | 2.84 | ns |
| LVCMOS15_S16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 2.19 | 2.15 | 2.37 | 2.79 | 2.84 | ns |

## Output Serializer/Deserializer Switching Characteristics

*Table 21:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.44/–0.25 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.60/–0.25 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.46/–0.25 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.15 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.70 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.54 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| **Combinatorial** | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.83 | 0.92 | 1.11 | 1.18 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

*Table 27:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.32/0.42 | 0.34/0.43 | 0.36/0.46 | 0.40/0.47 | ns, Min |
| $T_{RCCK\_WEA}/T_{RCKC\_WEA}$ | Write enable (WE) input (block RAM only) | 0.44/0.18 | 0.48/0.19 | 0.54/0.20 | 0.64/0.23 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.46/0.30 | 0.46/0.35 | 0.47/0.43 | 0.77/0.44 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.42/0.30 | 0.43/0.35 | 0.43/0.43 | 0.71/0.44 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.90 | 0.98 | 1.10 | 1.25 | ns, Max |
| $T_{RREC\_RST}/T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.87/–0.81 | 2.07/–0.81 | 2.37/–0.81 | 2.44/–0.71 | ns, Max |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses | 447.63 | 404.53 | 339.67 | 268.96 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 405.35 | 362.19 | 297.35 | 226.60 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 410.34 | 365.10 | 297.53 | 215.38 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 28:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.26/ 0.12 | 0.30/ 0.13 | 0.37/ 0.14 | 0.45/ 0.14 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.33/ 0.15 | 0.38/ 0.16 | 0.45/ 0.18 | 0.60/ 0.19 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.17/ 0.17 | 0.20/ 0.19 | 0.24/ 0.21 | 0.34/ 0.29 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.25/ 0.25 | 0.32/ 0.27 | 0.42/ 0.27 | 0.54/ 0.23 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.23/ 0.12 | 0.27/ 0.13 | 0.32/ 0.14 | 0.36/ 0.14 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.25/ 0.15 | 0.29/ 0.16 | 0.36/ 0.18 | 0.41/ 0.19 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/ –0.01 | 2.76/ –0.01 | 3.29/ –0.01 | 4.31/ –0.07 | ns |
| $T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$ | {A, D} input to AD register CLK | 1.29/ –0.02 | 1.48/ –0.02 | 1.76/ –0.02 | 2.29/ –0.27 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/ –0.28 | 4.60/ –0.28 | 5.48/ –0.28 | 6.95/ –0.48 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.93/ –0.73 | 4.50/ –0.73 | 5.35/ –0.73 | 6.73/ –1.68 | ns |
| $T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/ –0.28 | 1.98/ –0.28 | 2.35/ –0.28 | 2.80/ –0.48 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.54/ –0.26 | 1.76/ –0.26 | 2.10/ –0.26 | 2.54/ –0.45 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.32/ –0.15 | 1.51/ –0.15 | 1.80/ –0.15 | 2.13/ –0.25 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/ 0.06 | 0.42/ 0.08 | 0.52/ 0.11 | 0.64/ 0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.28/ 0.10 | 0.34/ 0.11 | 0.42/ 0.13 | 0.49/ 0.16 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.36/ –0.03 | 0.43/ –0.03 | 0.52/ –0.03 | 0.68/ 0.14 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.17/ 0.18 | 0.21/ 0.20 | 0.27/ 0.23 | 0.45/ 0.29 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.36/ 0.01 | 0.43/ 0.01 | 0.53/ 0.01 | 0.63/ 0.00 | ns |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.73 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 3.12 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 4.60 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.99 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 6.84 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.65 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.81 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 6.77 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 1.02 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 7.24 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 3.04 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 7.17 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 3.20 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 363.77 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 310.08 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 210.44 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 191.28 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 150.13 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 140.10 | MHz |

*Table 32:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| $T_{BHCCK\_CE}/T_{BHCKC\_CE}$ | CE pin setup and hold | 0.19/0.13 | 0.22/0.15 | 0.28/0.21 | 0.35/0.08 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 394.00 | MHz |

*Table 33:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $T_{DCD\_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7A100T | 0.27 | 0.33 | 0.36 | 0.48 | ns |
| | | XC7A200T | 0.40 | 0.48 | 0.54 | 0.69 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

*Table 34:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| MMCM_$F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| MMCM_$F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| MMCM_$F_{MIN_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_$F_{MAX_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| MMCM_$F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |

*Table 34:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

*Table 39:* **Clock-Capable Clock Input to Output Delay With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL. | | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL | XC7A100T | 0.70 | 0.70 | 0.70 | 1.41 | ns |
| | | XC7A200T | 0.69 | 0.69 | 0.69 | 1.47 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 40:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO. | | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock | 5.01 | 5.61 | 6.64 | 7.34 | ns |

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 41:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7A100T | 2.69/–0.46 | 2.89/–0.46 | 3.34/–0.46 | 5.66/–0.52 | ns |
| | | XC7A200T | 3.03/–0.50 | 3.27/–0.50 | 3.79/–0.50 | 6.66/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

*Table 42:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7A100T | 2.44/–0.62 | 2.80/–0.62 | 3.36/–0.62 | 2.15/–0.49 | ns |
| | | XC7A200T | 2.57/–0.63 | 2.94/–0.63 | 3.52/–0.63 | 2.32/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 43:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7A100T | 2.78/–0.32 | 3.15/–0.32 | 3.78/–0.32 | 2.47/–0.60 | ns |
| | | XC7A200T | 2.91/–0.33 | 3.29/–0.33 | 3.94/–0.33 | 2.64/–0.63 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 44:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.31 | –0.38/1.46 | –0.38/1.76 | –0.16/1.89 | ns |

*Table 45:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

*Table 46:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7A100T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |
| | | XC7A200T | SBG484 | 111 | ps |
| | | | FBG484 | 109 | ps |
| | | | FBG676 | 121 | ps |
| | | | FFG1156 | 151 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

*Table 48:* **GTP Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTP Transceiver Switching Characteristics

Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further information.

*Table 49:* **GTP Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | | | 0.9V | | |
| | | | -3 | | -2/-2L | | -1 | | -2L | | |
| | | | Package Type | | | | | | | | |
| | | | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | | 6.6 | 5.4 | 6.6 | 5.4 | 3.75 | 3.75 | 3.75 | 3.75 | Gb/s |
| $F_{GTPMIN}$ | Minimum GTP transceiver data rate | | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTPRANGE}$ | PLL line rate range | 1 | 3.2–6.6 | | 3.2–6.6 | | 3.2–3.75 | | 3.2–3.75 | | Gb/s |
| | | 2 | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.2 | | 1.6–3.2 | | Gb/s |
| | | 4 | 0.8–1.65 | | 0.8–1.65 | | 0.8–1.6 | | 0.8–1.6 | | Gb/s |
| | | 8 | 0.5–0.825 | | 0.5–0.825 | | 0.5–0.8 | | 0.5–0.8 | | Gb/s |
| $F_{GTPPLLRANGE}$ | GTP transceiver PLL frequency range | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | GHz |

*Table 50:* **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 175 | 175 | 156 | 125 | MHz |

*Table 51:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 660 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 20% – 80% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | – | 60 | % |

*Table 54:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 50 | – | ps |
| $T_{FTX}$ | TX fall time | 20%–80% | – | 50 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{6.6}$ | Total Jitter(2)(3) | 6.6 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.6}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.2}$ | Total Jitter(2)(3) | 3.20 Gb/s(4) | – | – | 0.2 | UI |
| $DJ_{3.2}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.2L}$ | Total Jitter(2)(3) | 3.20 Gb/s(5) | – | – | 0.32 | UI |
| $DJ_{3.2L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(6) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(7) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total Jitter(2)(3) | 500 Mb/s | – | – | 0.1 | UI |
| $DJ_{500}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

*Table 55:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 5000 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | | –1250 | – | 1250 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT\_SJ_{6.6}$ | Sinusoidal Jitter(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{5.0}$ | Sinusoidal Jitter(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{4.25}$ | Sinusoidal Jitter(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.75}$ | Sinusoidal Jitter(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.2}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $JT\_SJ_{3.2L}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| $JT\_SJ_{500}$ | Sinusoidal Jitter(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT\_TJSE_{3.2}$ | Total Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $JT\_TJSE_{6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $JT\_SJSE_{3.2}$ | Sinusoidal Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| $JT\_SJSE_{6.6}$ | | 6.6 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.