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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2600
Number of Logic Elements/Cells	33280
Total RAM Bits	1843200
Number of I/O	106
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	238-LFBGA, CSPBGA
Supplier Device Package	238-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7a35t-1cpg236c

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 6 shows the minimum current, in addition to I_{CCQ} , that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: Power-On Current for Artix-7 Devices⁽¹⁾

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
	Typ ⁽²⁾	Typ ⁽²⁾	Typ ⁽²⁾	Typ ⁽²⁾	
XC7A100T	$I_{CCINTQ} + 170$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7A200T	$I_{CCINTQ} + 340$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 80$	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

LVDS DC Specifications (LVDS_25)

See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information on the LVDS_25 standard in the HR I/O banks.

Table 11: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and \bar{Q}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and \bar{Q}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	$R_T = 100 \Omega$ across Q and \bar{Q} signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100 \Omega$ across Q and \bar{Q} signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in v1.07 from the 14.4/2012.4 device pack for ISE® Design Suite 14.4 and Vivado® Design Suite 2012.4 for the -3, -2, -2L (1.0V), and -1 speed grades and v1.05 from the 14.4/2012.4 device pack for the -2L (0.9V) speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 9](#).

Table 14: Networking Applications Interface Performances

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽¹⁾⁽²⁾

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586, 7 Series FPGAs Memory Interface Solutions User Guide](#).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_F4	0.77	0.86	0.93	0.98	1.85	1.97	2.23	2.27	2.42	2.63	3.06	2.92	ns
LVC MOS15_F8	0.77	0.86	0.93	0.98	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVC MOS15_F12	0.77	0.86	0.93	0.98	1.35	1.47	1.73	1.96	1.92	2.13	2.56	2.61	ns
LVC MOS15_F16	0.77	0.86	0.93	0.98	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVC MOS12_S4	0.87	0.95	1.02	1.08	2.57	2.69	2.95	3.18	3.14	3.35	3.78	3.83	ns
LVC MOS12_S8	0.87	0.95	1.02	1.08	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVC MOS12_S12	0.87	0.95	1.02	1.08	1.79	1.91	2.17	2.40	2.36	2.57	2.99	3.05	ns
LVC MOS12_F4	0.87	0.95	1.02	1.08	1.98	2.10	2.35	2.58	2.54	2.76	3.18	3.23	ns
LVC MOS12_F8	0.87	0.95	1.02	1.08	1.54	1.66	1.92	2.15	2.11	2.32	2.75	2.80	ns
LVC MOS12_F12	0.87	0.95	1.02	1.08	1.38	1.51	1.76	1.97	1.95	2.16	2.59	2.62	ns
SSTL135_S	0.67	0.75	0.82	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
SSTL15_S	0.60	0.68	0.75	0.80	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
SSTL18_I_S	0.67	0.75	0.82	0.87	1.67	1.79	2.04	2.24	2.23	2.45	2.87	2.89	ns
SSTL18_II_S	0.67	0.75	0.82	0.87	1.31	1.43	1.68	1.91	1.87	2.09	2.51	2.56	ns
DIFF_SSTL135_S	0.68	0.76	0.83	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
DIFF_SSTL15_S	0.68	0.76	0.83	0.87	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
DIFF_SSTL18_I_S	0.71	0.79	0.86	0.87	1.68	1.80	2.06	2.24	2.25	2.46	2.89	2.89	ns
DIFF_SSTL18_II_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.94	1.95	2.17	2.59	2.59	ns
SSTL135_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
SSTL15_F	0.60	0.68	0.75	0.80	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
SSTL18_I_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.72	1.69	1.90	2.32	2.37	ns
SSTL18_II_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL135_F	0.68	0.76	0.83	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL15_F	0.68	0.76	0.83	0.87	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
DIFF_SSTL18_I_F	0.71	0.79	0.86	0.87	1.23	1.35	1.60	1.80	1.79	2.01	2.43	2.45	ns
DIFF_SSTL18_II_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.79	1.78	1.99	2.42	2.44	ns

Table 17 specifies the values of T_{IOTPHZ} and T_{IOIBUFDISABLE}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{IOIBUFDISABLE} is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 17: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{IOTPHZ}	T input to pad high-impedance	2.06	2.19	2.37	2.19	ns
T _{IOIBUFDISABLE}	IBUF turn-on time from IBUFDISABLE to O output	2.11	2.30	2.60	2.30	ns

Input Serializer/Deserializer Switching Characteristics

Table 20: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCK_BITS_SLIP} / T_{ISCKC_BITS_SLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.14	0.02/0.15	0.02/0.17	0.02/0.21	ns
$T_{ISCK_CE} / T_{ISCKC_CE}^{(2)}$	CE pin setup/hold with respect to CLK (for CE1)	0.45/-0.01	0.50/-0.01	0.72/-0.01	0.35/-0.11	ns
$T_{ISCK_CE2} / T_{ISCKC_CE2}^{(2)}$	CE pin setup/hold with respect to CLKDIV (for CE2)	-0.10/0.33	-0.10/0.36	-0.10/0.40	-0.17/0.40	ns
Setup/Hold for Data Lines						
$T_{ISDCK_D} / T_{ISCKD_D}$	D pin setup/hold with respect to CLK	-0.02/0.12	-0.02/0.14	-0.02/0.17	-0.04/0.19	ns
$T_{ISDCK_DDLY} / T_{ISCKD_DDLY}$	DDLY pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾	-0.02/0.12	-0.02/0.14	-0.02/0.17	-0.03/0.19	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin setup/hold with respect to CLK at DDR mode	-0.02/0.12	-0.02/0.14	-0.02/0.17	-0.04/0.19	ns
$T_{ISDCK_DDLY_DDR} / T_{ISCKD_DDLY_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.12/0.12	0.14/0.14	0.17/0.17	0.19/0.19	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.53	0.54	0.66	0.67	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.11	0.11	0.13	0.14	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCK_CE} / T_{ISCKC_CE}$ in TRACE report.

CLB Switching Characteristics

Table 24: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T _{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T _{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T _{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T _{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T _{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T _{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T _{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T _{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T _{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.20	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.31	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.97/0.12	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.34/–0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.62/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

Block RAM and FIFO Switching Characteristics

Table 27: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.85	2.13	2.46	2.87	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.64	0.74	0.89	1.02	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.77	3.04	3.84	5.30	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.73	0.81	0.94	1.11	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with cascade (without output register) ⁽²⁾	2.61	2.88	3.30	3.76	ns, Max
	Clock CLK to DOUT output with cascade (with output register) ⁽⁴⁾	1.16	1.28	1.46	1.56	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.76	0.87	1.05	1.14	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.94	1.02	1.15	1.30	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	1.10	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	4.90	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	1.05	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.15	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.29	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.45/0.31	0.49/0.33	0.57/0.36	0.77/0.45	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.58/0.60	0.65/0.63	0.74/0.67	0.92/0.76	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.20/0.29	0.22/0.34	0.25/0.41	0.29/0.38	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.50/0.43	0.55/0.46	0.63/0.50	0.78/0.54	ns, Min
T _{RDCK_DI_ECCW} / T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.93/0.43	1.02/0.46	1.17/0.50	1.38/0.48	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	1.04/0.56	1.15/0.59	1.32/0.64	1.55/0.77	ns, Min
T _{RCKC_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	0.92/0.48	ns, Min
T _{RCKC_EN} /T _{RCKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.57/0.26	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.40/0.19	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.41/0.07	ns, Min

DSP48E1 Switching Characteristics

Table 28: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK_A_AREG}/T_{DSPCKD_A_AREG}$	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
$T_{DSPDCK_B_BREG}/T_{DSPCKD_B_BREG}$	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
$T_{DSPDCK_C_CREG}/T_{DSPCKD_C_CREG}$	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
$T_{DSPDCK_D_DREG}/T_{DSPCKD_D_DREG}$	D input to D register CLK	0.25/ 0.25	0.32/ 0.27	0.42/ 0.27	0.54/ 0.23	ns
$T_{DSPDCK_ACIN_AREG}/T_{DSPCKD_ACIN_AREG}$	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
$T_{DSPDCK_BCIN_BREG}/T_{DSPCKD_BCIN_BREG}$	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK_ \{A, B\} _MREG_MULT}/T_{DSPCKD_B_MREG_MULT}$	{A, B} input to M register CLK using multiplier	2.40/ -0.01	2.76/ -0.01	3.29/ -0.01	4.31/ -0.07	ns
$T_{DSPDCK_ \{A, B\} _ADREG}/T_{DSPCKD_D_ADREG}$	{A, D} input to AD register CLK	1.29/ -0.02	1.48/ -0.02	1.76/ -0.02	2.29/ -0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK_ \{A, B\} _PREG_MULT}/T_{DSPCKD_ \{A, B\} _PREG_MULT}$	{A, B} input to P register CLK using multiplier	4.02/ -0.28	4.60/ -0.28	5.48/ -0.28	6.95/ -0.48	ns
$T_{DSPDCK_D_PREG_MULT}/T_{DSPCKD_D_PREG_MULT}$	D input to P register CLK using multiplier	3.93/ -0.73	4.50/ -0.73	5.35/ -0.73	6.73/ -1.68	ns
$T_{DSPDCK_ \{A, B\} _PREG}/T_{DSPCKD_ \{A, B\} _PREG}$	A or B input to P register CLK not using multiplier	1.73/ -0.28	1.98/ -0.28	2.35/ -0.28	2.80/ -0.48	ns
$T_{DSPDCK_C_PREG}/T_{DSPCKD_C_PREG}$	C input to P register CLK not using multiplier	1.54/ -0.26	1.76/ -0.26	2.10/ -0.26	2.54/ -0.45	ns
$T_{DSPDCK_PCIN_PREG}/T_{DSPCKD_PCIN_PREG}$	PCIN input to P register CLK	1.32/ -0.15	1.51/ -0.15	1.80/ -0.15	2.13/ -0.25	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK_ \{CEA;CEB\} _ \{AREG;BREG\} }/T_{DSPCKD_ \{CEA;CEB\} _ \{AREG;BREG\} }$	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
$T_{DSPDCK_CEC_CREG}/T_{DSPCKD_CEC_CREG}$	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
$T_{DSPDCK_CED_DREG}/T_{DSPCKD_CED_DREG}$	CED input to D register CLK	0.36/ -0.03	0.43/ -0.03	0.52/ -0.03	0.68/ 0.14	ns
$T_{DSPDCK_CEM_MREG}/T_{DSPCKD_CEM_MREG}$	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
$T_{DSPDCK_CEP_PREG}/T_{DSPCKD_CEP_PREG}$	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Table 28: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO_P_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
$T_{DSPCKO_CARRYCASCOUT_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
$T_{DSPCKO_P_ADREG_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
$T_{DSPCKO_CARRYCASCOUT_ADREG_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO_P_AREG_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
$T_{DSPCKO_P_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
$T_{DSPCKO_P_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
$T_{DSPCKO_P_DREG_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO_ACOUT; BCOUT}_{AREG; BREG}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
$T_{DSPCKO_CARRYCASCOUT}_{AREG, BREG}_{MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
$T_{DSPCKO_CARRYCASCOUT_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
$T_{DSPCKO_CARRYCASCOUT_DREG_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
$T_{DSPCKO_CARRYCASCOUT_CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	363.77	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	310.08	MHz
$F_{MAX_MULT_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	210.44	MHz
$F_{MAX_MULT_NOMREG_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	191.28	MHz
$F_{MAX_PREADD_MULT_NOADREG}$	Without ADREG	397.30	346.26	290.44	223.26	MHz
$F_{MAX_PREADD_MULT_NOADREG_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	223.26	MHz
$F_{MAX_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	150.13	MHz
$F_{MAX_NOPIPELINEREG_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	140.10	MHz

Clock Buffers and Networks

Table 29: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.17	ns
$T_{BCCCKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.10	0.14	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	394.00	MHz

Notes:

- T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- T_{BCCCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCCKO_O} values.

Table 30: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.11	1.26	1.54	1.56	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 31: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.76	0.99	1.24	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.34	0.39	0.52	0.72	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.81	0.85	1.09	0.96	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

- The maximum input frequency to the BUFR and BUFRM is the BUFIO F_{MAX} frequency.

PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3				
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCK_DI} / T _{PLLCKD_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 39: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL.							
T _{ICKOFFPLLCC}	Clock-capable clock input and OUTFF with PLL	XC7A100T	0.70	0.70	0.70	1.41	ns
		XC7A200T	0.69	0.69	0.69	1.47	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 40: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
T _{ICKOFCS}	Clock to out of I/O clock	5.01	5.61	6.64	7.34	ns

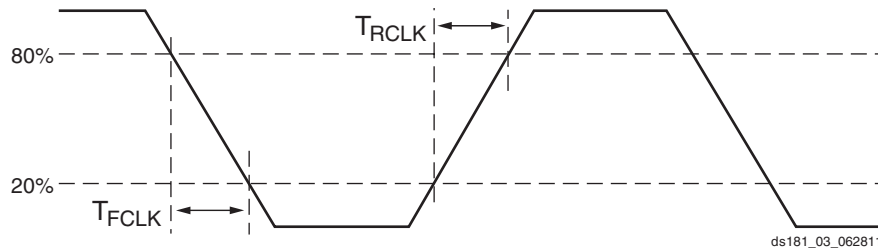


Figure 3: Reference Clock Timing Parameters

Table 52: GTP Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3×10^6	UI

Table 53: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{TXOUT}	TXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz

Notes:

1. Clocking must be implemented as described in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#).

Table 55: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTPMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	5000	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance⁽²⁾						
JT_SJ _{6.6}	Sinusoidal Jitter ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter.

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 ⁽¹⁾	0.60	–	UI
	6144.0 ⁽¹⁾	0.60	–	UI

Notes:

- 1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Table 62: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference⁽⁵⁾						
External Reference	V _{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V _{REFP} pin to AGND, T _j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
4. See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 63: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5.00	5.00	5.00	5.00	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Table 63: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCKD}	D[31:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCCK} /T _{SMCCKW}	RDWR_B setup/hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCKK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICFC}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 64: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I _{FS}	V _{CCAUX} supply current	–	–	115	mA
t _j	Temperature range	15	–	125	°C

Notes:

- The FPGA must not be configured during eFUSE programming.

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