# AMD Xilinx - XC7A50T-1CSG324C Datasheet


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4075 |
| Number of Logic Elements/Cells | 52160 |
| Total RAM Bits | 2764800 |
| Number of I/O | 210 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 324-LFBGA, CSPBGA |
| Supplier Device Package | 324-CSPBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a50t-1csg324c |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies (6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies (6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applied to DC signals.
5. For maximum undershoot and overshoot AC specifications, see Table 4.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$ | Internal supply voltage | 0.95 | 1.00 | 1.05 | V |
| | For -2L (0.9V) devices: internal supply voltage | 0.87 | 0.90 | 0.93 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$ | Block RAM supply voltage | 0.95 | 1.00 | 1.05 | V |
| $V_{CCO}$(3)(4) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| $V_{IN}$(5) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage for $V_{REF}$ and differential I/O standards | –0.20 | – | 2.625 | V |
| $I_{IN}$(6) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(7) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTP Transceiver** | | | | | |
| $V_{MGTAVCC}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver circuits | 0.97 | 1.0 | 1.03 | V |
| $V_{MGTAVTT}$(8)(9) | Analog supply voltage for the GTP transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. Configuration data is retained even if $V_{CCO}$ drops to 0V.
4. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
8. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.
9. Voltages are specified for the temperature range of $T_j$ = 0°C to +85°C.

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$(2) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$(3) | Battery supply current | – | – | 150 | nA |
| $R_{IN\_TERM}$(4) | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$ and $V_{CCO}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

*Table 12:* **Artix-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7A100T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |
| XC7A200T | -2L (0.9V) | | -3, -2, -2L (1.0V), -1 |

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 13:* **Artix-7 Device Production Software and Speed Specification Release**

| Device | Speed Grade | | | |
|---|---|---|---|---|
| | 1.0V | | | 0.9V |
| | -3 | -2/-2L | -1 | -2L |
| XC7A100T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |
| XC7A200T | ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07 | | | |

**Notes:**
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.98 | 1.85 | 1.97 | 2.23 | 2.27 | 2.42 | 2.63 | 3.06 | 2.92 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.98 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.35 | 1.47 | 1.73 | 1.96 | 1.92 | 2.13 | 2.56 | 2.61 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.08 | 2.57 | 2.69 | 2.95 | 3.18 | 3.14 | 3.35 | 3.78 | 3.83 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.08 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.79 | 1.91 | 2.17 | 2.40 | 2.36 | 2.57 | 2.99 | 3.05 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.08 | 1.98 | 2.10 | 2.35 | 2.58 | 2.54 | 2.76 | 3.18 | 3.23 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.08 | 1.54 | 1.66 | 1.92 | 2.15 | 2.11 | 2.32 | 2.75 | 2.80 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.38 | 1.51 | 1.76 | 1.97 | 1.95 | 2.16 | 2.59 | 2.62 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.80 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.67 | 1.79 | 2.04 | 2.24 | 2.23 | 2.45 | 2.87 | 2.89 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.31 | 1.43 | 1.68 | 1.91 | 1.87 | 2.09 | 2.51 | 2.56 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.68 | 1.80 | 2.06 | 2.24 | 2.25 | 2.46 | 2.89 | 2.89 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.94 | 1.95 | 2.17 | 2.59 | 2.59 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.80 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.72 | 1.69 | 1.90 | 2.32 | 2.37 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.23 | 1.35 | 1.60 | 1.80 | 1.79 | 2.01 | 2.43 | 2.45 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.79 | 1.78 | 1.99 | 2.42 | 2.44 | ns |

Table 17 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 17:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.19 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.30 | ns |

## Input/Output Logic Switching Characteristics

*Table 18:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK | 0.48/0.02 | 0.54/0.02 | 0.76/0.02 | 0.40/–0.07 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin setup/hold with respect to CLK | 0.60/0.01 | 0.70/0.01 | 1.13/0.01 | 0.88/–0.35 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin setup/hold with respect to CLK without Delay | 0.01/0.27 | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY) | 0.02/0.27 | 0.02/0.29 | 0.02/0.33 | 0.01/0.33 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.11 | 0.11 | 0.13 | 0.14 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY) | 0.11 | 0.12 | 0.14 | 0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.41 | 0.44 | 0.51 | 0.54 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) | 0.41 | 0.44 | 0.51 | 0.55 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.53 | 0.57 | 0.66 | 0.71 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out | 0.96 | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum pulse width, SR inputs | 0.61 | 0.72 | 0.72 | 0.68 | ns, Min |

*Table 19:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.67/–0.11 | 0.71/–0.11 | 0.84/–0.11 | 0.60/–0.18 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.10 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.37/0.21 | 0.44/0.21 | 0.80/0.21 | 0.62/–0.25 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.69/–0.14 | 0.73/–0.14 | 0.89/–0.14 | 0.60/–0.18 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.10 | ns |
| **Combinatorial** | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.83 | 0.96 | 1.16 | 1.36 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| $T_{RQ\_OLOGIC}$ | SR pin to OQ/TQ out | 0.72 | 0.80 | 0.95 | 1.12 | ns |
| $T_{GSRQ\_OLOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_OLOGIC}$ | Minimum pulse width, SR inputs | 0.64 | 0.74 | 0.74 | 0.68 | ns, Min |

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 25:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs | 0.98 | 1.09 | 1.32 | 1.54 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 1.37 | 1.53 | 1.86 | 2.18 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK | 0.54/0.28 | 0.60/0.30 | 0.72/0.35 | 0.96/0.40 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock | 0.27/0.55 | 0.30/0.60 | 0.37/0.70 | 0.43/0.71 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.69/0.18 | 0.77/0.21 | 0.94/0.26 | 1.11/0.29 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock | 0.38/0.10 | 0.43/0.12 | 0.53/0.17 | 0.62/0.13 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK | 0.39/0.10 | 0.44/0.11 | 0.53/0.17 | 0.63/0.12 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_LRAM}$ | Minimum pulse width | 1.05 | 1.13 | 1.25 | 0.82 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 2.10 | 2.26 | 2.50 | 1.64 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 26:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.19 | 1.33 | 1.61 | 1.89 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.58 | 1.77 | 2.15 | 2.53 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 1.12 | 1.23 | 1.46 | 1.68 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS\_SHFREG}/T_{WH\_SHFREG}$ | WE input | 0.37/0.10 | 0.41/0.12 | 0.51/0.17 | 0.59/0.13 | ns, Min |
| $T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$ | CE input to CLK | 0.37/0.10 | 0.42/0.11 | 0.52/0.17 | 0.60/0.12 | ns, Min |
| $T_{DS\_SHFREG}/T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.33/0.34 | 0.37/0.37 | 0.44/0.43 | 0.54/0.47 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.77 | 0.86 | 0.98 | 1.04 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

## Block RAM and FIFO Switching Characteristics

*Table 27:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.85 | 2.13 | 2.46 | 2.87 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.64 | 0.74 | 0.89 | 1.02 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.77 | 3.04 | 3.84 | 5.30 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.73 | 0.81 | 0.94 | 1.11 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with cascade (without output register)[2] | 2.61 | 2.88 | 3.30 | 3.76 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register)[4] | 1.16 | 1.28 | 1.46 | 1.56 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.76 | 0.87 | 1.05 | 1.14 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.94 | 1.02 | 1.15 | 1.30 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.78 | 0.85 | 0.94 | 1.10 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register) | 2.56 | 2.81 | 3.55 | 4.90 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.68 | 0.76 | 0.89 | 1.05 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.75 | 0.88 | 1.07 | 1.15 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.84 | 0.93 | 1.08 | 1.29 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$ | ADDR inputs[8] | 0.45/0.31 | 0.49/0.33 | 0.57/0.36 | 0.77/0.45 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9] | 0.58/0.60 | 0.65/0.63 | 0.74/0.67 | 0.92/0.76 | ns, Min |
| $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode[9] | 0.20/0.29 | 0.22/0.34 | 0.25/0.41 | 0.29/0.38 | ns, Min |
| $T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.50/0.43 | 0.55/0.46 | 0.63/0.50 | 0.78/0.54 | ns, Min |
| $T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only[9] | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.38/0.48 | ns, Min |
| $T_{RDCK\_DI\_ECC\_FIFO}/T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode[9] | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.55/0.77 | ns, Min |
| $T_{RCCK\_INJECTBITERR}/T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.58/0.35 | 0.64/0.37 | 0.74/0.40 | 0.92/0.48 | ns, Min |
| $T_{RCCK\_EN}/T_{RCKC\_EN}$ | Block RAM enable (EN) input | 0.35/0.20 | 0.39/0.21 | 0.45/0.23 | 0.57/0.26 | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | 0.24/0.15 | 0.29/0.15 | 0.36/0.16 | 0.40/0.19 | ns, Min |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.29/0.07 | 0.32/0.07 | 0.35/0.07 | 0.41/0.07 | ns, Min |

*Table 27:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.32/0.42 | 0.34/0.43 | 0.36/0.46 | 0.40/0.47 | ns, Min |
| $T_{RCCK\_WEA}/T_{RCKC\_WEA}$ | Write enable (WE) input (block RAM only) | 0.44/0.18 | 0.48/0.19 | 0.54/0.20 | 0.64/0.23 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.46/0.30 | 0.46/0.35 | 0.47/0.43 | 0.77/0.44 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.42/0.30 | 0.43/0.35 | 0.43/0.43 | 0.71/0.44 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.90 | 0.98 | 1.10 | 1.25 | ns, Max |
| $T_{RREC\_RST}/T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.87/–0.81 | 2.07/–0.81 | 2.37/–0.81 | 2.44/–0.71 | ns, Max |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses | 447.63 | 404.53 | 339.67 | 268.96 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 405.35 | 362.19 | 297.35 | 226.60 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 410.34 | 365.10 | 297.53 | 215.38 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.73 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 3.12 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 4.60 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.99 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 6.84 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.65 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.81 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 6.77 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 1.02 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 7.24 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 3.04 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 7.17 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 3.20 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 363.77 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 310.08 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 210.44 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 191.28 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 150.13 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 140.10 | MHz |

*Table 34:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

## PLL Switching Characteristics

*Table 35:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $PLL\_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| $PLL\_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| $PLL\_F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| $PLL\_F_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| $PLL\_F_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $PLL\_T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $PLL\_T_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | |
| $PLL\_T_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $PLL\_T_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $PLL\_F_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $PLL\_F_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| $PLL\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| $PLL\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $PLL\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $PLL\_F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| $PLL\_T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| $T_{PLLDCK\_DADDR}$/ $T_{PLLCKD\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DI}/T_{PLLCKD\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DEN}$/ $T_{PLLCKD\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{PLLDCK\_DWE}$/ $T_{PLLCKD\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

*Table 39:* **Clock-Capable Clock Input to Output Delay With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL. | | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL | XC7A100T | 0.70 | 0.70 | 0.70 | 1.41 | ns |
| | | XC7A200T | 0.69 | 0.69 | 0.69 | 1.47 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 40:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO. | | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock | 5.01 | 5.61 | 6.64 | 7.34 | ns |

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 41:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7A100T | 2.69/–0.46 | 2.89/–0.46 | 3.34/–0.46 | 5.66/–0.52 | ns |
| | | XC7A200T | 3.03/–0.50 | 3.27/–0.50 | 3.79/–0.50 | 6.66/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. A zero "0" hold time listing indicates no hold time or a negative hold time.

*Table 42:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7A100T | 2.44/–0.62 | 2.80/–0.62 | 3.36/–0.62 | 2.15/–0.49 | ns |
| | | XC7A200T | 2.57/–0.63 | 2.94/–0.63 | 3.52/–0.63 | 2.32/–0.53 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 43:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7A100T | 2.78/–0.32 | 3.15/–0.32 | 3.78/–0.32 | 2.47/–0.60 | ns |
| | | XC7A200T | 2.91/–0.33 | 3.29/–0.33 | 3.94/–0.33 | 2.64/–0.63 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

*Table 48:* **GTP Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTP Transceiver Switching Characteristics

Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further information.

*Table 49:* **GTP Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | | | 0.9V | | |
| | | | -3 | | -2/-2L | | -1 | | -2L | | |
| | | | Package Type | | | | | | | | |
| | | | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | FFG FBG SBG | FGG FTG CSG | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | | 6.6 | 5.4 | 6.6 | 5.4 | 3.75 | 3.75 | 3.75 | 3.75 | Gb/s |
| $F_{GTPMIN}$ | Minimum GTP transceiver data rate | | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTPRANGE}$ | PLL line rate range | 1 | 3.2–6.6 | | 3.2–6.6 | | 3.2–3.75 | | 3.2–3.75 | | Gb/s |
| | | 2 | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.2 | | 1.6–3.2 | | Gb/s |
| | | 4 | 0.8–1.65 | | 0.8–1.65 | | 0.8–1.6 | | 0.8–1.6 | | Gb/s |
| | | 8 | 0.5–0.825 | | 0.5–0.825 | | 0.5–0.8 | | 0.5–0.8 | | Gb/s |
| $F_{GTPPLLRANGE}$ | GTP transceiver PLL frequency range | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | GHz |

*Table 50:* **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 175 | 175 | 156 | 125 | MHz |

*Table 51:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 660 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 20% – 80% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | – | 60 | % |

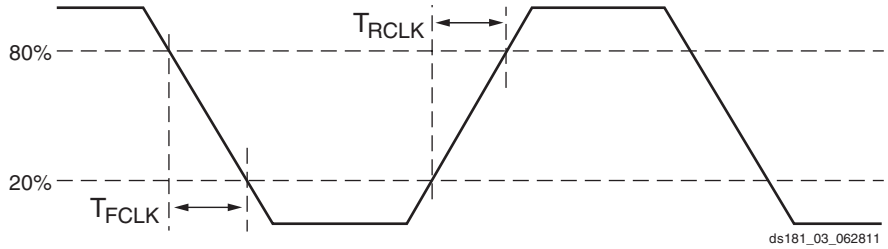


*Figure 3:* **Reference Clock Timing Parameters**

*Table 52:* **GTP Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time. | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | $2.3 \times 10^6$ | UI |

*Table 53:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

# XADC Specifications

*Table 62:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±2 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Unipolar operation | – | – | ±8 | LSBs |
| | | Bipolar operation | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 70 | – | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |

*Table 63:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Internal Configuration Access Port** | | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{CCO}$ | DOUT clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | D[31:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B setup/hold | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 7.00 | 7.00 | 7.00 | 8.00 | ns, Max |
| $T_{SMCO}$ | D[31:00] clock to out in readback | 8.00 | 8.00 | 8.00 | 10.00 | ns, Max |
| $F_{RBCCK}$ | Readback frequency | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI setup/hold | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output | 7.00 | 7.00 | 7.00 | 8.50 | ns, Max |
| $F_{TCK}$ | TCK frequency | 66.00 | 66.00 | 66.00 | 50.00 | MHz, Max |
| **BPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{BPICCO}$ (2) | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | 8.50 | 8.50 | 8.50 | 10.00 | ns, Max |
| $T_{BPIDCC}/T_{BPICCD}$ | D[15:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| **SPI Flash Master Mode Programming Switching** | | | | | | |
| $T_{SPIDCC}/T_{SPICCD}$ | D[03:00] setup/hold | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | ns, Min |
| $T_{SPICCM}$ | MOSI clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

*Table 64:* **eFUSE Programming Conditions** (1)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $t_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description |
|---|---|---|
| 09/26/11 | 1.0 | Initial Xilinx release. |
| 11/07/11 | 1.1 | Revised the $V_{OCM}$ specification in Table 11. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35. In Table 36 through Table 43, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46. |
| 02/13/12 | 1.2 | Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade.<br>Updated summary description on page 1. In Table 2, revised $V_{CCO}$ for the 3.3V HR I/O banks and updated $T_j$. Updated the notes in Table 5. Added MGTAVCC and MGTAVTT power supply ramp times to Table 7. Rearranged Table 8, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10. Revised the specifications in Table 11. Revised $V_{IN}$ in Table 47. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the  table. Revised $F_{TXIN}$ and $F_{RXIN}$ in Table 53. Revised $I_{CCADC}$ and updated Note 1 in Table 62. Revised DDR LVDS transmitter data width in Table 14. Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63. Updated Note 1 in Table 33. |
| 06/01/12 | 1.3 | Reorganized entire data sheet including adding Table 40 and Table 44.<br>Updated $T_{SOL}$ in Table 1. Updated $I_{BATT}$ and added $R_{IN\_TERM}$ to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8, updated many parameters including SSTL135 and SSTL135_R. Removed $V_{OX}$ column and added DIFF_HSUL_12 to Table 10. Updated $V_{OL}$ in Table 11. Updated Table 14 and removed notes 2 and 3. Updated Table 15.<br>Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document.<br>In Table 27, updated Reset Delays section including Note 10 and Note 11. In Table 53, replaced $F_{TXOUT}$ with $F_{GLK}$. Updated many of the XADC specifications in Table 62 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 63 to Table 34 and Table 35. |