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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	5900
Number of Logic Elements/Cells	75520
Total RAM Bits	3870720
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc7a75t-2fgg676c">https://www.e-xfl.com/product-detail/xilinx/xc7a75t-2fgg676c</a>

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a  $V_{CCO}/2$  level.

Table 4:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks<sup>(1)</sup>

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I <sub>CCINTQ</sub>	Quiescent $V_{CCINT}$ supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I <sub>CCOQ</sub>	Quiescent $V_{CCO}$ supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I <sub>CCAUXQ</sub>	Quiescent $V_{CCAUX}$ supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
I <sub>CCBRAMQ</sub>	Quiescent $V_{CCBRAM}$ supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ( $T_j$ ) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_II_F	0.65	0.73	0.80	0.85	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
HSTL_I_18_F	0.67	0.75	0.82	0.87	1.13	1.26	1.51	1.72	1.70	1.92	2.34	2.37	ns
HSTL_II_18_F	0.66	0.75	0.81	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.85	1.18	1.30	1.56	1.77	1.75	1.96	2.39	2.42	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.85	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
LVC MOS33_S4	1.26	1.34	1.41	1.62	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVC MOS33_S8	1.26	1.34	1.41	1.62	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVC MOS33_S12	1.26	1.34	1.41	1.62	3.09	3.21	3.46	3.69	3.65	3.87	4.29	4.34	ns
LVC MOS33_S16	1.26	1.34	1.41	1.62	3.40	3.52	3.77	4.00	3.97	4.18	4.60	4.65	ns
LVC MOS33_F4	1.26	1.34	1.41	1.62	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVC MOS33_F8	1.26	1.34	1.41	1.62	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS33_F12	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS33_F16	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVC MOS25_S4	1.12	1.20	1.27	1.43	3.13	3.26	3.51	3.72	3.70	3.91	4.34	4.37	ns
LVC MOS25_S8	1.12	1.20	1.27	1.43	2.88	3.01	3.26	3.49	3.45	3.67	4.09	4.14	ns
LVC MOS25_S12	1.12	1.20	1.27	1.43	2.48	2.60	2.85	3.08	3.05	3.26	3.68	3.73	ns
LVC MOS25_S16	1.12	1.20	1.27	1.43	2.82	2.94	3.20	3.43	3.39	3.60	4.03	4.08	ns
LVC MOS25_F4	1.12	1.20	1.27	1.43	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVC MOS25_F8	1.12	1.20	1.27	1.43	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS25_F12	1.12	1.20	1.27	1.43	2.16	2.29	2.54	2.77	2.73	2.95	3.37	3.42	ns
LVC MOS25_F16	1.12	1.20	1.27	1.43	2.01	2.13	2.39	2.61	2.58	2.79	3.21	3.26	ns
LVC MOS18_S4	0.74	0.83	0.89	0.94	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
LVC MOS18_S8	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S12	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVC MOS18_S16	0.74	0.83	0.89	0.94	1.52	1.65	1.90	2.13	2.09	2.31	2.73	2.78	ns
LVC MOS18_S24	0.74	0.83	0.89	0.94	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVC MOS18_F4	0.74	0.83	0.89	0.94	1.45	1.57	1.82	2.05	2.01	2.23	2.65	2.70	ns
LVC MOS18_F8	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F12	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVC MOS18_F16	0.74	0.83	0.89	0.94	1.40	1.52	1.77	2.00	1.97	2.18	2.60	2.65	ns
LVC MOS18_F24	0.74	0.83	0.89	0.94	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVC MOS15_S4	0.77	0.86	0.93	0.98	2.05	2.18	2.43	2.50	2.62	2.84	3.26	3.15	ns
LVC MOS15_S8	0.77	0.86	0.93	0.98	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVC MOS15_S12	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns
LVC MOS15_S16	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP0</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_F4	0.77	0.86	0.93	0.98	1.85	1.97	2.23	2.27	2.42	2.63	3.06	2.92	ns
LVC MOS15_F8	0.77	0.86	0.93	0.98	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVC MOS15_F12	0.77	0.86	0.93	0.98	1.35	1.47	1.73	1.96	1.92	2.13	2.56	2.61	ns
LVC MOS15_F16	0.77	0.86	0.93	0.98	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVC MOS12_S4	0.87	0.95	1.02	1.08	2.57	2.69	2.95	3.18	3.14	3.35	3.78	3.83	ns
LVC MOS12_S8	0.87	0.95	1.02	1.08	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVC MOS12_S12	0.87	0.95	1.02	1.08	1.79	1.91	2.17	2.40	2.36	2.57	2.99	3.05	ns
LVC MOS12_F4	0.87	0.95	1.02	1.08	1.98	2.10	2.35	2.58	2.54	2.76	3.18	3.23	ns
LVC MOS12_F8	0.87	0.95	1.02	1.08	1.54	1.66	1.92	2.15	2.11	2.32	2.75	2.80	ns
LVC MOS12_F12	0.87	0.95	1.02	1.08	1.38	1.51	1.76	1.97	1.95	2.16	2.59	2.62	ns
SSTL135_S	0.67	0.75	0.82	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
SSTL15_S	0.60	0.68	0.75	0.80	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
SSTL18_I_S	0.67	0.75	0.82	0.87	1.67	1.79	2.04	2.24	2.23	2.45	2.87	2.89	ns
SSTL18_II_S	0.67	0.75	0.82	0.87	1.31	1.43	1.68	1.91	1.87	2.09	2.51	2.56	ns
DIFF_SSTL135_S	0.68	0.76	0.83	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
DIFF_SSTL15_S	0.68	0.76	0.83	0.87	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
DIFF_SSTL18_I_S	0.71	0.79	0.86	0.87	1.68	1.80	2.06	2.24	2.25	2.46	2.89	2.89	ns
DIFF_SSTL18_II_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.94	1.95	2.17	2.59	2.59	ns
SSTL135_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
SSTL15_F	0.60	0.68	0.75	0.80	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
SSTL18_I_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.72	1.69	1.90	2.32	2.37	ns
SSTL18_II_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL135_F	0.68	0.76	0.83	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL15_F	0.68	0.76	0.83	0.87	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
DIFF_SSTL18_I_F	0.71	0.79	0.86	0.87	1.23	1.35	1.60	1.80	1.79	2.01	2.43	2.45	ns
DIFF_SSTL18_II_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.79	1.78	1.99	2.42	2.44	ns

Table 17 specifies the values of T<sub>IOTPHZ</sub> and T<sub>IOIBUFDISABLE</sub>. T<sub>IOTPHZ</sub> is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T<sub>IOIBUFDISABLE</sub> is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN\_TERM termination turn-off time is always faster than T<sub>IOTPHZ</sub> when the INTERMDISABLE pin is used.

Table 17: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T <sub>IOTPHZ</sub>	T input to pad high-impedance	2.06	2.19	2.37	2.19	ns
T <sub>IOIBUFDISABLE</sub>	IBUF turn-on time from IBUFDISABLE to O output	2.11	2.30	2.60	2.30	ns

## Input/Output Logic Switching Characteristics

Table 18: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold</b>						
$T_{ICE1CK}/T_{ICKCE1}$	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.40/−0.07	ns
$T_{ISRCK}/T_{ICKSR}$	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/−0.35	ns
$T_{IDOCK}/T_{IOCKD}$	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
$T_{IDOCKD}/T_{IOCKDD}$	DDL pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
<b>Combinatorial</b>						
$T_{IDI}$	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
$T_{IDID}$	DDL pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
<b>Sequential Delays</b>						
$T_{IDLO}$	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
$T_{IDLOD}$	DDL pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
$T_{ICKQ}$	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
$T_{RQ\_ILOGIC}$	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
$T_{GSRQ\_ILOGIC}$	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
<b>Set/Reset</b>						
$T_{RPW\_ILOGIC}$	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.68	ns, Min

Table 19: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold</b>						
$T_{ODCK}/T_{OCKD}$	D1/D2 pins setup/hold with respect to CLK	0.67/−0.11	0.71/−0.11	0.84/−0.11	0.60/−0.18	ns
$T_{OOCECK}/T_{OCKOCE}$	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/−0.10	ns
$T_{OSRCK}/T_{OCKSR}$	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/−0.25	ns
$T_{OTCK}/T_{OCKT}$	T1/T2 pins setup/hold with respect to CLK	0.69/−0.14	0.73/−0.14	0.89/−0.14	0.60/−0.18	ns
$T_{OTCECK}/T_{OCKTCE}$	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/−0.10	ns
<b>Combinatorial</b>						
$T_{ODQ}$	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
<b>Sequential Delays</b>						
$T_{OCKQ}$	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
$T_{RQ\_OLOGIC}$	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
$T_{GSRQ\_OLOGIC}$	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
<b>Set/Reset</b>						
$T_{RPW\_OLOGIC}$	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.68	ns, Min

## Output Serializer/Deserializer Switching Characteristics

Table 21: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold</b>						
$T_{OSDCK\_D}/T_{OSCKD\_D}$	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.44/-0.25	ns
$T_{OSDCK\_T}/T_{OSCKD\_T}^{(1)}$	T input setup/hold with respect to CLK	0.69/-0.13	0.73/-0.13	0.88/-0.13	0.60/-0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}^{(1)}$	T input setup/hold with respect to CLKDIV	0.31/-0.13	0.34/-0.13	0.39/-0.13	0.46/-0.25	ns
$T_{OSCKCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.21/-0.15	ns
$T_{OSCKCK\_S}$	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.70	ns
$T_{OSCKCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.22/-0.15	ns
<b>Sequential Delays</b>						
$T_{OSCKO\_OQ}$	Clock to out from CLK to OQ	0.40	0.42	0.48	0.54	ns
$T_{OSCKO\_TQ}$	Clock to out from CLK to TQ	0.47	0.49	0.56	0.63	ns
<b>Combinatorial</b>						
$T_{OSDO\_TTQ}$	T input to TQ Out	0.83	0.92	1.11	1.18	ns

**Notes:**

- $T_{OSDCK\_T2}$  and  $T_{OSCKD\_T2}$  are reported as  $T_{OSDCK\_T}/T_{OSCKD\_T}$  in TRACE report.

Table 27: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCKK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	0.40/0.47	ns, Min
$T_{RCKK\_WEA}/T_{RCKC\_WEA}$	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	0.64/0.23	ns, Min
$T_{RCKK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	0.77/0.44	ns, Min
$T_{RCKK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	0.71/0.44	ns, Min
<b>Reset Delays</b>						
$T_{RCO\_FLAGS}$	Reset RST to FIFO flags/pointers <sup>(10)</sup>	0.90	0.98	1.10	1.25	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing <sup>(11)</sup>	1.87/-0.81	2.07/-0.81	2.37/-0.81	2.44/-0.71	ns, Max
<b>Maximum Frequency</b>						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode	509.68	460.83	388.20	315.66	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B	509.68	460.83	388.20	315.66	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses	447.63	404.53	339.67	268.96	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode	467.07	418.59	345.78	273.30	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled	467.07	418.59	345.78	273.30	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	405.35	362.19	297.35	226.60	MHz
$F_{MAX\_FIFO}$	FIFO in all modes without ECC	509.68	460.83	388.20	315.66	MHz
$F_{MAX\_ECC}$	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	215.38	MHz

**Notes:**

- TRACE will report all of these parameters as  $T_{RCKO\_DO}$ .
- $T_{RCKO\_DOR}$  includes  $T_{RCKO\_DOW}$ ,  $T_{RCKO\_DOPR}$ , and  $T_{RCKO\_DOPW}$  as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with  $DO\_REG = 0$ .
- $T_{RCKO\_DO}$  includes  $T_{RCKO\_DOP}$  as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with  $DO\_REG = 1$ .
- $T_{RCKO\_FLAGS}$  includes the following parameters:  $T_{RCKO\_AEMPTY}$ ,  $T_{RCKO\_AFULL}$ ,  $T_{RCKO\_EMPTY}$ ,  $T_{RCKO\_FULL}$ ,  $T_{RCKO\_RDERR}$ ,  $T_{RCKO\_WRERR}$ .
- $T_{RCKO\_POINTERS}$  includes both  $T_{RCKO\_RDCOUNT}$  and  $T_{RCKO\_WRCOUNT}$ .
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- These parameters include both A and B inputs as well as the parity inputs of A and B.
- $T_{RCO\_FLAGS}$  includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 28: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup and Hold Times of the RST Pins</b>						
$T_{DSPDCK\_RSTA; RSTB\_AREG; BREG} / T_{DSPCKD\_RSTA; RSTB\_AREG; BREG}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{DSPDCK\_RSTC\_CREG} / T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG} / T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{DSPDCK\_RSTM\_MREG} / T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{DSPDCK\_RSTP\_PREG} / T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
<b>Combinatorial Delays from Input Pins to Output Pins</b>						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	2.22	ns
<b>Combinatorial Delays from Input Pins to Cascading Output Pins</b>						
$T_{DSPDO\_A; B\_ACOUT; BCOUT}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{DSPDO\_A; B\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{DSPDO\_A; B\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
<b>Combinatorial Delays from Cascading Input Pins to All Output Pins</b>						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
<b>Clock to Outs from Output Register Clock to Output Pins</b>						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns



Table 32: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T <sub>BHCKO_O</sub>	BUFH delay from I to O	0.10	0.11	0.13	0.16	ns
T <sub>BHCKK_CE</sub> /T <sub>BHCKC_CE</sub>	CE pin setup and hold	0.19/0.13	0.22/0.15	0.28/0.21	0.35/0.08	ns
<b>Maximum Frequency</b>						
F <sub>MAX_BUFH</sub>	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	394.00	MHz

Table 33: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T <sub>DCD_CLK</sub>	Global clock tree duty-cycle distortion <sup>(1)</sup>	All	0.20	0.20	0.20	0.25	ns
T <sub>CKSKEW</sub>	Global clock tree skew <sup>(2)</sup>	XC7A100T	0.27	0.33	0.36	0.48	ns
		XC7A200T	0.40	0.48	0.54	0.69	ns
T <sub>DCD_BUFIO</sub>	I/O clock tree duty cycle distortion	All	0.14	0.14	0.14	0.14	ns
T <sub>BUFIOSKEW</sub>	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
T <sub>DCD_BUFR</sub>	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18	0.18	ns

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T<sub>CKSKEW</sub> value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA\_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

**MMCM Switching Characteristics**

Table 34: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F <sub>INMAX</sub>	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F <sub>INMIN</sub>	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F <sub>INJITTER</sub>	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F <sub>INDUTY</sub>	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
MMCM_F <sub>MIN_PSCLK</sub>	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F <sub>MAX_PSCLK</sub>	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F <sub>VCOMIN</sub>	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F <sub>VCOMAX</sub>	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz

Table 34: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F <sub>BANDWIDTH</sub>	Low MMCM bandwidth at typical <sup>(1)</sup>	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical <sup>(1)</sup>	4.00	4.00	4.00	4.00	MHz
MMCM_T <sub>STATPHAOFFSET</sub>	Static phase offset of the MMCM outputs <sup>(2)</sup>	0.12	0.12	0.12	0.12	ns
MMCM_T <sub>OUTJITTER</sub>	MMCM output jitter	Note 3				
MMCM_T <sub>OUTDUTY</sub>	MMCM output clock duty-cycle precision <sup>(4)</sup>	0.20	0.20	0.20	0.25	ns
MMCM_T <sub>LOCKMAX</sub>	MMCM maximum lock time	100.00	100.00	100.00	100.00	μs
MMCM_F <sub>OUTMAX</sub>	MMCM maximum output frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F <sub>OUTMIN</sub>	MMCM minimum output frequency <sup>(5)(6)</sup>	4.69	4.69	4.69	4.69	MHz
MMCM_T <sub>EXTFDVAR</sub>	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_RST <sub>MINPULSE</sub>	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
MMCM_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	10.00	MHz
MMCM_T <sub>FBDELAY</sub>	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
<b>MMCM Switching Characteristics Setup and Hold</b>						
T <sub>MMCMDCK_PSEN</sub> / T <sub>MMCMCKD_PSEN</sub>	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T <sub>MMCMDCK_PSINCDEC</sub> / T <sub>MMCMCKD_PSINCDEC</sub>	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T <sub>MMCMCKO_PSDONE</sub>	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	0.78	ns
<b>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</b>						
T <sub>MMCMDCK_DADDR</sub> / T <sub>MMCMCKD_DADDR</sub>	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>MMCMDCK_DI</sub> / T <sub>MMCMCKD_DI</sub>	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>MMCMDCK_DEN</sub> / T <sub>MMCMCKD_DEN</sub>	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T <sub>MMCMDCK_DWE</sub> / T <sub>MMCMCKD_DWE</sub>	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>MMCMCKO_DRDY</sub>	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F <sub>DCK</sub>	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.  
See [http://www.xilinx.com/products/intellectual-property/clocking\\_wizard.htm](http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm).
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.
6. When CLKOUT4\_CASCADE = TRUE, MMCM\_F<sub>OUTMIN</sub> is 0.036 MHz.

## PLL Switching Characteristics

Table 35: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F <sub>INMAX</sub>	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F <sub>INMIN</sub>	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
PLL_F <sub>INJITTER</sub>	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F <sub>INDUTY</sub>	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F <sub>VCOMIN</sub>	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F <sub>VCOMAX</sub>	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_F <sub>BANDWIDTH</sub>	Low PLL bandwidth at typical <sup>(1)</sup>	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical <sup>(1)</sup>	4.00	4.00	4.00	4.00	MHz
PLL_T <sub>STATPHAOFFSET</sub>	Static phase offset of the PLL outputs <sup>(2)</sup>	0.12	0.12	0.12	0.12	ns
PLL_T <sub>OUTJITTER</sub>	PLL output jitter	Note 3				
PLL_T <sub>OUTDUTY</sub>	PLL output clock duty-cycle precision <sup>(4)</sup>	0.20	0.20	0.20	0.25	ns
PLL_T <sub>LOCKMAX</sub>	PLL maximum lock time	100.00	100.00	100.00	100.00	μs
PLL_F <sub>OUTMAX</sub>	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F <sub>OUTMIN</sub>	PLL minimum output frequency <sup>(5)</sup>	6.25	6.25	6.25	6.25	MHz
PLL_T <sub>EXTFDVAR</sub>	External clock feedback variation	< 20% of clock input period or 1 ns Max				
PLL_RST <sub>MINPULSE</sub>	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
PLL_T <sub>FBDELAY</sub>	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
<b>Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK</b>						
T <sub>PLLCK_DADDR</sub> / T <sub>PLLCKD_DADDR</sub>	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>PLLCK_DI</sub> / T <sub>PLLCKD_DI</sub>	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>PLLCK_DEN</sub> / T <sub>PLLCKD_DEN</sub>	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T <sub>PLLCK_DWE</sub> / T <sub>PLLCKD_DWE</sub>	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T <sub>PLLCKO_DRDY</sub>	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F <sub>DCK</sub>	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.  
See [http://www.xilinx.com/products/intellectual-property/clocking\\_wizard.htm](http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm).
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

**Table 36: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T <sub>ICKOF</sub>	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7A100T	5.14	5.74	6.72	7.64	ns
		XC7A200T	5.47	6.11	7.16	8.10	ns

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

**Table 37: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T <sub>ICKOFFAR</sub>	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7A100T	5.38	6.01	7.02	7.96	ns
		XC7A200T	6.17	6.89	8.05	9.05	ns

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

**Table 38: Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T <sub>ICKOFMMCMCC</sub>	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7A100T	0.89	0.94	0.96	1.81	ns
		XC7A200T	0.90	0.97	1.01	1.86	ns

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- MMCM output jitter is already included in the timing calculation.

Table 44: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T <sub>PSCS</sub> /T <sub>PHCS</sub>	Setup and hold of I/O clock	-0.38/1.31	-0.38/1.46	-0.38/1.76	-0.16/1.89	ns

Table 45: Sample Window

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T <sub>SAMP</sub>	Sampling error at receiver pins <sup>(1)</sup>	0.59	0.64	0.70	0.70	ns
T <sub>SAMP_BUFIO</sub>	Sampling error at receiver pins using BUFIO <sup>(2)</sup>	0.35	0.40	0.46	0.46	ns

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 MMCM jitter
  - MMCM accuracy (phase offset)
  - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

**Additional Package Parameter Guidelines**

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 46: Package Skew

Symbol	Description	Device	Package	Value	Units
T <sub>PKGSKEW</sub>	Package skew <sup>(1)</sup>	XC7A100T	CSG324	113	ps
			FTG256	120	ps
			FGG484	144	ps
			FGG676	153	ps
		XC7A200T	SBG484	111	ps
			FBG484	109	ps
			FBG676	121	ps
			FFG1156	151	ps

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 48: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V <sub>IDIFF</sub>	Differential peak-to-peak input voltage	350	–	2000	mV
R <sub>IN</sub>	Differential input resistance	–	100	–	Ω
C <sub>EXT</sub>	Required external AC coupling capacitor	–	100	–	nF

### GTP Transceiver Switching Characteristics

Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further information.

Table 49: GTP Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V				0.9V				
			-3		-2/-2L		-1		-2L		
			Package Type								
			FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	
F <sub>GTPMAX</sub>	Maximum GTP transceiver data rate		6.6	5.4	6.6	5.4	3.75	3.75	3.75	3.75	Gb/s
F <sub>GTPMIN</sub>	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F <sub>GTPRANGE</sub>	PLL line rate range	1	3.2–6.6		3.2–6.6		3.2–3.75		3.2–3.75		Gb/s
		2	1.6–3.3		1.6–3.3		1.6–3.2		1.6–3.2		Gb/s
		4	0.8–1.65		0.8–1.65		0.8–1.6		0.8–1.6		Gb/s
		8	0.5–0.825		0.5–0.825		0.5–0.8		0.5–0.8		Gb/s
F <sub>GTPPLL</sub>	GTP transceiver PLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz

Table 50: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
F <sub>GTPDRPCLK</sub>	GTPDRPCLK maximum frequency	175	175	156	125	MHz

Table 51: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F <sub>GCLK</sub>	Reference clock frequency range		60	–	660	MHz
T <sub>RCLK</sub>	Reference clock rise time	20% – 80%	–	200	–	ps
T <sub>FCLK</sub>	Reference clock fall time	20% – 80%	–	200	–	ps
T <sub>DCREF</sub>	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

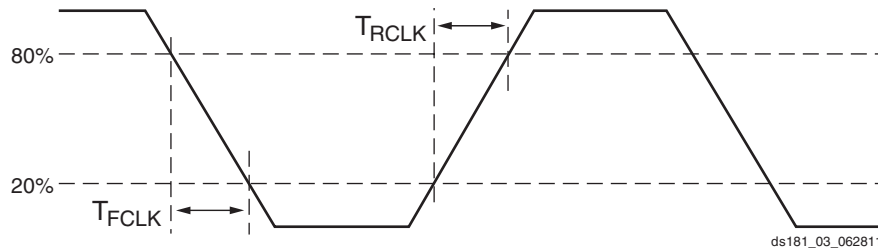


Figure 3: Reference Clock Timing Parameters

Table 52: GTP Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
$T_{LOCK}$	Initial PLL lock		–	–	1	ms
$T_{DLOCK}$	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	$2.3 \times 10^6$	UI

Table 53: GTP Transceiver User Clock Switching Characteristics<sup>(1)</sup>

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
$F_{TXOUT}$	TXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
$F_{RXOUT}$	RXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
$F_{TXIN}$	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
$F_{RXIN}$	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
$F_{TXIN2}$	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
$F_{RXIN2}$	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz

**Notes:**

1. Clocking must be implemented as described in [UG482: 7 Series FPGAs GTP Transceiver User Guide](#).

**Table 54: GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F <sub>GTPTX</sub>	Serial data rate range		0.500	–	F <sub>GTPMAX</sub>	Gb/s
T <sub>RTX</sub>	TX rise time	20%–80%	–	50	–	ps
T <sub>FTX</sub>	TX fall time	20%–80%	–	50	–	ps
T <sub>LLSKEW</sub>	TX lane-to-lane skew <sup>(1)</sup>		–	–	500	ps
V <sub>TXOOBVDPP</sub>	Electrical idle amplitude		–	–	20	mV
T <sub>TXOOBTRANSITION</sub>	Electrical idle transition time		–	–	140	ns
T <sub>J6.6</sub>	Total Jitter <sup>(2)(3)</sup>	6.6 Gb/s	–	–	0.30	UI
D <sub>J6.6</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.15	UI
T <sub>J5.0</sub>	Total Jitter <sup>(2)(3)</sup>	5.0 Gb/s	–	–	0.30	UI
D <sub>J5.0</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.15	UI
T <sub>J4.25</sub>	Total Jitter <sup>(2)(3)</sup>	4.25 Gb/s	–	–	0.30	UI
D <sub>J4.25</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.15	UI
T <sub>J3.75</sub>	Total Jitter <sup>(2)(3)</sup>	3.75 Gb/s	–	–	0.30	UI
D <sub>J3.75</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.15	UI
T <sub>J3.2</sub>	Total Jitter <sup>(2)(3)</sup>	3.20 Gb/s <sup>(4)</sup>	–	–	0.2	UI
D <sub>J3.2</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.1	UI
T <sub>J3.2L</sub>	Total Jitter <sup>(2)(3)</sup>	3.20 Gb/s <sup>(5)</sup>	–	–	0.32	UI
D <sub>J3.2L</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.16	UI
T <sub>J2.5</sub>	Total Jitter <sup>(2)(3)</sup>	2.5 Gb/s <sup>(6)</sup>	–	–	0.20	UI
D <sub>J2.5</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.08	UI
T <sub>J1.25</sub>	Total Jitter <sup>(2)(3)</sup>	1.25 Gb/s <sup>(7)</sup>	–	–	0.15	UI
D <sub>J1.25</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.06	UI
T <sub>J500</sub>	Total Jitter <sup>(2)(3)</sup>	500 Mb/s	–	–	0.1	UI
D <sub>J500</sub>	Deterministic Jitter <sup>(2)(3)</sup>		–	–	0.03	UI

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
- Using PLL[0/1]\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e<sup>-12</sup>.
- PLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- PLL frequency at 1.6 GHz and TXOUT\_DIV = 1.
- PLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- PLL frequency at 2.5 GHz and TXOUT\_DIV = 4.



Table 55: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F <sub>GTPRX</sub>	Serial data rate	RX oversampler not enabled	0.500	–	F <sub>GTPMAX</sub>	Gb/s
T <sub>RXELECIDLE</sub>	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX <sub>OOBVDPP</sub>	OOB detect threshold peak-to-peak		60	–	150	mV
RX <sub>SST</sub>	Receiver spread-spectrum tracking <sup>(1)</sup>	Modulated @ 33 KHz	–5000	–	5000	ppm
RX <sub>RL</sub>	Run length (CID)		–	–	512	UI
RX <sub>PPMTOL</sub>	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
<b>SJ Jitter Tolerance<sup>(2)</sup></b>						
JT_SJ <sub>6.6</sub>	Sinusoidal Jitter <sup>(3)</sup>	6.6 Gb/s	0.44	–	–	UI
JT_SJ <sub>5.0</sub>	Sinusoidal Jitter <sup>(3)</sup>	5.0 Gb/s	0.44	–	–	UI
JT_SJ <sub>4.25</sub>	Sinusoidal Jitter <sup>(3)</sup>	4.25 Gb/s	0.44	–	–	UI
JT_SJ <sub>3.75</sub>	Sinusoidal Jitter <sup>(3)</sup>	3.75 Gb/s	0.44	–	–	UI
JT_SJ <sub>3.2</sub>	Sinusoidal Jitter <sup>(3)</sup>	3.2 Gb/s <sup>(4)</sup>	0.45	–	–	UI
JT_SJ <sub>3.2L</sub>	Sinusoidal Jitter <sup>(3)</sup>	3.2 Gb/s <sup>(5)</sup>	0.45	–	–	UI
JT_SJ <sub>2.5</sub>	Sinusoidal Jitter <sup>(3)</sup>	2.5 Gb/s <sup>(6)</sup>	0.5	–	–	UI
JT_SJ <sub>1.25</sub>	Sinusoidal Jitter <sup>(3)</sup>	1.25 Gb/s <sup>(7)</sup>	0.5	–	–	UI
JT_SJ <sub>500</sub>	Sinusoidal Jitter <sup>(3)</sup>	500 Mb/s	0.4	–	–	UI
<b>SJ Jitter Tolerance with Stressed Eye<sup>(2)</sup></b>						
JT_TJSE <sub>3.2</sub>	Total Jitter with Stressed Eye <sup>(8)</sup>	3.2 Gb/s	0.70	–	–	UI
JT_TJSE <sub>6.6</sub>		6.6 Gb/s	0.70	–	–	UI
JT_SJSE <sub>3.2</sub>	Sinusoidal Jitter with Stressed Eye <sup>(8)</sup>	3.2 Gb/s	0.1	–	–	UI
JT_SJSE <sub>6.6</sub>		6.6 Gb/s	0.1	–	–	UI

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e<sup>-12</sup>.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- PLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- PLL frequency at 1.6 GHz and RXOUT\_DIV = 1.
- PLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- PLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter.

## GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
<b>Gigabit Ethernet Transmitter Jitter Generation</b>				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
<b>Gigabit Ethernet Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
<b>XAUI Transmitter Jitter Generation</b>				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
<b>XAUI Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: PCI Express Protocol Characteristics<sup>(1)</sup>

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
<b>PCI Express Transmitter Jitter Generation</b>					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
<b>PCI Express Receiver High Frequency Jitter Tolerance</b>					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2 <sup>(2)</sup>	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: CEI-6G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
<b>CEI-6G Transmitter Jitter Generation</b>					
Total transmitter jitter <sup>(1)</sup>	4976–6375	CEI-6G-SR	–	0.3	UI
<b>CEI-6G Receiver High Frequency Jitter Tolerance</b>					
Total receiver jitter tolerance <sup>(1)</sup>	4976–6375	CEI-6G-SR	0.6	–	UI

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 60: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
<b>CPRI Transmitter Jitter Generation</b>				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
<b>CPRI Receiver Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2 <sup>(1)</sup>	0.60	–	UI
	6144.0 <sup>(1)</sup>	0.60	–	UI

**Notes:**

1. Tested to CEI-6G-SR.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F <sub>PIPECLK</sub>	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F <sub>USERCLK</sub>	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F <sub>USERCLK2</sub>	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F <sub>DRPCLK</sub>	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Table 62: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
<b>XADC Reference<sup>(5)</sup></b>						
External Reference	V <sub>REFP</sub>	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V <sub>REFP</sub> pin to AGND, T <sub>j</sub> = –40°C to 100°C	1.2375	1.25	1.2625	V

**Notes:**

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal V<sub>REFP</sub> = 1.25V and V<sub>REFN</sub> = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

## Configuration Switching Characteristics

Table 63: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
<b>Power-up Timing Characteristics</b>						
T <sub>PL</sub> <sup>(1)</sup>	Program latency	5.00	5.00	5.00	5.00	ms, Max
T <sub>POR</sub> <sup>(1)</sup>	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T <sub>PROGRAM</sub>	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
<b>CCLK Output (Master Mode)</b>						
T <sub>ICCK</sub>	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T <sub>MCCKL</sub>	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T <sub>MCCKH</sub>	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F <sub>MCCK</sub>	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F <sub>MCCK_START</sub>	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F <sub>MCCKTOL</sub>	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
<b>CCLK Input (Slave Modes)</b>						
T <sub>SCCKL</sub>	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T <sub>SCCKH</sub>	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F <sub>SCCK</sub>	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
<b>EMCCLK Input (Master Mode)</b>						
T <sub>EMCCKL</sub>	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T <sub>EMCCKH</sub>	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F <sub>EMCCK</sub>	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Date	Version	Description
09/20/12	1.4	<p>In <a href="#">Table 1</a>, updated the descriptions, changed <math>V_{IN}</math> and <a href="#">Note 2</a>, and added <a href="#">Note 4</a>. In <a href="#">Table 2</a>, changed descriptions and notes. Updated parameters in <a href="#">Table 3</a>. Added <a href="#">Table 4</a>. Revised the <a href="#">Power-On/Off Power Supply Sequencing</a> section. Updated standards and specifications in <a href="#">Table 8</a>, <a href="#">Table 9</a>, and <a href="#">Table 10</a>. Removed the XC7A350T device from data sheet.</p> <p>Updated the <a href="#">AC Switching Characteristics</a> section to the ISE 14.2 speed specifications throughout the document. Updated the <a href="#">IOB Pad Input/Output/3-State</a> discussion and changed <a href="#">Table 17</a> by adding <math>T_{IOIBUFDISABLE}</math>. Removed many of the combinatorial delay specifications and <math>T_{CINCK}/T_{CKCIN}</math> from <a href="#">Table 24</a>. Changed <math>F_{PFDMAX}</math> conditions in <a href="#">Table 34</a> and <a href="#">Table 35</a>. Updated the <a href="#">GTP Transceiver Specifications</a> section, moved the GTP Transceiver DC characteristics section to the overall <a href="#">DC Characteristics</a> section, and added the <a href="#">GTP Transceiver Protocol Jitter Characteristics</a> section. In <a href="#">Table 62</a>, updated <a href="#">Note 1</a>. In <a href="#">Table 63</a>, updated <math>T_{POR}</math>.</p>
02/01/13	1.5	<p>Updated the <a href="#">AC Switching Characteristics</a> based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to <a href="#">Table 12</a> and <a href="#">Table 13</a> for -3, -2, -2L (1.0V), -1 speed specifications.</p> <p>Revised <math>I_{DCIN}</math> and <math>I_{DCOUT}</math> and added <a href="#">Note 5</a> in <a href="#">Table 1</a>. Added <a href="#">Note 2</a> to <a href="#">Table 2</a>. Updated <a href="#">Table 5</a>. Added minimum current specifications to <a href="#">Table 6</a>. Removed SSTL12 and HSTL_I_12 from <a href="#">Table 8</a>. Removed DIFF_SSTL12 from <a href="#">Table 10</a>. Updated <a href="#">Table 12</a>. Added a 2:1 memory controller section to <a href="#">Table 15</a>. Updated <a href="#">Note 1</a> in <a href="#">Table 31</a>. Revised <a href="#">Table 33</a>. Updated <a href="#">Note 1</a> and <a href="#">Note 2</a> in <a href="#">Table 46</a>.</p> <p>Updated <math>D_{VPPIN}</math> in <a href="#">Table 47</a>. Updated <math>V_{IDIFF}</math> in <a href="#">Table 48</a>. Removed <math>T_{LOCK}</math> and <math>T_{PHASE}</math> and revised <math>F_{GCLK}</math> in <a href="#">Table 51</a>. Updated <math>T_{DLOCK}</math> in <a href="#">Table 52</a>. Updated <a href="#">Table 53</a>. In <a href="#">Table 54</a>, updated <math>T_{RTX}</math>, <math>T_{FTX}</math>, <math>V_{TXOVBVDDP}</math>, and revised <a href="#">Note 1</a> through <a href="#">Note 7</a>. In <a href="#">Table 55</a>, updated <math>RX_{SST}</math> and <math>RX_{PPMTOL}</math> and revised <a href="#">Note 4</a> through <a href="#">Note 7</a>. In <a href="#">Table 60</a>, revised and added <a href="#">Note 1</a>.</p> <p>Revised the maximum external channel input ranges in <a href="#">Table 62</a>. In <a href="#">Table 63</a>, revised <math>F_{MCCK}</math> and added the <a href="#">Internal Configuration Access Port</a> section.</p>