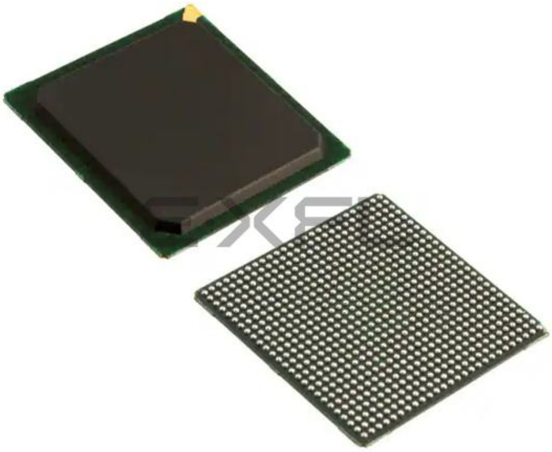
# AMD Xilinx - XC7A75T-2FGG676I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 5900 |
| Number of Logic Elements/Cells | 75520 |
| Total RAM Bits | 3870720 |
| Number of I/O | 300 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7a75t-2fgg676i |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.40 | 100 | –0.40 | 100 |
| $V_{CCO}$ + 0.45 | 100 | –0.45 | 61.7 |
| $V_{CCO}$ + 0.50 | 100 | –0.50 | 25.8 |
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7A100T | 155 | 155 | 155 | 108 | mA |
| | | XC7A200T | 328 | 328 | 328 | 232 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 5 | 5 | 5 | 5 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7A100T | 36 | 36 | 36 | 36 | mA |
| | | XC7A200T | 73 | 73 | 73 | 73 | mA |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7A100T | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 11 | 11 | 11 | 11 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | | $V_{OCM}$(3) | | | $V_{OD}$(4) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage ($Q - \overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage ($Q - \overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | $V_{OL}$(3) | $V_{OH}$(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | $(V_{CCO}/2) - 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage ($Q - \overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

*Table 14:* **Networking Applications Interface Performances**

| Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 15:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

| Memory Standard | Speed Grade | | | | Units |
|---|---|---|---|---|---|
| | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | |
| **4:1 Memory Controllers** | | | | | |
| DDR3 | 1066 | 800 | 800 | 800 | Mb/s |
| DDR3L | 800 | 800 | 667 | 667 | Mb/s |
| DDR2 | 800 | 800 | 667 | 667 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 533 | Mb/s |
| **2:1 Memory Controllers** | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | 620 | Mb/s |
| DDR2 | 800 | 700 | 620 | 620 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).

## IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVTTL_S4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.80 | 3.93 | 4.18 | 4.41 | 4.37 | 4.59 | 5.01 | 5.06 | ns |
| LVTTL_S8 | 1.26 | 1.34 | 1.41 | 1.58 | 3.54 | 3.66 | 3.92 | 4.15 | 4.11 | 4.32 | 4.75 | 4.80 | ns |
| LVTTL_S12 | 1.26 | 1.34 | 1.41 | 1.58 | 3.52 | 3.65 | 3.90 | 4.13 | 4.09 | 4.31 | 4.73 | 4.78 | ns |
| LVTTL_S16 | 1.26 | 1.34 | 1.41 | 1.58 | 3.07 | 3.19 | 3.45 | 3.68 | 3.64 | 3.85 | 4.28 | 4.33 | ns |
| LVTTL_S24 | 1.26 | 1.34 | 1.41 | 1.58 | 3.29 | 3.41 | 3.67 | 3.90 | 3.86 | 4.07 | 4.50 | 4.55 | ns |
| LVTTL_F4 | 1.26 | 1.34 | 1.41 | 1.58 | 3.26 | 3.38 | 3.64 | 3.86 | 3.83 | 4.04 | 4.46 | 4.51 | ns |
| LVTTL_F8 | 1.26 | 1.34 | 1.41 | 1.58 | 2.74 | 2.87 | 3.12 | 3.35 | 3.31 | 3.52 | 3.95 | 4.00 | ns |
| LVTTL_F12 | 1.26 | 1.34 | 1.41 | 1.58 | 2.73 | 2.85 | 3.10 | 3.33 | 3.29 | 3.51 | 3.93 | 3.98 | ns |
| LVTTL_F16 | 1.26 | 1.34 | 1.41 | 1.58 | 2.55 | 2.68 | 2.93 | 3.16 | 3.12 | 3.34 | 3.76 | 3.81 | ns |
| LVTTL_F24 | 1.26 | 1.34 | 1.41 | 1.58 | 2.52 | 2.65 | 2.90 | 3.22 | 3.09 | 3.31 | 3.73 | 3.87 | ns |
| LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| MINI_LVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| BLVDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.84 | 1.96 | 2.21 | 2.44 | 2.40 | 2.62 | 3.04 | 3.09 | ns |
| RSDS_25 (point to point) | 0.73 | 0.81 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.88 | 1.84 | 2.06 | 2.48 | 2.53 | ns |
| PPDS_25 | 0.73 | 0.81 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.88 | 1.86 | 2.07 | 2.49 | 2.53 | ns |
| TMDS_33 | 0.73 | 0.81 | 0.88 | 0.90 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| PCI33_3 | 1.24 | 1.32 | 1.39 | 1.57 | 3.10 | 3.22 | 3.48 | 3.71 | 3.67 | 3.88 | 4.31 | 4.36 | ns |
| HSUL_12 | 0.67 | 0.75 | 0.82 | 0.87 | 1.80 | 1.93 | 2.18 | 2.41 | 2.37 | 2.59 | 3.01 | 3.06 | ns |
| DIFF_HSUL_12 | 0.68 | 0.76 | 0.83 | 0.88 | 1.80 | 1.93 | 2.18 | 2.21 | 2.37 | 2.59 | 3.01 | 2.86 | ns |
| HSTL_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.62 | 1.74 | 1.99 | 2.19 | 2.19 | 2.40 | 2.82 | 2.84 | ns |
| HSTL_II_S | 0.65 | 0.73 | 0.80 | 0.85 | 1.41 | 1.54 | 1.79 | 1.99 | 1.98 | 2.20 | 2.62 | 2.64 | ns |
| HSTL_I_18_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.29 | 1.41 | 1.67 | 1.86 | 1.86 | 2.07 | 2.49 | 2.51 | ns |
| HSTL_II_18_S | 0.66 | 0.75 | 0.81 | 0.87 | 1.41 | 1.54 | 1.79 | 1.97 | 1.98 | 2.20 | 2.62 | 2.62 | ns |
| DIFF_HSTL_I_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.59 | 1.71 | 1.96 | 2.13 | 2.15 | 2.37 | 2.79 | 2.78 | ns |
| DIFF_HSTL_II_S | 0.68 | 0.76 | 0.83 | 0.85 | 1.51 | 1.63 | 1.88 | 2.07 | 2.08 | 2.29 | 2.71 | 2.72 | ns |
| DIFF_HSTL_I_18_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.96 | 1.95 | 2.17 | 2.59 | 2.61 | ns |
| DIFF_HSTL_II_18_S | 0.70 | 0.78 | 0.85 | 0.87 | 1.46 | 1.58 | 1.84 | 2.00 | 2.03 | 2.24 | 2.67 | 2.65 | ns |
| HSTL_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.10 | 1.22 | 1.48 | 1.69 | 1.67 | 1.88 | 2.31 | 2.34 | ns |

*Table 16:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.98 | 1.85 | 1.97 | 2.23 | 2.27 | 2.42 | 2.63 | 3.06 | 2.92 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.98 | 1.60 | 1.72 | 1.98 | 2.21 | 2.17 | 2.38 | 2.81 | 2.86 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.98 | 1.35 | 1.47 | 1.73 | 1.96 | 1.92 | 2.13 | 2.56 | 2.61 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.98 | 1.34 | 1.46 | 1.71 | 1.94 | 1.90 | 2.12 | 2.54 | 2.59 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.08 | 2.57 | 2.69 | 2.95 | 3.18 | 3.14 | 3.35 | 3.78 | 3.83 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.08 | 2.09 | 2.21 | 2.46 | 2.69 | 2.65 | 2.87 | 3.29 | 3.34 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.79 | 1.91 | 2.17 | 2.40 | 2.36 | 2.57 | 2.99 | 3.05 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.08 | 1.98 | 2.10 | 2.35 | 2.58 | 2.54 | 2.76 | 3.18 | 3.23 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.08 | 1.54 | 1.66 | 1.92 | 2.15 | 2.11 | 2.32 | 2.75 | 2.80 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.08 | 1.38 | 1.51 | 1.76 | 1.97 | 1.95 | 2.16 | 2.59 | 2.62 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.80 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.67 | 1.79 | 2.04 | 2.24 | 2.23 | 2.45 | 2.87 | 2.89 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.87 | 1.31 | 1.43 | 1.68 | 1.91 | 1.87 | 2.09 | 2.51 | 2.56 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.35 | 1.47 | 1.73 | 1.93 | 1.92 | 2.13 | 2.56 | 2.58 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.87 | 1.30 | 1.43 | 1.68 | 1.88 | 1.87 | 2.09 | 2.51 | 2.53 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.68 | 1.80 | 2.06 | 2.24 | 2.25 | 2.46 | 2.89 | 2.89 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.94 | 1.95 | 2.17 | 2.59 | 2.59 | ns |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.80 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.72 | 1.69 | 1.90 | 2.32 | 2.37 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL135_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.12 | 1.24 | 1.49 | 1.71 | 1.69 | 1.90 | 2.32 | 2.36 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.87 | 1.07 | 1.19 | 1.45 | 1.68 | 1.64 | 1.85 | 2.28 | 2.33 | ns |
| DIFF_SSTL18_I_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.23 | 1.35 | 1.60 | 1.80 | 1.79 | 2.01 | 2.43 | 2.45 | ns |
| DIFF_SSTL18_II_F | 0.71 | 0.79 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.79 | 1.78 | 1.99 | 2.42 | 2.44 | ns |

Table 17 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 17:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.19 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.30 | ns |

## Output Serializer/Deserializer Switching Characteristics

*Table 21:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.44/–0.25 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.60/–0.25 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.46/–0.25 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.21/–0.15 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.70 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.22/–0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.54 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.63 | ns |
| **Combinatorial** | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.83 | 0.92 | 1.11 | 1.18 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

## Input/Output Delay Switching Characteristics

*Table 22:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **IDELAYCTRL** | | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to ready for IDELAYCTRL | 3.67 | 3.67 | 3.67 | 3.22 | µs |
| $F_{IDELAYCTRL\_REF}$ | Attribute REFCLK frequency = 200.00(1) | 200.00 | 200.00 | 200.00 | 200.00 | MHz |
| | Attribute REFCLK frequency = 300.00(1) | 300.00 | 300.00 | N/A | N/A | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum Reset pulse width | 59.28 | 59.28 | 59.28 | 52.00 | ns |
| **IDELAY** | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY chain delay resolution | 1/(32 x 2 x $F_{REF}$) | | | | ps |
| $T_{IDELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3) | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4) | ±9 | ±9 | ±9 | ±9 | ps per tap |
| $T_{IDELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IDELAY | 680.00 | 680.00 | 600.00 | 520.00 | MHz |
| $T_{IDCCK\_CE}$ / $T_{IDCKC\_CE}$ | CE pin setup/hold with respect to C for IDELAY | 0.12/0.11 | 0.16/0.13 | 0.21/0.16 | 0.14/0.16 | ns |
| $T_{IDCCK\_INC}$/ $T_{IDCKC\_INC}$ | INC pin setup/hold with respect to C for IDELAY | 0.12/0.16 | 0.14/0.18 | 0.16/0.22 | 0.10/0.23 | ns |
| $T_{IDCCK\_RST}$/ $T_{IDCKC\_RST}$ | RST pin setup/hold with respect to C for IDELAY | 0.15/0.09 | 0.16/0.11 | 0.18/0.14 | 0.22/0.19 | ns |
| $T_{IDDO\_IDATAIN}$ | Propagation delay through IDELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

## CLB Switching Characteristics

*Table 24:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.10 | 0.11 | 0.13 | 0.15 | ns, Max |
| $T_{ILO\_2}$ | An – Dn LUT address to AMUX/CMUX | 0.27 | 0.30 | 0.36 | 0.41 | ns, Max |
| $T_{ILO\_3}$ | An – Dn LUT address to BMUX_A | 0.42 | 0.46 | 0.55 | 0.65 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.94 | 1.05 | 1.27 | 1.51 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.62 | 0.69 | 0.84 | 1.01 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.58 | 0.66 | 0.83 | 0.98 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.60 | 0.68 | 0.82 | 0.98 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.68 | 0.75 | 0.90 | 1.08 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.51 | 0.57 | 0.69 | 0.82 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.62 | 0.69 | 0.82 | 0.99 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.42 | 0.48 | 0.58 | 0.69 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.53 | 0.59 | 0.71 | 0.86 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.52 | 0.58 | 0.70 | 0.84 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.40 | 0.44 | 0.53 | 0.62 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.47 | 0.53 | 0.66 | 0.73 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{AS}/T_{AH}$ | $A_N$ – $D_N$ input to CLK on A – D flip-flops | 0.07/0.12 | 0.09/0.14 | 0.11/0.18 | 0.11/0.20 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | $A_X$ – $D_X$ input to CLK on A – D flip-flops | 0.06/0.19 | 0.07/0.21 | 0.09/0.26 | 0.09/0.31 | ns, Min |
| | $A_X$ – $D_X$ input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08 | 0.66/0.09 | 0.81/0.11 | 0.97/0.12 | ns, Min |
| $T_{CECK\_CLB}/$ $T_{CKCE\_CLB}$ | CE input to CLK on A – D flip-flops | 0.15/0.00 | 0.17/0.00 | 0.21/0.01 | 0.34/–0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | 0.38/0.03 | 0.43/0.04 | 0.53/0.05 | 0.62/0.05 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 0.95 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.53 | 0.59 | 0.71 | 0.83 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.70 | 0.83 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412 | 1286 | 1098 | 1098 | MHz |

*Table 27:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{RCCK\_RSTRAM}$/$T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.32/0.42 | 0.34/0.43 | 0.36/0.46 | 0.40/0.47 | ns, Min |
| $T_{RCCK\_WEA}$/$T_{RCKC\_WEA}$ | Write enable (WE) input (block RAM only) | 0.44/0.18 | 0.48/0.19 | 0.54/0.20 | 0.64/0.23 | ns, Min |
| $T_{RCCK\_WREN}$/$T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.46/0.30 | 0.46/0.35 | 0.47/0.43 | 0.77/0.44 | ns, Min |
| $T_{RCCK\_RDEN}$/$T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.42/0.30 | 0.43/0.35 | 0.43/0.43 | 0.71/0.44 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.90 | 0.98 | 1.10 | 1.25 | ns, Max |
| $T_{RREC\_RST}$/$T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.87/–0.81 | 2.07/–0.81 | 2.37/–0.81 | 2.44/–0.71 | ns, Max |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses | 447.63 | 404.53 | 339.67 | 268.96 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled | 467.07 | 418.59 | 345.78 | 273.30 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 405.35 | 362.19 | 297.35 | 226.60 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 509.68 | 460.83 | 388.20 | 315.66 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 410.34 | 365.10 | 297.53 | 215.38 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 28:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.26/ 0.12 | 0.30/ 0.13 | 0.37/ 0.14 | 0.45/ 0.14 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.33/ 0.15 | 0.38/ 0.16 | 0.45/ 0.18 | 0.60/ 0.19 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.17/ 0.17 | 0.20/ 0.19 | 0.24/ 0.21 | 0.34/ 0.29 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.25/ 0.25 | 0.32/ 0.27 | 0.42/ 0.27 | 0.54/ 0.23 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.23/ 0.12 | 0.27/ 0.13 | 0.32/ 0.14 | 0.36/ 0.14 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.25/ 0.15 | 0.29/ 0.16 | 0.36/ 0.18 | 0.41/ 0.19 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/ –0.01 | 2.76/ –0.01 | 3.29/ –0.01 | 4.31/ –0.07 | ns |
| $T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$ | {A, D} input to AD register CLK | 1.29/ –0.02 | 1.48/ –0.02 | 1.76/ –0.02 | 2.29/ –0.27 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/ –0.28 | 4.60/ –0.28 | 5.48/ –0.28 | 6.95/ –0.48 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.93/ –0.73 | 4.50/ –0.73 | 5.35/ –0.73 | 6.73/ –1.68 | ns |
| $T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/ –0.28 | 1.98/ –0.28 | 2.35/ –0.28 | 2.80/ –0.48 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.54/ –0.26 | 1.76/ –0.26 | 2.10/ –0.26 | 2.54/ –0.45 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.32/ –0.15 | 1.51/ –0.15 | 1.80/ –0.15 | 2.13/ –0.25 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/ 0.06 | 0.42/ 0.08 | 0.52/ 0.11 | 0.64/ 0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.28/ 0.10 | 0.34/ 0.11 | 0.42/ 0.13 | 0.49/ 0.16 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.36/ –0.03 | 0.43/ –0.03 | 0.52/ –0.03 | 0.68/ 0.14 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.17/ 0.18 | 0.21/ 0.20 | 0.27/ 0.23 | 0.45/ 0.29 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.36/ 0.01 | 0.43/ 0.01 | 0.53/ 0.01 | 0.63/ 0.00 | ns |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup and Hold Times of the RST Pins** | | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/ 0.11 | 0.46/ 0.13 | 0.55/ 0.15 | 0.63/ 0.40 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.07/ 0.10 | 0.08/ 0.11 | 0.09/ 0.12 | 0.13/ 0.11 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.44/ 0.07 | 0.50/ 0.08 | 0.59/ 0.09 | 0.67/ 0.08 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.21/ 0.22 | 0.23/ 0.24 | 0.27/ 0.28 | 0.28/ 0.35 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.27/ 0.01 | 0.30/ 0.01 | 0.35/ 0.01 | 0.43/ 0.00 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier | 3.79 | 4.35 | 5.18 | 6.61 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier | 3.72 | 4.26 | 5.07 | 6.41 | ns |
| $T_{DSPDO\_B\_P}$ | B input to P output not using multiplier | 1.53 | 1.75 | 2.08 | 2.48 | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output | 1.33 | 1.53 | 1.82 | 2.22 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.55 | 0.63 | 0.74 | 0.87 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier | 4.06 | 4.65 | 5.54 | 7.03 | ns |
| $T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$ | D input to CARRYCASCOUT output using multiplier | 3.97 | 4.54 | 5.40 | 6.81 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77 | 2.03 | 2.41 | 2.88 | ns |
| $T_{DSPDO\_C\_CARRYCASCOUT}$ | C input to CARRYCASCOUT output | 1.58 | 1.81 | 2.15 | 2.62 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | |
| $T_{DSPDO\_ACIN\_P\_MULT}$ | ACIN input to P output using multiplier | 3.65 | 4.19 | 5.00 | 6.40 | ns |
| $T_{DSPDO\_ACIN\_P}$ | ACIN input to P output not using multiplier | 1.37 | 1.57 | 1.88 | 2.44 | ns |
| $T_{DSPDO\_ACIN\_ACOUT}$ | ACIN input to ACOUT output | 0.38 | 0.44 | 0.53 | 0.63 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier | 3.90 | 4.47 | 5.33 | 6.79 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier | 1.61 | 1.85 | 2.21 | 2.84 | ns |
| $T_{DSPDO\_PCIN\_P}$ | PCIN input to P output | 1.11 | 1.28 | 1.52 | 1.82 | ns |
| $T_{DSPDO\_PCIN\_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output | 1.36 | 1.56 | 1.85 | 2.21 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK PREG to P output | 0.33 | 0.37 | 0.44 | 0.54 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_PREG}$ | CLK PREG to CARRYCASCOUT output | 0.52 | 0.59 | 0.69 | 0.84 | ns |

*Table 28:* **DSP48E1 Switching Characteristics *(Cont'd)***

| **Symbol** | **Description** | **Speed Grade** | | | | **Units** |
|---|---|---|---|---|---|---|
| | | **1.0V** | | | **0.9V** | |
| | | **-3** | **-2/-2L** | **-1** | **-2L** | |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.73 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 3.12 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 4.60 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.99 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 6.84 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.65 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.81 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 6.77 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 1.02 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 7.24 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 3.04 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 7.17 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 3.20 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 363.77 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 310.08 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 210.44 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 191.28 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 223.26 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 150.13 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 140.10 | MHz |

## Clock Buffers and Networks

*Table 29:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BCCCK\_CE}$/$T_{BCCKC\_CE}$(1) | CE pins setup/hold | 0.12/0.39 | 0.13/0.40 | 0.16/0.41 | 0.31/0.17 | ns |
| $T_{BCCCK\_S}$/$T_{BCCKC\_S}$(1) | S pins setup/hold | 0.12/0.39 | 0.13/0.40 | 0.16/0.41 | 0.31/0.17 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O | 0.08 | 0.09 | 0.10 | 0.14 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFG}$ | Global clock tree (BUFG) | 628.00 | 628.00 | 464.00 | 394.00 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 30:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O | 1.11 | 1.26 | 1.54 | 1.56 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFIO}$ | I/O clock tree (BUFIO) | 680.00 | 680.00 | 600.00 | 600.00 | MHz |

*Table 31:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O | 0.64 | 0.76 | 0.99 | 1.24 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.34 | 0.39 | 0.52 | 0.72 | ns |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O | 0.81 | 0.85 | 1.09 | 0.96 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFR}$(1) | Regional clock tree (BUFR) | 420.00 | 375.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO $F_{MAX}$ frequency.

*Table 32:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.16 | ns |
| $T_{BHCCK\_CE}$/$T_{BHCKC\_CE}$ | CE pin setup and hold | 0.19/0.13 | 0.22/0.15 | 0.28/0.21 | 0.35/0.08 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 394.00 | MHz |

*Table 33:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $T_{DCD\_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7A100T | 0.27 | 0.33 | 0.36 | 0.48 | ns |
| | | XC7A200T | 0.40 | 0.48 | 0.54 | 0.69 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

*Table 34:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| $MMCM\_F_{MIN\_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM\_F_{MAX\_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM\_F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |

## PLL Switching Characteristics

*Table 35:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| PLL_$F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| PLL_$F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| PLL_$F_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| PLL_$F_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| PLL_$T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_$T_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | |
| PLL_$T_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| PLL_$T_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| PLL_$F_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| PLL_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| PLL_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| $T_{PLLDCK\_DADDR}$/ $T_{PLLCKD\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DI}$/$T_{PLLCKD\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK\_DEN}$/ $T_{PLLCKD\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{PLLDCK\_DWE}$/ $T_{PLLCKD\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.

*Table 44:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.31 | –0.38/1.46 | –0.38/1.76 | –0.16/1.89 | ns |

*Table 45:* **Sample Window**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.35 | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

*Table 46:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7A100T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |
| | | XC7A200T | SBG484 | 111 | ps |
| | | | FBG484 | 109 | ps |
| | | | FBG676 | 121 | ps |
| | | | FFG1156 | 151 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

*Table 54:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 50 | – | ps |
| $T_{FTX}$ | TX fall time | 20%–80% | – | 50 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{6.6}$ | Total Jitter(2)(3) | 6.6 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.6}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.2}$ | Total Jitter(2)(3) | 3.20 Gb/s(4) | – | – | 0.2 | UI |
| $DJ_{3.2}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.2L}$ | Total Jitter(2)(3) | 3.20 Gb/s(5) | – | – | 0.32 | UI |
| $DJ_{3.2L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(6) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(7) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total Jitter(2)(3) | 500 Mb/s | – | – | 0.1 | UI |
| $DJ_{500}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

## GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the UG482: *7 Series FPGAs GTP Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

*Table 56:* **Gigabit Ethernet Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **Gigabit Ethernet Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| **Gigabit Ethernet Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

*Table 57:* **XAUI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **XAUI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| **XAUI Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

*Table 58:* **PCI Express Protocol Characteristics(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **PCI Express Transmitter Jitter Generation** | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI |
| **PCI Express Receiver High Frequency Jitter Tolerance** | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI |
| PCI Express Gen 2(2) | Receiver inherent timing error | 5000 | 0.40 | – | UI |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI |

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

*Table 59:* **CEI-6G Protocol Characteristics**

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|---|---|---|---|---|
| **CEI-6G Transmitter Jitter Generation** | | | | | |
| Total transmitter jitter(1) | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| **CEI-6G Receiver High Frequency Jitter Tolerance** | | | | | |
| Total receiver jitter tolerance(1) | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

## XADC Specifications

*Table 62:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±2 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Unipolar operation | – | – | ±8 | LSBs |
| | | Bipolar operation | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 70 | – | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description |
|---|---|---|
| 09/26/11 | 1.0 | Initial Xilinx release. |
| 11/07/11 | 1.1 | Revised the $V_{OCM}$ specification in Table 11. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35. In Table 36 through Table 43, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46. |
| 02/13/12 | 1.2 | Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade.<br>Updated summary description on page 1. In Table 2, revised $V_{CCO}$ for the 3.3V HR I/O banks and updated $T_j$. Updated the notes in Table 5. Added MGTAVCC and MGTAVTT power supply ramp times to Table 7. Rearranged Table 8, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10. Revised the specifications in Table 11. Revised $V_{IN}$ in Table 47. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the  table. Revised $F_{TXIN}$ and $F_{RXIN}$ in Table 53. Revised $I_{CCADC}$ and updated Note 1 in Table 62. Revised DDR LVDS transmitter data width in Table 14. Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63. Updated Note 1 in Table 33. |
| 06/01/12 | 1.3 | Reorganized entire data sheet including adding Table 40 and Table 44.<br>Updated $T_{SOL}$ in Table 1. Updated $I_{BATT}$ and added $R_{IN\_TERM}$ to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8, updated many parameters including SSTL135 and SSTL135_R. Removed $V_{OX}$ column and added DIFF_HSUL_12 to Table 10. Updated $V_{OL}$ in Table 11. Updated Table 14 and removed notes 2 and 3. Updated Table 15.<br>Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document.<br>In Table 27, updated Reset Delays section including Note 10 and Note 11. In Table 53, replaced $F_{TXOUT}$ with $F_{GLK}$. Updated many of the XADC specifications in Table 62 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 63 to Table 34 and Table 35. |