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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                         |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                  |
| Number of LABs/CLBs            | 5900                                                                                                                                    |
| Number of Logic Elements/Cells | 75520                                                                                                                                   |
| Total RAM Bits                 | 3870720                                                                                                                                 |
| Number of I/O                  | 285                                                                                                                                     |
| Number of Gates                | -                                                                                                                                       |
| Voltage - Supply               | 0.95V ~ 1.05V                                                                                                                           |
| Mounting Type                  | Surface Mount                                                                                                                           |
| Operating Temperature          | 0°C ~ 100°C (TJ)                                                                                                                        |
| Package / Case                 | 484-BBGA                                                                                                                                |
| Supplier Device Package        | 484-FBGA (23x23)                                                                                                                        |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc7a75t-3fgg484e">https://www.e-xfl.com/product-detail/xilinx/xc7a75t-3fgg484e</a> |

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

| Symbol             | Description                                                               | Min | Max  | Units |
|--------------------|---------------------------------------------------------------------------|-----|------|-------|
| <b>Temperature</b> |                                                                           |     |      |       |
| T <sub>STG</sub>   | Storage temperature (ambient)                                             | –65 | 150  | °C    |
| T <sub>SOL</sub>   | Maximum soldering temperature for Pb/Sn component bodies <sup>(6)</sup>   | –   | +220 | °C    |
|                    | Maximum soldering temperature for Pb-free component bodies <sup>(6)</sup> | –   | +260 | °C    |
| T <sub>j</sub>     | Maximum junction temperature <sup>(6)</sup>                               | –   | +125 | °C    |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).
- The maximum limit applied to DC signals.
- For maximum undershoot and overshoot AC specifications, see [Table 4](#).
- For soldering guidelines and thermal considerations, see [UG475: 7 Series FPGA Packaging and Pinout Specification](#).

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup>

| Symbol                                 | Description                                                                                          | Min   | Typ  | Max                     | Units |
|----------------------------------------|------------------------------------------------------------------------------------------------------|-------|------|-------------------------|-------|
| <b>FPGA Logic</b>                      |                                                                                                      |       |      |                         |       |
| V <sub>CCINT</sub>                     | Internal supply voltage                                                                              | 0.95  | 1.00 | 1.05                    | V     |
|                                        | For -2L (0.9V) devices: internal supply voltage                                                      | 0.87  | 0.90 | 0.93                    | V     |
| V <sub>CCAUX</sub>                     | Auxiliary supply voltage                                                                             | 1.71  | 1.80 | 1.89                    | V     |
| V <sub>CCBRAM</sub>                    | Block RAM supply voltage                                                                             | 0.95  | 1.00 | 1.05                    | V     |
| V <sub>CCO</sub> <sup>(3)(4)</sup>     | Supply voltage for 3.3V HR I/O banks                                                                 | 1.14  | –    | 3.465                   | V     |
| V <sub>IN</sub> <sup>(5)</sup>         | I/O input voltage                                                                                    | –0.20 | –    | V <sub>CCO</sub> + 0.20 | V     |
|                                        | I/O input voltage for V <sub>REF</sub> and differential I/O standards                                | –0.20 | –    | 2.625                   | V     |
| I <sub>IN</sub> <sup>(6)</sup>         | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | –     | –    | 10                      | mA    |
| V <sub>CCBATT</sub> <sup>(7)</sup>     | Battery voltage                                                                                      | 1.0   | –    | 1.89                    | V     |
| <b>GTP Transceiver</b>                 |                                                                                                      |       |      |                         |       |
| V <sub>MGTAVCC</sub> <sup>(8)(9)</sup> | Analog supply voltage for the GTP transmitter and receiver circuits                                  | 0.97  | 1.0  | 1.03                    | V     |
| V <sub>MGTAVTT</sub> <sup>(8)(9)</sup> | Analog supply voltage for the GTP transmitter and receiver termination circuits                      | 1.17  | 1.2  | 1.23                    | V     |
| <b>XADC</b>                            |                                                                                                      |       |      |                         |       |
| V <sub>CCADC</sub>                     | XADC supply relative to GNDADC                                                                       | 1.71  | 1.80 | 1.89                    | V     |
| V <sub>REFP</sub>                      | Externally supplied reference voltage                                                                | 1.20  | 1.25 | 1.30                    | V     |

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup> (Cont'd)

| Symbol             | Description                                                                 | Min | Typ | Max | Units |
|--------------------|-----------------------------------------------------------------------------|-----|-----|-----|-------|
| <b>Temperature</b> |                                                                             |     |     |     |       |
| $T_j$              | Junction temperature operating range for commercial (C) temperature devices | 0   | –   | 85  | °C    |
|                    | Junction temperature operating range for extended (E) temperature devices   | 0   | –   | 100 | °C    |
|                    | Junction temperature operating range for industrial (I) temperature devices | –40 | –   | 100 | °C    |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult [UG483](#), 7 Series FPGAs PCB Design and Pin Planning Guide.
3. Configuration data is retained even if  $V_{CCO}$  drops to 0V.
4. Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7.  $V_{CCBATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ .
8. Each voltage listed requires the filter circuit described in [UG482](#): 7 Series FPGAs GTP Transceiver User Guide.
9. Voltages are specified for the temperature range of  $T_j = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Table 3: DC Characteristics Over Recommended Operating Conditions

| Symbol               | Description                                                                                                                                                                     | Min  | Typ <sup>(1)</sup> | Max | Units         |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------|-----|---------------|
| $V_{DRINT}$          | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost)                                                                                               | 0.75 | –                  | –   | V             |
| $V_{DRI}$            | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost)                                                                                               | 1.5  | –                  | –   | V             |
| $I_{REF}$            | $V_{REF}$ leakage current per pin                                                                                                                                               | –    | –                  | 15  | $\mu\text{A}$ |
| $I_L$                | Input or output leakage current per pin (sample-tested)                                                                                                                         | –    | –                  | 15  | $\mu\text{A}$ |
| $C_{IN}^{(2)}$       | Die input capacitance at the pad                                                                                                                                                | –    | –                  | 8   | pF            |
| $I_{RPU}$            | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 3.3\text{V}$                                                                                                    | 90   | –                  | 330 | $\mu\text{A}$ |
|                      | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 2.5\text{V}$                                                                                                    | 68   | –                  | 250 | $\mu\text{A}$ |
|                      | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.8\text{V}$                                                                                                    | 34   | –                  | 220 | $\mu\text{A}$ |
|                      | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.5\text{V}$                                                                                                    | 23   | –                  | 150 | $\mu\text{A}$ |
|                      | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.2\text{V}$                                                                                                    | 12   | –                  | 120 | $\mu\text{A}$ |
| $I_{RPD}$            | Pad pull-down (when selected) @ $V_{IN} = 3.3\text{V}$                                                                                                                          | 68   | –                  | 330 | $\mu\text{A}$ |
|                      | Pad pull-down (when selected) @ $V_{IN} = 1.8\text{V}$                                                                                                                          | 45   | –                  | 180 | $\mu\text{A}$ |
| $I_{CCADC}$          | Analog supply current, analog circuits in powered up state                                                                                                                      | –    | –                  | 25  | mA            |
| $I_{BATT}^{(3)}$     | Battery supply current                                                                                                                                                          | –    | –                  | 150 | nA            |
| $R_{IN\_TERM}^{(4)}$ | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices | 28   | 40                 | 55  | $\Omega$      |
|                      | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices | 35   | 50                 | 65  | $\Omega$      |
|                      | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices | 44   | 60                 | 83  | $\Omega$      |

Table 6 shows the minimum current, in addition to  $I_{CCQ}$ , that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after  $V_{CCINT}$  is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: Power-On Current for Artix-7 Devices<sup>(1)</sup>

| Device   | $I_{CCINTMIN}$     | $I_{CCAUXMIN}$     | $I_{CCOMIN}$                | $I_{CCBRAMMIN}$    | Units |
|----------|--------------------|--------------------|-----------------------------|--------------------|-------|
|          | Typ <sup>(2)</sup> | Typ <sup>(2)</sup> | Typ <sup>(2)</sup>          | Typ <sup>(2)</sup> |       |
| XC7A100T | $I_{CCINTQ} + 170$ | $I_{CCAUXQ} + 40$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 60$ | mA    |
| XC7A200T | $I_{CCINTQ} + 340$ | $I_{CCAUXQ} + 50$  | $I_{CCOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 80$ | mA    |

**Notes:**

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 7: Power Supply Ramp Time

| Symbol            | Description                                                     | Conditions                 | Min | Max | Units |
|-------------------|-----------------------------------------------------------------|----------------------------|-----|-----|-------|
| $T_{VCCINT}$      | Ramp time from GND to 90% of $V_{CCINT}$                        |                            | 0.2 | 50  | ms    |
| $T_{VCCO}$        | Ramp time from GND to 90% of $V_{CCO}$                          |                            | 0.2 | 50  | ms    |
| $T_{VCCAUX}$      | Ramp time from GND to 90% of $V_{CCAUX}$                        |                            | 0.2 | 50  | ms    |
| $T_{VCCBRAM}$     | Ramp time from GND to 90% of $V_{CCBRAM}$                       |                            | 0.2 | 50  | ms    |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ | $T_J = 100^{\circ}C^{(1)}$ | –   | 500 | ms    |
|                   |                                                                 | $T_J = 85^{\circ}C^{(1)}$  | –   | 800 |       |
| $T_{MGTAVCC}$     | Ramp time from GND to 90% of $V_{MGTAVCC}$                      |                            | 0.2 | 50  | ms    |
| $T_{MGTAVTT}$     | Ramp time from GND to 90% of $V_{MGTAVTT}$                      |                            | 0.2 | 50  | ms    |

**Notes:**

1. Based on 240,000 power cycles with nominal  $V_{CCO}$  of 3.3V or 36,500 power cycles with worst case  $V_{CCO}$  of 3.465V.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels<sup>(1)(2)</sup>

| I/O Standard | $V_{IL}$ |                   | $V_{IH}$          |                   | $V_{OL}$            | $V_{OH}$            | $I_{OL}$ | $I_{OH}$ |
|--------------|----------|-------------------|-------------------|-------------------|---------------------|---------------------|----------|----------|
|              | V, Min   | V, Max            | V, Min            | V, Max            | V, Max              | V, Min              | mA, Max  | mA, Min  |
| HSTL_I       | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8.00     | -8.00    |
| HSTL_I_18    | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 8.00     | -8.00    |
| HSTL_II      | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 16.00    | -16.00   |
| HSTL_II_18   | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | 16.00    | -16.00   |
| HSUL_12      | -0.300   | $V_{REF} - 0.130$ | $V_{REF} + 0.130$ | $V_{CCO} + 0.300$ | 20% $V_{CCO}$       | 80% $V_{CCO}$       | 0.10     | -0.10    |
| LVC MOS12    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 3   | Note 3   |
| LVC MOS15    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 25% $V_{CCO}$       | 75% $V_{CCO}$       | Note 4   | Note 4   |
| LVC MOS18    | -0.300   | 35% $V_{CCO}$     | 65% $V_{CCO}$     | $V_{CCO} + 0.300$ | 0.450               | $V_{CCO} - 0.450$   | Note 5   | Note 5   |
| LVC MOS25    | -0.300   | 0.7               | 1.700             | $V_{CCO} + 0.300$ | 0.400               | $V_{CCO} - 0.400$   | Note 4   | Note 4   |
| LVC MOS33    | -0.300   | 0.8               | 2.000             | 3.450             | 0.400               | $V_{CCO} - 0.400$   | Note 4   | Note 4   |
| LV TTL       | -0.300   | 0.8               | 2.000             | 3.450             | 0.400               | 2.400               | Note 5   | Note 5   |
| MOBILE_DDR   | -0.300   | 20% $V_{CCO}$     | 80% $V_{CCO}$     | $V_{CCO} + 0.300$ | 10% $V_{CCO}$       | 90% $V_{CCO}$       | 0.10     | -0.10    |
| PCI33_3      | -0.500   | 30% $V_{CCO}$     | 50% $V_{CCO}$     | $V_{CCO} + 0.500$ | 10% $V_{CCO}$       | 90% $V_{CCO}$       | 1.50     | -0.50    |
| SSTL135      | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 13.00    | -13.00   |
| SSTL135_R    | -0.300   | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 8.90     | -8.90    |
| SSTL15       | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 13.00    | -13.00   |
| SSTL15_R     | -0.300   | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 8.90     | -8.90    |
| SSTL18_I     | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.470$ | $V_{CCO}/2 + 0.470$ | 8.00     | -8.00    |
| SSTL18_II    | -0.300   | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.600$ | $V_{CCO}/2 + 0.600$ | 13.40    | -13.40   |

### Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see [UG471](#): 7 Series FPGAs SelectIO Resources User Guide.

Table 9: Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}^{(1)}$ |        |             | $V_{ID}^{(2)}$ |        |        | $V_{OCM}^{(3)}$ |                 |                 | $V_{OD}^{(4)}$ |        |        |
|--------------|-----------------|--------|-------------|----------------|--------|--------|-----------------|-----------------|-----------------|----------------|--------|--------|
|              | V, Min          | V, Typ | V, Max      | V, Min         | V, Typ | V, Max | V, Min          | V, Typ          | V, Max          | V, Min         | V, Typ | V, Max |
| BLVDS_25     | 0.300           | 1.200  | 1.425       | 0.100          | —      | —      | —               | 1.250           | —               | Note 5         |        |        |
| MINI_LVDS_25 | 0.300           | 1.200  | $V_{CCAUX}$ | 0.200          | 0.400  | 0.600  | 1.000           | 1.200           | 1.400           | 0.300          | 0.450  | 0.600  |
| PPDS_25      | 0.200           | 0.900  | $V_{CCAUX}$ | 0.100          | 0.250  | 0.400  | 0.500           | 0.950           | 1.400           | 0.100          | 0.250  | 0.400  |
| RSDS_25      | 0.300           | 0.900  | 1.500       | 0.100          | 0.350  | 0.600  | 1.000           | 1.200           | 1.400           | 0.100          | 0.350  | 0.600  |
| TMDS_33      | 2.700           | 2.965  | 3.230       | 0.150          | 0.675  | 1.200  | $V_{CCO}-0.405$ | $V_{CCO}-0.300$ | $V_{CCO}-0.190$ | 0.400          | 0.600  | 0.800  |

**Notes:**

1.  $V_{ICM}$  is the input common mode voltage.
2.  $V_{ID}$  is the input differential voltage ( $Q - \bar{Q}$ ).
3.  $V_{OCM}$  is the output common mode voltage.
4.  $V_{OD}$  is the output differential voltage ( $Q - \bar{Q}$ ).
5.  $V_{OD}$  for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

| I/O Standard    | $V_{ICM}^{(1)}$ |        |        | $V_{ID}^{(2)}$ |        | $V_{OL}^{(3)}$        | $V_{OH}^{(4)}$        | $I_{OL}$ | $I_{OH}$ |
|-----------------|-----------------|--------|--------|----------------|--------|-----------------------|-----------------------|----------|----------|
|                 | V, Min          | V, Typ | V, Max | V, Min         | V, Max | V, Max                | V, Min                | mA, Max  | mA, Min  |
| DIFF_HSTL_I     | 0.300           | 0.750  | 1.125  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 8.00     | -8.00    |
| DIFF_HSTL_I_18  | 0.300           | 0.900  | 1.425  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 8.00     | -8.00    |
| DIFF_HSTL_II    | 0.300           | 0.750  | 1.125  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 16.00    | -16.00   |
| DIFF_HSTL_II_18 | 0.300           | 0.900  | 1.425  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 16.00    | -16.00   |
| DIFF_HSUL_12    | 0.300           | 0.600  | 0.850  | 0.100          | —      | 20% $V_{CCO}$         | 80% $V_{CCO}$         | 0.100    | -0.100   |
| DIFF_MOBILE_DDR | 0.300           | 0.900  | 1.425  | 0.100          | —      | 10% $V_{CCO}$         | 90% $V_{CCO}$         | 0.100    | -0.100   |
| DIFF_SSTL135    | 0.300           | 0.675  | 1.000  | 0.100          | —      | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 13.0     | -13.0    |
| DIFF_SSTL135_R  | 0.300           | 0.675  | 1.000  | 0.100          | —      | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.9      | -8.9     |
| DIFF_SSTL15     | 0.300           | 0.750  | 1.125  | 0.100          | —      | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 13.0     | -13.0    |
| DIFF_SSTL15_R   | 0.300           | 0.750  | 1.125  | 0.100          | —      | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 8.9      | -8.9     |
| DIFF_SSTL18_I   | 0.300           | 0.900  | 1.425  | 0.100          | —      | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 8.00     | -8.00    |
| DIFF_SSTL18_II  | 0.300           | 0.900  | 1.425  | 0.100          | —      | $(V_{CCO}/2) - 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4     | -13.4    |

**Notes:**

1.  $V_{ICM}$  is the input common mode voltage.
2.  $V_{ID}$  is the input differential voltage ( $Q - \bar{Q}$ ).
3.  $V_{OL}$  is the single-ended low-output voltage.
4.  $V_{OH}$  is the single-ended high-output voltage.

Table 16: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

| I/O Standard      | T <sub>IOPI</sub> |        |      |      | T <sub>IOOP</sub> |        |      |      | T <sub>IOTP</sub> |        |      |      | Units |
|-------------------|-------------------|--------|------|------|-------------------|--------|------|------|-------------------|--------|------|------|-------|
|                   | Speed Grade       |        |      |      | Speed Grade       |        |      |      | Speed Grade       |        |      |      |       |
|                   | 1.0V              |        | 0.9V |      | 1.0V              |        | 0.9V |      | 1.0V              |        | 0.9V |      |       |
|                   | -3                | -2/-2L | -1   | -2L  | -3                | -2/-2L | -1   | -2L  | -3                | -2/-2L | -1   | -2L  |       |
| HSTL_II_F         | 0.65              | 0.73   | 0.80 | 0.85 | 1.12              | 1.24   | 1.49 | 1.71 | 1.69              | 1.90   | 2.32 | 2.36 | ns    |
| HSTL_I_18_F       | 0.67              | 0.75   | 0.82 | 0.87 | 1.13              | 1.26   | 1.51 | 1.72 | 1.70              | 1.92   | 2.34 | 2.37 | ns    |
| HSTL_II_18_F      | 0.66              | 0.75   | 0.81 | 0.87 | 1.12              | 1.24   | 1.49 | 1.71 | 1.69              | 1.90   | 2.32 | 2.36 | ns    |
| DIFF_HSTL_I_F     | 0.68              | 0.76   | 0.83 | 0.85 | 1.18              | 1.30   | 1.56 | 1.77 | 1.75              | 1.96   | 2.39 | 2.42 | ns    |
| DIFF_HSTL_II_F    | 0.68              | 0.76   | 0.83 | 0.85 | 1.21              | 1.33   | 1.59 | 1.77 | 1.78              | 1.99   | 2.42 | 2.42 | ns    |
| DIFF_HSTL_I_18_F  | 0.71              | 0.79   | 0.86 | 0.87 | 1.21              | 1.33   | 1.59 | 1.77 | 1.78              | 1.99   | 2.42 | 2.42 | ns    |
| DIFF_HSTL_II_18_F | 0.70              | 0.78   | 0.85 | 0.87 | 1.21              | 1.33   | 1.59 | 1.77 | 1.78              | 1.99   | 2.42 | 2.42 | ns    |
| LVC MOS33_S4      | 1.26              | 1.34   | 1.41 | 1.62 | 3.80              | 3.93   | 4.18 | 4.41 | 4.37              | 4.59   | 5.01 | 5.06 | ns    |
| LVC MOS33_S8      | 1.26              | 1.34   | 1.41 | 1.62 | 3.52              | 3.65   | 3.90 | 4.13 | 4.09              | 4.31   | 4.73 | 4.78 | ns    |
| LVC MOS33_S12     | 1.26              | 1.34   | 1.41 | 1.62 | 3.09              | 3.21   | 3.46 | 3.69 | 3.65              | 3.87   | 4.29 | 4.34 | ns    |
| LVC MOS33_S16     | 1.26              | 1.34   | 1.41 | 1.62 | 3.40              | 3.52   | 3.77 | 4.00 | 3.97              | 4.18   | 4.60 | 4.65 | ns    |
| LVC MOS33_F4      | 1.26              | 1.34   | 1.41 | 1.62 | 3.26              | 3.38   | 3.64 | 3.86 | 3.83              | 4.04   | 4.46 | 4.51 | ns    |
| LVC MOS33_F8      | 1.26              | 1.34   | 1.41 | 1.62 | 2.74              | 2.87   | 3.12 | 3.35 | 3.31              | 3.52   | 3.95 | 4.00 | ns    |
| LVC MOS33_F12     | 1.26              | 1.34   | 1.41 | 1.62 | 2.55              | 2.68   | 2.93 | 3.16 | 3.12              | 3.34   | 3.76 | 3.81 | ns    |
| LVC MOS33_F16     | 1.26              | 1.34   | 1.41 | 1.62 | 2.55              | 2.68   | 2.93 | 3.16 | 3.12              | 3.34   | 3.76 | 3.81 | ns    |
| LVC MOS25_S4      | 1.12              | 1.20   | 1.27 | 1.43 | 3.13              | 3.26   | 3.51 | 3.72 | 3.70              | 3.91   | 4.34 | 4.37 | ns    |
| LVC MOS25_S8      | 1.12              | 1.20   | 1.27 | 1.43 | 2.88              | 3.01   | 3.26 | 3.49 | 3.45              | 3.67   | 4.09 | 4.14 | ns    |
| LVC MOS25_S12     | 1.12              | 1.20   | 1.27 | 1.43 | 2.48              | 2.60   | 2.85 | 3.08 | 3.05              | 3.26   | 3.68 | 3.73 | ns    |
| LVC MOS25_S16     | 1.12              | 1.20   | 1.27 | 1.43 | 2.82              | 2.94   | 3.20 | 3.43 | 3.39              | 3.60   | 4.03 | 4.08 | ns    |
| LVC MOS25_F4      | 1.12              | 1.20   | 1.27 | 1.43 | 2.74              | 2.87   | 3.12 | 3.35 | 3.31              | 3.52   | 3.95 | 4.00 | ns    |
| LVC MOS25_F8      | 1.12              | 1.20   | 1.27 | 1.43 | 2.18              | 2.30   | 2.56 | 2.79 | 2.75              | 2.96   | 3.39 | 3.44 | ns    |
| LVC MOS25_F12     | 1.12              | 1.20   | 1.27 | 1.43 | 2.16              | 2.29   | 2.54 | 2.77 | 2.73              | 2.95   | 3.37 | 3.42 | ns    |
| LVC MOS25_F16     | 1.12              | 1.20   | 1.27 | 1.43 | 2.01              | 2.13   | 2.39 | 2.61 | 2.58              | 2.79   | 3.21 | 3.26 | ns    |
| LVC MOS18_S4      | 0.74              | 0.83   | 0.89 | 0.94 | 1.62              | 1.74   | 1.99 | 2.19 | 2.19              | 2.40   | 2.82 | 2.84 | ns    |
| LVC MOS18_S8      | 0.74              | 0.83   | 0.89 | 0.94 | 2.18              | 2.30   | 2.56 | 2.79 | 2.75              | 2.96   | 3.39 | 3.44 | ns    |
| LVC MOS18_S12     | 0.74              | 0.83   | 0.89 | 0.94 | 2.18              | 2.30   | 2.56 | 2.79 | 2.75              | 2.96   | 3.39 | 3.44 | ns    |
| LVC MOS18_S16     | 0.74              | 0.83   | 0.89 | 0.94 | 1.52              | 1.65   | 1.90 | 2.13 | 2.09              | 2.31   | 2.73 | 2.78 | ns    |
| LVC MOS18_S24     | 0.74              | 0.83   | 0.89 | 0.94 | 1.60              | 1.72   | 1.98 | 2.21 | 2.17              | 2.38   | 2.81 | 2.86 | ns    |
| LVC MOS18_F4      | 0.74              | 0.83   | 0.89 | 0.94 | 1.45              | 1.57   | 1.82 | 2.05 | 2.01              | 2.23   | 2.65 | 2.70 | ns    |
| LVC MOS18_F8      | 0.74              | 0.83   | 0.89 | 0.94 | 1.68              | 1.80   | 2.06 | 2.29 | 2.25              | 2.46   | 2.89 | 2.94 | ns    |
| LVC MOS18_F12     | 0.74              | 0.83   | 0.89 | 0.94 | 1.68              | 1.80   | 2.06 | 2.29 | 2.25              | 2.46   | 2.89 | 2.94 | ns    |
| LVC MOS18_F16     | 0.74              | 0.83   | 0.89 | 0.94 | 1.40              | 1.52   | 1.77 | 2.00 | 1.97              | 2.18   | 2.60 | 2.65 | ns    |
| LVC MOS18_F24     | 0.74              | 0.83   | 0.89 | 0.94 | 1.34              | 1.46   | 1.71 | 1.94 | 1.90              | 2.12   | 2.54 | 2.59 | ns    |
| LVC MOS15_S4      | 0.77              | 0.86   | 0.93 | 0.98 | 2.05              | 2.18   | 2.43 | 2.50 | 2.62              | 2.84   | 3.26 | 3.15 | ns    |
| LVC MOS15_S8      | 0.77              | 0.86   | 0.93 | 0.98 | 2.09              | 2.21   | 2.46 | 2.69 | 2.65              | 2.87   | 3.29 | 3.34 | ns    |
| LVC MOS15_S12     | 0.77              | 0.86   | 0.93 | 0.98 | 1.59              | 1.71   | 1.96 | 2.19 | 2.15              | 2.37   | 2.79 | 2.84 | ns    |
| LVC MOS15_S16     | 0.77              | 0.86   | 0.93 | 0.98 | 1.59              | 1.71   | 1.96 | 2.19 | 2.15              | 2.37   | 2.79 | 2.84 | ns    |

## Input Serializer/Deserializer Switching Characteristics

Table 20: ISERDES Switching Characteristics

| Symbol                                                       | Description                                                                    | Speed Grade |            |            |            | Units |
|--------------------------------------------------------------|--------------------------------------------------------------------------------|-------------|------------|------------|------------|-------|
|                                                              |                                                                                | 1.0V        |            |            | 0.9V       |       |
|                                                              |                                                                                | -3          | -2/-2L     | -1         | -2L        |       |
| Setup/Hold for Control Lines                                 |                                                                                |             |            |            |            |       |
| T <sub>ISCK_BITSIP</sub> / T <sub>ISCK_BITSIP</sub>          | BITSIP pin setup/hold with respect to CLKDIV                                   | 0.01/0.14   | 0.02/0.15  | 0.02/0.17  | 0.02/0.21  | ns    |
| T <sub>ISCK_CE</sub> / T <sub>ISCK_CE</sub> <sup>(2)</sup>   | CE pin setup/hold with respect to CLK (for CE1)                                | 0.45/−0.01  | 0.50/−0.01 | 0.72/−0.01 | 0.35/−0.11 | ns    |
| T <sub>ISCK_CE2</sub> / T <sub>ISCK_CE2</sub> <sup>(2)</sup> | CE pin setup/hold with respect to CLKDIV (for CE2)                             | −0.10/0.33  | −0.10/0.36 | −0.10/0.40 | −0.17/0.40 | ns    |
| Setup/Hold for Data Lines                                    |                                                                                |             |            |            |            |       |
| T <sub>ISDCK_D</sub> / T <sub>ISCKD_D</sub>                  | D pin setup/hold with respect to CLK                                           | −0.02/0.12  | −0.02/0.14 | −0.02/0.17 | −0.04/0.19 | ns    |
| T <sub>ISDCK_DDLY</sub> / T <sub>ISCKD_DDLY</sub>            | DDLY pin setup/hold with respect to CLK (using IDELAY) <sup>(1)</sup>          | −0.02/0.12  | −0.02/0.14 | −0.02/0.17 | −0.03/0.19 | ns    |
| T <sub>ISDCK_D_DDR</sub> / T <sub>ISCKD_D_DDR</sub>          | D pin setup/hold with respect to CLK at DDR mode                               | −0.02/0.12  | −0.02/0.14 | −0.02/0.17 | −0.04/0.19 | ns    |
| T <sub>ISDCK_DDLY_DDR</sub> / T <sub>ISCKD_DDLY_DDR</sub>    | D pin setup/hold with respect to CLK at DDR mode (using IDELAY) <sup>(1)</sup> | 0.12/0.12   | 0.14/0.14  | 0.17/0.17  | 0.19/0.19  | ns    |
| Sequential Delays                                            |                                                                                |             |            |            |            |       |
| T <sub>ISCO_Q</sub>                                          | CLKDIV to out at Q pin                                                         | 0.53        | 0.54       | 0.66       | 0.67       | ns    |
| Propagation Delays                                           |                                                                                |             |            |            |            |       |
| T <sub>ISDO_DO</sub>                                         | D input to DO output pin                                                       | 0.11        | 0.11       | 0.13       | 0.14       | ns    |

### Notes:

- Recorded at 0 tap value.
- $T_{ISCK\_CE2}$  and  $T_{ISCK\_CE2}$  are reported as  $T_{ISCK\_CE} / T_{ISCK\_CE}$  in TRACE report.

Table 23: IO\_FIFO Switching Characteristics

| Symbol                                             | Description            | Speed Grade |            |            |            | Units |
|----------------------------------------------------|------------------------|-------------|------------|------------|------------|-------|
|                                                    |                        | 1.0V        |            |            | 0.9V       |       |
|                                                    |                        | -3          | -2/-2L     | -1         | -2L        |       |
| IO_FIFO Clock to Out Delays                        |                        |             |            |            |            |       |
| T <sub>OFFCKO_DO</sub>                             | RDCLK to Q outputs     | 0.55        | 0.60       | 0.68       | 0.81       | ns    |
| T <sub>CKO_FLAGS</sub>                             | Clock to IO_FIFO flags | 0.55        | 0.61       | 0.77       | 0.55       | ns    |
| Setup/Hold                                         |                        |             |            |            |            |       |
| T <sub>CCK_D</sub> /T <sub>CKC_D</sub>             | D inputs to WRCLK      | 0.47/0.02   | 0.51/0.02  | 0.58/0.02  | 0.76/−0.05 | ns    |
| T <sub>IFFCKC_WREN</sub> /T <sub>IFFCKC_WREN</sub> | WREN to WRCLK          | 0.42/−0.01  | 0.47/−0.01 | 0.53/−0.01 | 0.70/−0.05 | ns    |
| T <sub>OFFCKC_RDEN</sub> /T <sub>OFFCKC_RDEN</sub> | RDEN to RDCLK          | 0.53/0.02   | 0.58/0.02  | 0.66/0.02  | 0.79/−0.02 | ns    |
| Minimum Pulse Width                                |                        |             |            |            |            |       |
| T <sub>PWH_IO_FIFO</sub>                           | RESET, RDCLK, WRCLK    | 1.62        | 2.15       | 2.15       | 2.15       | ns    |
| T <sub>PWL_IO_FIFO</sub>                           | RESET, RDCLK, WRCLK    | 1.62        | 2.15       | 2.15       | 2.15       | ns    |
| Maximum Frequency                                  |                        |             |            |            |            |       |
| F <sub>MAX</sub>                                   | RDCLK and WRCLK        | 266.67      | 200.00     | 200.00     | 200.00     | MHz   |

## CLB Switching Characteristics

Table 24: CLB Switching Characteristics

| Symbol                                                        | Description                                                                                      | Speed Grade |           |           |            | Units   |
|---------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-------------|-----------|-----------|------------|---------|
|                                                               |                                                                                                  | 1.0V        |           |           | 0.9V       |         |
|                                                               |                                                                                                  | -3          | -2/-2L    | -1        | -2L        |         |
| Combinatorial Delays                                          |                                                                                                  |             |           |           |            |         |
| T <sub>ILO</sub>                                              | An – Dn LUT address to A                                                                         | 0.10        | 0.11      | 0.13      | 0.15       | ns, Max |
| T <sub>ILO_2</sub>                                            | An – Dn LUT address to AMUX/CMUX                                                                 | 0.27        | 0.30      | 0.36      | 0.41       | ns, Max |
| T <sub>ILO_3</sub>                                            | An – Dn LUT address to BMUX_A                                                                    | 0.42        | 0.46      | 0.55      | 0.65       | ns, Max |
| T <sub>ITO</sub>                                              | An – Dn inputs to A – D Q outputs                                                                | 0.94        | 1.05      | 1.27      | 1.51       | ns, Max |
| T <sub>AXA</sub>                                              | AX inputs to AMUX output                                                                         | 0.62        | 0.69      | 0.84      | 1.01       | ns, Max |
| T <sub>AXB</sub>                                              | AX inputs to BMUX output                                                                         | 0.58        | 0.66      | 0.83      | 0.98       | ns, Max |
| T <sub>AXC</sub>                                              | AX inputs to CMUX output                                                                         | 0.60        | 0.68      | 0.82      | 0.98       | ns, Max |
| T <sub>AXD</sub>                                              | AX inputs to DMUX output                                                                         | 0.68        | 0.75      | 0.90      | 1.08       | ns, Max |
| T <sub>BXB</sub>                                              | BX inputs to BMUX output                                                                         | 0.51        | 0.57      | 0.69      | 0.82       | ns, Max |
| T <sub>BXD</sub>                                              | BX inputs to DMUX output                                                                         | 0.62        | 0.69      | 0.82      | 0.99       | ns, Max |
| T <sub>CXC</sub>                                              | CX inputs to CMUX output                                                                         | 0.42        | 0.48      | 0.58      | 0.69       | ns, Max |
| T <sub>CXD</sub>                                              | CX inputs to DMUX output                                                                         | 0.53        | 0.59      | 0.71      | 0.86       | ns, Max |
| T <sub>DXD</sub>                                              | DX inputs to DMUX output                                                                         | 0.52        | 0.58      | 0.70      | 0.84       | ns, Max |
| Sequential Delays                                             |                                                                                                  |             |           |           |            |         |
| T <sub>CKO</sub>                                              | Clock to AQ – DQ outputs                                                                         | 0.40        | 0.44      | 0.53      | 0.62       | ns, Max |
| T <sub>SHCKO</sub>                                            | Clock to AMUX – DMUX outputs                                                                     | 0.47        | 0.53      | 0.66      | 0.73       | ns, Max |
| Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK |                                                                                                  |             |           |           |            |         |
| T <sub>AS</sub> /T <sub>AH</sub>                              | A <sub>N</sub> – D <sub>N</sub> input to CLK on A – D flip-flops                                 | 0.07/0.12   | 0.09/0.14 | 0.11/0.18 | 0.11/0.20  | ns, Min |
| T <sub>DICK</sub> /T <sub>CKDI</sub>                          | A <sub>X</sub> – D <sub>X</sub> input to CLK on A – D flip-flops                                 | 0.06/0.19   | 0.07/0.21 | 0.09/0.26 | 0.09/0.31  | ns, Min |
|                                                               | A <sub>X</sub> – D <sub>X</sub> input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08   | 0.66/0.09 | 0.81/0.11 | 0.97/0.12  | ns, Min |
| T <sub>CECK_CLB</sub> /T <sub>CKCE_CLB</sub>                  | CE input to CLK on A – D flip-flops                                                              | 0.15/0.00   | 0.17/0.00 | 0.21/0.01 | 0.34/–0.01 | ns, Min |
| T <sub>SRCK</sub> /T <sub>CKSR</sub>                          | SR input to CLK on A – D flip-flops                                                              | 0.38/0.03   | 0.43/0.04 | 0.53/0.05 | 0.62/0.05  | ns, Min |
| Set/Reset                                                     |                                                                                                  |             |           |           |            |         |
| T <sub>SRMIN</sub>                                            | SR input minimum pulse width                                                                     | 0.52        | 0.78      | 1.04      | 0.95       | ns, Min |
| T <sub>RQ</sub>                                               | Delay from SR input to AQ – DQ flip-flops                                                        | 0.53        | 0.59      | 0.71      | 0.83       | ns, Max |
| T <sub>CEO</sub>                                              | Delay from CE input to AQ – DQ flip-flops                                                        | 0.52        | 0.58      | 0.70      | 0.83       | ns, Max |
| F <sub>TOG</sub>                                              | Toggle frequency (for export control)                                                            | 1412        | 1286      | 1098      | 1098       | MHz     |

Table 28: DSP48E1 Switching Characteristics (Cont'd)

| Symbol                                                                                     | Description                                              | Speed Grade   |               |               |               | Units |
|--------------------------------------------------------------------------------------------|----------------------------------------------------------|---------------|---------------|---------------|---------------|-------|
|                                                                                            |                                                          | 1.0V          |               |               | 0.9V          |       |
|                                                                                            |                                                          | -3            | -2/-2L        | -1            | -2L           |       |
| Setup and Hold Times of the RST Pins                                                       |                                                          |               |               |               |               |       |
| T <sub>DSPDCK_{RSTA; RSTB}_{AREG; BREG}/T<sub>DSPCKD_{RSTA; RSTB}_{AREG; BREG}</sub></sub> | {RSTA, RSTB} input to {A, B} register CLK                | 0.41/<br>0.11 | 0.46/<br>0.13 | 0.55/<br>0.15 | 0.63/<br>0.40 | ns    |
| T <sub>DSPDCK_RSTC_CREG/T<sub>DSPCKD_RSTC_CREG</sub></sub>                                 | RSTC input to C register CLK                             | 0.07/<br>0.10 | 0.08/<br>0.11 | 0.09/<br>0.12 | 0.13/<br>0.11 | ns    |
| T <sub>DSPDCK_RSTD_DREG/T<sub>DSPCKD_RSTD_DREG</sub></sub>                                 | RSTD input to D register CLK                             | 0.44/<br>0.07 | 0.50/<br>0.08 | 0.59/<br>0.09 | 0.67/<br>0.08 | ns    |
| T <sub>DSPDCK_RSTM_MREG/T<sub>DSPCKD_RSTM_MREG</sub></sub>                                 | RSTM input to M register CLK                             | 0.21/<br>0.22 | 0.23/<br>0.24 | 0.27/<br>0.28 | 0.28/<br>0.35 | ns    |
| T <sub>DSPDCK_RSTP_PREG/T<sub>DSPCKD_RSTP_PREG</sub></sub>                                 | RSTP input to P register CLK                             | 0.27/<br>0.01 | 0.30/<br>0.01 | 0.35/<br>0.01 | 0.43/<br>0.00 | ns    |
| Combinatorial Delays from Input Pins to Output Pins                                        |                                                          |               |               |               |               |       |
| T <sub>DSPDO_A_CARRYOUT_MULT</sub>                                                         | A input to CARRYOUT output using multiplier              | 3.79          | 4.35          | 5.18          | 6.61          | ns    |
| T <sub>DSPDO_D_P_MULT</sub>                                                                | D input to P output using multiplier                     | 3.72          | 4.26          | 5.07          | 6.41          | ns    |
| T <sub>DSPDO_B_P</sub>                                                                     | B input to P output not using multiplier                 | 1.53          | 1.75          | 2.08          | 2.48          | ns    |
| T <sub>DSPDO_C_P</sub>                                                                     | C input to P output                                      | 1.33          | 1.53          | 1.82          | 2.22          | ns    |
| Combinatorial Delays from Input Pins to Cascading Output Pins                              |                                                          |               |               |               |               |       |
| T <sub>DSPDO_{A; B}_{ACOUT; BCOUT}</sub>                                                   | {A, B} input to {ACOUT, BCOUT} output                    | 0.55          | 0.63          | 0.74          | 0.87          | ns    |
| T <sub>DSPDO_{A, B}_CARRYCASCOUT_MULT</sub>                                                | {A, B} input to CARRYCASCOUT output using multiplier     | 4.06          | 4.65          | 5.54          | 7.03          | ns    |
| T <sub>DSPDO_D_CARRYCASCOUT_MULT</sub>                                                     | D input to CARRYCASCOUT output using multiplier          | 3.97          | 4.54          | 5.40          | 6.81          | ns    |
| T <sub>DSPDO_{A, B}_CARRYCASCOUT</sub>                                                     | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77          | 2.03          | 2.41          | 2.88          | ns    |
| T <sub>DSPDO_C_CARRYCASCOUT</sub>                                                          | C input to CARRYCASCOUT output                           | 1.58          | 1.81          | 2.15          | 2.62          | ns    |
| Combinatorial Delays from Cascading Input Pins to All Output Pins                          |                                                          |               |               |               |               |       |
| T <sub>DSPDO_ACIN_P_MULT</sub>                                                             | ACIN input to P output using multiplier                  | 3.65          | 4.19          | 5.00          | 6.40          | ns    |
| T <sub>DSPDO_ACIN_P</sub>                                                                  | ACIN input to P output not using multiplier              | 1.37          | 1.57          | 1.88          | 2.44          | ns    |
| T <sub>DSPDO_ACIN_ACOUT</sub>                                                              | ACIN input to ACOUT output                               | 0.38          | 0.44          | 0.53          | 0.63          | ns    |
| T <sub>DSPDO_ACIN_CARRYCASCOUT_MULT</sub>                                                  | ACIN input to CARRYCASCOUT output using multiplier       | 3.90          | 4.47          | 5.33          | 6.79          | ns    |
| T <sub>DSPDO_ACIN_CARRYCASCOUT</sub>                                                       | ACIN input to CARRYCASCOUT output not using multiplier   | 1.61          | 1.85          | 2.21          | 2.84          | ns    |
| T <sub>DSPDO_PCIN_P</sub>                                                                  | PCIN input to P output                                   | 1.11          | 1.28          | 1.52          | 1.82          | ns    |
| T <sub>DSPDO_PCIN_CARRYCASCOUT</sub>                                                       | PCIN input to CARRYCASCOUT output                        | 1.36          | 1.56          | 1.85          | 2.21          | ns    |
| Clock to Outs from Output Register Clock to Output Pins                                    |                                                          |               |               |               |               |       |
| T <sub>DSPCKO_P_PREG</sub>                                                                 | CLK PREG to P output                                     | 0.33          | 0.37          | 0.44          | 0.54          | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_PREG</sub>                                                      | CLK PREG to CARRYCASCOUT output                          | 0.52          | 0.59          | 0.69          | 0.84          | ns    |

Table 28: DSP48E1 Switching Characteristics (Cont'd)

| Symbol                                                           | Description                                                  | Speed Grade |        |        |        | Units |
|------------------------------------------------------------------|--------------------------------------------------------------|-------------|--------|--------|--------|-------|
|                                                                  |                                                              | 1.0V        |        |        | 0.9V   |       |
|                                                                  |                                                              | -3          | -2/-2L | -1     | -2L    |       |
| Clock to Outs from Pipeline Register Clock to Output Pins        |                                                              |             |        |        |        |       |
| T <sub>DSPCKO_P_MREG</sub>                                       | CLK MREG to P output                                         | 1.68        | 1.93   | 2.31   | 2.73   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_MREG</sub>                            | CLK MREG to CARRYCASCOUT output                              | 1.92        | 2.21   | 2.64   | 3.12   | ns    |
| T <sub>DSPCKO_P_ADREG_MULT</sub>                                 | CLK ADREG to P output using multiplier                       | 2.72        | 3.10   | 3.69   | 4.60   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_ADREG_MULT</sub>                      | CLK ADREG to CARRYCASCOUT output using multiplier            | 2.96        | 3.38   | 4.02   | 4.99   | ns    |
| Clock to Outs from Input Register Clock to Output Pins           |                                                              |             |        |        |        |       |
| T <sub>DSPCKO_P_AREG_MULT</sub>                                  | CLK AREG to P output using multiplier                        | 3.94        | 4.51   | 5.37   | 6.84   | ns    |
| T <sub>DSPCKO_P_BREG</sub>                                       | CLK BREG to P output not using multiplier                    | 1.64        | 1.87   | 2.22   | 2.65   | ns    |
| T <sub>DSPCKO_P_CREG</sub>                                       | CLK CREG to P output not using multiplier                    | 1.69        | 1.93   | 2.30   | 2.81   | ns    |
| T <sub>DSPCKO_P_DREG_MULT</sub>                                  | CLK DREG to P output using multiplier                        | 3.91        | 4.48   | 5.32   | 6.77   | ns    |
| Clock to Outs from Input Register Clock to Cascading Output Pins |                                                              |             |        |        |        |       |
| T <sub>DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}</sub>                  | CLK (ACOUT, BCOUT) to {A,B} register output                  | 0.64        | 0.73   | 0.87   | 1.02   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT</sub>               | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier     | 4.19        | 4.79   | 5.70   | 7.24   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_BREG</sub>                            | CLK BREG to CARRYCASCOUT output not using multiplier         | 1.88        | 2.15   | 2.55   | 3.04   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_DREG_MULT</sub>                       | CLK DREG to CARRYCASCOUT output using multiplier             | 4.16        | 4.76   | 5.65   | 7.17   | ns    |
| T <sub>DSPCKO_CARRYCASCOUT_CREG</sub>                            | CLK CREG to CARRYCASCOUT output                              | 1.94        | 2.21   | 2.63   | 3.20   | ns    |
| Maximum Frequency                                                |                                                              |             |        |        |        |       |
| F <sub>MAX</sub>                                                 | With all registers used                                      | 628.93      | 550.66 | 464.25 | 363.77 | MHz   |
| F <sub>MAX_PATDET</sub>                                          | With pattern detector                                        | 531.63      | 465.77 | 392.93 | 310.08 | MHz   |
| F <sub>MAX_MULT_NOMREG</sub>                                     | Two register multiply without MREG                           | 349.28      | 305.62 | 257.47 | 210.44 | MHz   |
| F <sub>MAX_MULT_NOMREG_PATDET</sub>                              | Two register multiply without MREG with pattern detect       | 317.26      | 277.62 | 233.92 | 191.28 | MHz   |
| F <sub>MAX_PREADD_MULT_NOADREG</sub>                             | Without ADREG                                                | 397.30      | 346.26 | 290.44 | 223.26 | MHz   |
| F <sub>MAX_PREADD_MULT_NOADREG_PATDET</sub>                      | Without ADREG with pattern detect                            | 397.30      | 346.26 | 290.44 | 223.26 | MHz   |
| F <sub>MAX_NOPIPELINEREG</sub>                                   | Without pipeline registers (MREG, ADREG)                     | 260.01      | 227.01 | 190.69 | 150.13 | MHz   |
| F <sub>MAX_NOPIPELINEREG_PATDET</sub>                            | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72      | 211.15 | 177.43 | 140.10 | MHz   |

## Clock Buffers and Networks

Table 29: Global Clock Switching Characteristics (Including BUFGCTRL)

| Symbol                              | Description                    | Speed Grade |           |           |           | Units |
|-------------------------------------|--------------------------------|-------------|-----------|-----------|-----------|-------|
|                                     |                                | 1.0V        |           |           | 0.9V      |       |
|                                     |                                | -3          | -2/-2L    | -1        | -2L       |       |
| $T_{BCCCK\_CE}/T_{BCCCK\_CE}^{(1)}$ | CE pins setup/hold             | 0.12/0.39   | 0.13/0.40 | 0.16/0.41 | 0.31/0.17 | ns    |
| $T_{BCCCK\_S}/T_{BCCCK\_S}^{(1)}$   | S pins setup/hold              | 0.12/0.39   | 0.13/0.40 | 0.16/0.41 | 0.31/0.17 | ns    |
| $T_{BCKO\_O}^{(2)}$                 | BUFGCTRL delay from I0/I1 to O | 0.08        | 0.09      | 0.10      | 0.14      | ns    |
| <b>Maximum Frequency</b>            |                                |             |           |           |           |       |
| $F_{MAX\_BUFG}$                     | Global clock tree (BUFG)       | 628.00      | 628.00    | 464.00    | 394.00    | MHz   |

**Notes:**

1.  $T_{BCCCK\_CE}$  and  $T_{BCCCK\_S}$  must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2.  $T_{BCKO\_O}$  (BUFG delay from I0 to O) values are the same as  $T_{BCKO\_O}$  values.

Table 30: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol                   | Description                    | Speed Grade |        |        |        | Units |
|--------------------------|--------------------------------|-------------|--------|--------|--------|-------|
|                          |                                | 1.0V        |        |        | 0.9V   |       |
|                          |                                | -3          | -2/-2L | -1     | -2L    |       |
| $T_{BIOCKO\_O}$          | Clock to out delay from I to O | 1.11        | 1.26   | 1.54   | 1.56   | ns    |
| <b>Maximum Frequency</b> |                                |             |        |        |        |       |
| $F_{MAX\_BUFIO}$         | I/O clock tree (BUFIO)         | 680.00      | 680.00 | 600.00 | 600.00 | MHz   |

Table 31: Regional Clock Buffer Switching Characteristics (BUFR)

| Symbol                   | Description                                                     | Speed Grade |        |        |        | Units |
|--------------------------|-----------------------------------------------------------------|-------------|--------|--------|--------|-------|
|                          |                                                                 | 1.0V        |        |        | 0.9V   |       |
|                          |                                                                 | -3          | -2/-2L | -1     | -2L    |       |
| $T_{BRCKO\_O}$           | Clock to out delay from I to O                                  | 0.64        | 0.76   | 0.99   | 1.24   | ns    |
| $T_{BRCKO\_O\_BYP}$      | Clock to out delay from I to O with Divide Bypass attribute set | 0.34        | 0.39   | 0.52   | 0.72   | ns    |
| $T_{BRDO\_O}$            | Propagation delay from CLR to O                                 | 0.81        | 0.85   | 1.09   | 0.96   | ns    |
| <b>Maximum Frequency</b> |                                                                 |             |        |        |        |       |
| $F_{MAX\_BUFR}^{(1)}$    | Regional clock tree (BUFR)                                      | 420.00      | 375.00 | 315.00 | 315.00 | MHz   |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO  $F_{MAX}$  frequency.

Table 32: Horizontal Clock Buffer Switching Characteristics (BUFH)

| Symbol                      | Description                    | Speed Grade |           |           |           | Units |
|-----------------------------|--------------------------------|-------------|-----------|-----------|-----------|-------|
|                             |                                | 1.0V        |           |           | 0.9V      |       |
|                             |                                | -3          | -2/-2L    | -1        | -2L       |       |
| $T_{BHCKO\_O}$              | BUFH delay from I to O         | 0.10        | 0.11      | 0.13      | 0.16      | ns    |
| $T_{BHCK\_CE}/T_{BHCK\_CE}$ | CE pin setup and hold          | 0.19/0.13   | 0.22/0.15 | 0.28/0.21 | 0.35/0.08 | ns    |
| <b>Maximum Frequency</b>    |                                |             |           |           |           |       |
| $F_{MAX\_BUFH}$             | Horizontal clock buffer (BUFH) | 628.00      | 628.00    | 464.00    | 394.00    | MHz   |

Table 33: Duty Cycle Distortion and Clock-Tree Skew

| Symbol           | Description                                            | Device   | Speed Grade |        |      |      | Units |
|------------------|--------------------------------------------------------|----------|-------------|--------|------|------|-------|
|                  |                                                        |          | 1.0V        |        |      | 0.9V |       |
|                  |                                                        |          | -3          | -2/-2L | -1   | -2L  |       |
| $T_{DCD\_CLK}$   | Global clock tree duty-cycle distortion <sup>(1)</sup> | All      | 0.20        | 0.20   | 0.20 | 0.25 | ns    |
| $T_{CKSKEW}$     | Global clock tree skew <sup>(2)</sup>                  | XC7A100T | 0.27        | 0.33   | 0.36 | 0.48 | ns    |
|                  |                                                        | XC7A200T | 0.40        | 0.48   | 0.54 | 0.69 | ns    |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion                   | All      | 0.14        | 0.14   | 0.14 | 0.14 | ns    |
| $T_{BUFIOSKEW}$  | I/O clock tree skew across one clock region            | All      | 0.03        | 0.03   | 0.03 | 0.03 | ns    |
| $T_{DCD\_BUFR}$  | Regional clock tree duty cycle distortion              | All      | 0.18        | 0.18   | 0.18 | 0.18 | ns    |

**Notes:**

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The  $T_{CKSKEW}$  value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA\_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

Table 34: MMCM Specification

| Symbol                 | Description                                 | Speed Grade                             |         |         |         | Units |
|------------------------|---------------------------------------------|-----------------------------------------|---------|---------|---------|-------|
|                        |                                             | 1.0V                                    |         |         | 0.9V    |       |
|                        |                                             | -3                                      | -2/-2L  | -1      | -2L     |       |
| $MMCM\_F_{INMAX}$      | Maximum input clock frequency               | 800.00                                  | 800.00  | 800.00  | 800.00  | MHz   |
| $MMCM\_F_{INMIN}$      | Minimum input clock frequency               | 10.00                                   | 10.00   | 10.00   | 10.00   | MHz   |
| $MMCM\_F_{INJITTER}$   | Maximum input clock period jitter           | < 20% of clock input period or 1 ns Max |         |         |         |       |
| $MMCM\_F_{INDUTY}$     | Allowable input duty cycle: 10—49 MHz       | 25                                      | 25      | 25      | 25      | %     |
|                        | Allowable input duty cycle: 50—199 MHz      | 30                                      | 30      | 30      | 30      | %     |
|                        | Allowable input duty cycle: 200—399 MHz     | 35                                      | 35      | 35      | 35      | %     |
|                        | Allowable input duty cycle: 400—499 MHz     | 40                                      | 40      | 40      | 40      | %     |
|                        | Allowable input duty cycle: >500 MHz        | 45                                      | 45      | 45      | 45      | %     |
| $MMCM\_F_{MIN\_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01                                    | 0.01    | 0.01    | 0.01    | MHz   |
| $MMCM\_F_{MAX\_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00                                  | 500.00  | 450.00  | 450.00  | MHz   |
| $MMCM\_F_{VCOMIN}$     | Minimum MMCM VCO frequency                  | 600.00                                  | 600.00  | 600.00  | 600.00  | MHz   |
| $MMCM\_F_{VCOMAX}$     | Maximum MMCM VCO frequency                  | 1600.00                                 | 1440.00 | 1200.00 | 1200.00 | MHz   |

Table 34: MMCM Specification (Cont'd)

| Symbol                                                            | Description                                            | Speed Grade                             |           |           |           | Units    |
|-------------------------------------------------------------------|--------------------------------------------------------|-----------------------------------------|-----------|-----------|-----------|----------|
|                                                                   |                                                        | 1.0V                                    |           |           | 0.9V      |          |
|                                                                   |                                                        | -3                                      | -2/-2L    | -1        | -2L       |          |
| MMCM_F <sub>BANDWIDTH</sub>                                       | Low MMCM bandwidth at typical <sup>(1)</sup>           | 1.00                                    | 1.00      | 1.00      | 1.00      | MHz      |
|                                                                   | High MMCM bandwidth at typical <sup>(1)</sup>          | 4.00                                    | 4.00      | 4.00      | 4.00      | MHz      |
| MMCM_T <sub>STATPHAOFFSET</sub>                                   | Static phase offset of the MMCM outputs <sup>(2)</sup> | 0.12                                    | 0.12      | 0.12      | 0.12      | ns       |
| MMCM_T <sub>OUTJITTER</sub>                                       | MMCM output jitter                                     | Note 3                                  |           |           |           |          |
| MMCM_T <sub>OUTDUTY</sub>                                         | MMCM output clock duty-cycle precision <sup>(4)</sup>  | 0.20                                    | 0.20      | 0.20      | 0.25      | ns       |
| MMCM_T <sub>LOCKMAX</sub>                                         | MMCM maximum lock time                                 | 100.00                                  | 100.00    | 100.00    | 100.00    | μs       |
| MMCM_F <sub>OUTMAX</sub>                                          | MMCM maximum output frequency                          | 800.00                                  | 800.00    | 800.00    | 800.00    | MHz      |
| MMCM_F <sub>OUTMIN</sub>                                          | MMCM minimum output frequency <sup>(5)(6)</sup>        | 4.69                                    | 4.69      | 4.69      | 4.69      | MHz      |
| MMCM_T <sub>EXTFDVAR</sub>                                        | External clock feedback variation                      | < 20% of clock input period or 1 ns Max |           |           |           |          |
| MMCM_RST <sub>MINPULSE</sub>                                      | Minimum reset pulse width                              | 5.00                                    | 5.00      | 5.00      | 5.00      | ns       |
| MMCM_F <sub>PFDMAX</sub>                                          | Maximum frequency at the phase frequency detector      | 550.00                                  | 500.00    | 450.00    | 450.00    | MHz      |
| MMCM_F <sub>PFDMIN</sub>                                          | Minimum frequency at the phase frequency detector      | 10.00                                   | 10.00     | 10.00     | 10.00     | MHz      |
| MMCM_T <sub>FBDELAY</sub>                                         | Maximum delay in the feedback path                     | 3 ns Max or one CLKIN cycle             |           |           |           |          |
| MMCM Switching Characteristics Setup and Hold                     |                                                        |                                         |           |           |           |          |
| T <sub>MMCMDCK_PSEN</sub> /<br>T <sub>MMCMCKD_PSEN</sub>          | Setup and hold of phase-shift enable                   | 1.04/0.00                               | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns       |
| T <sub>MMCMDCK_PSINCDEC</sub> /<br>T <sub>MMCMCKD_PSINCDEC</sub>  | Setup and hold of phase-shift increment/decrement      | 1.04/0.00                               | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns       |
| T <sub>MMCMCKO_PSDONE</sub>                                       | Phase shift clock-to-out of PSDONE                     | 0.59                                    | 0.68      | 0.81      | 0.78      | ns       |
| Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK |                                                        |                                         |           |           |           |          |
| T <sub>MMCMDCK_DADDR</sub> /<br>T <sub>MMCMCKD_DADDR</sub>        | DADDR setup/hold                                       | 1.25/0.15                               | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>MMCMDCK_DI</sub> /<br>T <sub>MMCMCKD_DI</sub>              | DI setup/hold                                          | 1.25/0.15                               | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>MMCMDCK_DEN</sub> /<br>T <sub>MMCMCKD_DEN</sub>            | DEN setup/hold                                         | 1.76/0.00                               | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min  |
| T <sub>MMCMDCK_DWE</sub> /<br>T <sub>MMCMCKD_DWE</sub>            | DWE setup/hold                                         | 1.25/0.15                               | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min  |
| T <sub>MMCMCKO_DRDY</sub>                                         | CLK to out of DRDY                                     | 0.65                                    | 0.72      | 0.99      | 0.70      | ns, Max  |
| F <sub>DCK</sub>                                                  | DCLK frequency                                         | 200.00                                  | 200.00    | 200.00    | 100.00    | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.  
See [http://www.xilinx.com/products/intellectual-property/clocking\\_wizard.htm](http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm).
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.
6. When CLKOUT4\_CASCADE = TRUE, MMCM\_F<sub>OUTMIN</sub> is 0.036 MHz.

## Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

**Table 36: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

| Symbol                                                                                                            | Description                                                                     | Device   | Speed Grade |        |      |      | Units |
|-------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|----------|-------------|--------|------|------|-------|
|                                                                                                                   |                                                                                 |          | 1.0V        |        |      | 0.9V |       |
|                                                                                                                   |                                                                                 |          | -3          | -2/-2L | -1   | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. |                                                                                 |          |             |        |      |      |       |
| T <sub>ICKOF</sub>                                                                                                | Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region) | XC7A100T | 5.14        | 5.74   | 6.72 | 7.64 | ns    |
|                                                                                                                   |                                                                                 | XC7A200T | 5.47        | 6.11   | 7.16 | 8.10 | ns    |

### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

**Table 37: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

| Symbol                                                                                                            | Description                                                                    | Device   | Speed Grade |        |      |      | Units |
|-------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|----------|-------------|--------|------|------|-------|
|                                                                                                                   |                                                                                |          | 1.0V        |        |      | 0.9V |       |
|                                                                                                                   |                                                                                |          | -3          | -2/-2L | -1   | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. |                                                                                |          |             |        |      |      |       |
| T <sub>ICKOFFAR</sub>                                                                                             | Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region) | XC7A100T | 5.38        | 6.01   | 7.02 | 7.96 | ns    |
|                                                                                                                   |                                                                                | XC7A200T | 6.17        | 6.89   | 8.05 | 9.05 | ns    |

### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

**Table 38: Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol                                                                                                     | Description                                          | Device   | Speed Grade |        |      |      | Units |
|------------------------------------------------------------------------------------------------------------|------------------------------------------------------|----------|-------------|--------|------|------|-------|
|                                                                                                            |                                                      |          | 1.0V        |        |      | 0.9V |       |
|                                                                                                            |                                                      |          | -3          | -2/-2L | -1   | -2L  |       |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM. |                                                      |          |             |        |      |      |       |
| T <sub>ICKOFMMCMCC</sub>                                                                                   | Clock-capable clock input and OUTFF <i>with</i> MMCM | XC7A100T | 0.89        | 0.94   | 0.96 | 1.81 | ns    |
|                                                                                                            |                                                      | XC7A200T | 0.90        | 0.97   | 1.01 | 1.86 | ns    |

### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 44: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

| Symbol                                                                                             | Description                 | Speed Grade |            |            |            | Units |
|----------------------------------------------------------------------------------------------------|-----------------------------|-------------|------------|------------|------------|-------|
|                                                                                                    |                             | 1.0V        |            |            | 0.9V       |       |
|                                                                                                    |                             | -3          | -2/-2L     | -1         | -2L        |       |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. |                             |             |            |            |            |       |
| T <sub>PSCS</sub> /T <sub>PHCS</sub>                                                               | Setup and hold of I/O clock | −0.38/1.31  | −0.38/1.46 | −0.38/1.76 | −0.16/1.89 | ns    |

Table 45: Sample Window

| Symbol            | Description                                                | Speed Grade |        |      |      | Units |
|-------------------|------------------------------------------------------------|-------------|--------|------|------|-------|
|                   |                                                            | 1.0V        |        |      | 0.9V |       |
|                   |                                                            | -3          | -2/-2L | -1   | -2L  |       |
| $T_{SAMP}$        | Sampling error at receiver pins <sup>(1)</sup>             | 0.59        | 0.64   | 0.70 | 0.70 | ns    |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO <sup>(2)</sup> | 0.35        | 0.40   | 0.46 | 0.46 | ns    |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 MMCM jitter
  - MMCM accuracy (phase offset)
  - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

**Additional Package Parameter Guidelines**

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 46: Package Skew

| Symbol        | Description                 | Device   | Package | Value | Units |
|---------------|-----------------------------|----------|---------|-------|-------|
| $T_{PKGSKEW}$ | Package skew <sup>(1)</sup> | XC7A100T | CSG324  | 113   | ps    |
|               |                             |          | FTG256  | 120   | ps    |
|               |                             |          | FGG484  | 144   | ps    |
|               |                             |          | FGG676  | 153   | ps    |
|               |                             | XC7A200T | SBG484  | 111   | ps    |
|               |                             |          | FBG484  | 109   | ps    |
|               |                             |          | FBG676  | 121   | ps    |
|               |                             |          | FFG1156 | 151   | ps    |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further details.

Table 48: GTP Transceiver Clock DC Input Level Specification

| Symbol             | DC Parameter                            | Min | Typ | Max  | Units |
|--------------------|-----------------------------------------|-----|-----|------|-------|
| V <sub>IDIFF</sub> | Differential peak-to-peak input voltage | 350 | –   | 2000 | mV    |
| R <sub>IN</sub>    | Differential input resistance           | –   | 100 | –    | Ω     |
| C <sub>EXT</sub>   | Required external AC coupling capacitor | –   | 100 | –    | nF    |

## GTP Transceiver Switching Characteristics

Consult [UG482: 7 Series FPGAs GTP Transceiver User Guide](#) for further information.

Table 49: GTP Transceiver Performance

| Symbol                    | Description                         | Output<br>Divider | Speed Grade       |                   |                   |                   |                   |                   |                   |                   | Units |
|---------------------------|-------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------|
|                           |                                     |                   | 1.0V              |                   |                   |                   |                   |                   | 0.9V              |                   |       |
|                           |                                     |                   | -3                |                   | -2/-2L            |                   | -1                |                   | -2L               |                   |       |
|                           |                                     |                   | Package Type      |                   |                   |                   |                   |                   |                   |                   |       |
|                           |                                     |                   | FFG<br>FBG<br>SBG | FGG<br>FTG<br>CSG | FFG<br>FBG<br>SBG | FGG<br>FTG<br>CSG | FFG<br>FBG<br>SBG | FGG<br>FTG<br>CSG | FFG<br>FBG<br>SBG | FGG<br>FTG<br>CSG |       |
| F <sub>GTPMAX</sub>       | Maximum GTP transceiver data rate   |                   | 6.6               | 5.4               | 6.6               | 5.4               | 3.75              | 3.75              | 3.75              | 3.75              | Gb/s  |
| F <sub>GTPMIN</sub>       | Minimum GTP transceiver data rate   |                   | 0.500             | 0.500             | 0.500             | 0.500             | 0.500             | 0.500             | 0.500             | 0.500             | Gb/s  |
| F <sub>GTPRANGE</sub>     | PLL line rate range                 | 1                 | 3.2–6.6           |                   | 3.2–6.6           |                   | 3.2–3.75          |                   | 3.2–3.75          |                   | Gb/s  |
|                           |                                     | 2                 | 1.6–3.3           |                   | 1.6–3.3           |                   | 1.6–3.2           |                   | 1.6–3.2           |                   | Gb/s  |
|                           |                                     | 4                 | 0.8–1.65          |                   | 0.8–1.65          |                   | 0.8–1.6           |                   | 0.8–1.6           |                   | Gb/s  |
|                           |                                     | 8                 | 0.5–0.825         |                   | 0.5–0.825         |                   | 0.5–0.8           |                   | 0.5–0.8           |                   | Gb/s  |
| F <sub>GTPPLL</sub> RANGE | GTP transceiver PLL frequency range |                   | 1.6–3.3           |                   | 1.6–3.3           |                   | 1.6–3.3           |                   | 1.6–3.3           |                   | GHz   |

Table 50: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                 | Speed Grade |        |     |      | Units |
|------------------------|-----------------------------|-------------|--------|-----|------|-------|
|                        |                             | 1.0V        |        |     | 0.9V |       |
|                        |                             | -3          | -2/-2L | -1  | -2L  |       |
| F <sub>GTPDRPCLK</sub> | GTPDRPCLK maximum frequency | 175         | 175    | 156 | 125  | MHz   |

Table 51: GTP Transceiver Reference Clock Switching Characteristics

| Symbol             | Description                     | Conditions           | All Speed Grades |     |     | Units |
|--------------------|---------------------------------|----------------------|------------------|-----|-----|-------|
|                    |                                 |                      | Min              | Typ | Max |       |
| F <sub>GCLK</sub>  | Reference clock frequency range |                      | 60               | –   | 660 | MHz   |
| T <sub>RCLK</sub>  | Reference clock rise time       | 20% – 80%            | –                | 200 | –   | ps    |
| T <sub>FCLK</sub>  | Reference clock fall time       | 20% – 80%            | –                | 200 | –   | ps    |
| T <sub>DCREF</sub> | Reference clock duty cycle      | Transceiver PLL only | 40               | –   | 60  | %     |

Table 60: CPRI Protocol Characteristics

| Description                                     | Line Rate (Mb/s)      | Min  | Max  | Units |
|-------------------------------------------------|-----------------------|------|------|-------|
| <b>CPRI Transmitter Jitter Generation</b>       |                       |      |      |       |
| Total transmitter jitter                        | 614.4                 | –    | 0.35 | UI    |
|                                                 | 1228.8                | –    | 0.35 | UI    |
|                                                 | 2457.6                | –    | 0.35 | UI    |
|                                                 | 3072.0                | –    | 0.35 | UI    |
|                                                 | 4915.2                | –    | 0.3  | UI    |
|                                                 | 6144.0                | –    | 0.3  | UI    |
| <b>CPRI Receiver Frequency Jitter Tolerance</b> |                       |      |      |       |
| Total receiver jitter tolerance                 | 614.4                 | 0.65 | –    | UI    |
|                                                 | 1228.8                | 0.65 | –    | UI    |
|                                                 | 2457.6                | 0.65 | –    | UI    |
|                                                 | 3072.0                | 0.65 | –    | UI    |
|                                                 | 4915.2 <sup>(1)</sup> | 0.60 | –    | UI    |
|                                                 | 6144.0 <sup>(1)</sup> | 0.60 | –    | UI    |

**Notes:**

1. Tested to CEI-6G-SR.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 61: Maximum Performance for PCI Express Designs

| Symbol                | Description                    | Speed Grade |        |        |        | Units |
|-----------------------|--------------------------------|-------------|--------|--------|--------|-------|
|                       |                                | 1.0V        |        |        | 0.9V   |       |
|                       |                                | -3          | -2/-2L | -1     | -2L    |       |
| F <sub>PIPECLK</sub>  | Pipe clock maximum frequency   | 250.00      | 250.00 | 250.00 | 250.00 | MHz   |
| F <sub>USERCLK</sub>  | User clock maximum frequency   | 250.00      | 250.00 | 250.00 | 250.00 | MHz   |
| F <sub>USERCLK2</sub> | User clock 2 maximum frequency | 250.00      | 250.00 | 250.00 | 250.00 | MHz   |
| F <sub>DRPCLK</sub>   | DRP clock maximum frequency    | 250.00      | 250.00 | 250.00 | 250.00 | MHz   |

Table 63: Configuration Switching Characteristics (Cont'd)

| Symbol                                         | Description                                                 | Speed Grade |            |            |            | Units    |
|------------------------------------------------|-------------------------------------------------------------|-------------|------------|------------|------------|----------|
|                                                |                                                             | 1.0V        |            |            | 0.9V       |          |
|                                                |                                                             | -3          | -2/-2L     | -1         | -2L        |          |
| Internal Configuration Access Port             |                                                             |             |            |            |            |          |
| F <sub>ICAPCK</sub>                            | Internal configuration access port (ICAPE2) clock frequency | 100.00      | 100.00     | 100.00     | 70.00      | MHz, Max |
| Master/Slave Serial Mode Programming Switching |                                                             |             |            |            |            |          |
| T <sub>DCCK</sub> /T <sub>CCKD</sub>           | DIN setup/hold                                              | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 5.00/0.00  | ns, Min  |
| T <sub>CCO</sub>                               | DOUT clock to out                                           | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max  |
| SelectMAP Mode Programming Switching           |                                                             |             |            |            |            |          |
| T <sub>SMDCCK</sub> /T <sub>SMCCKD</sub>       | D[31:00] setup/hold                                         | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 4.50/0.00  | ns, Min  |
| T <sub>SMCSCCK</sub> /T <sub>SMCCCKS</sub>     | CSI_B setup/hold                                            | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 5.00/0.00  | ns, Min  |
| T <sub>SMWCCK</sub> /T <sub>SMCCKW</sub>       | RDWR_B setup/hold                                           | 10.00/0.00  | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min  |
| T <sub>SMCKCSO</sub>                           | CSO_B clock to out (330 Ω pull-up resistor required)        | 7.00        | 7.00       | 7.00       | 8.00       | ns, Max  |
| T <sub>SMCO</sub>                              | D[31:00] clock to out in readback                           | 8.00        | 8.00       | 8.00       | 10.00      | ns, Max  |
| F <sub>RBCK</sub>                              | Readback frequency                                          | 100.00      | 100.00     | 100.00     | 70.00      | MHz, Max |
| Boundary-Scan Port Timing Specifications       |                                                             |             |            |            |            |          |
| T <sub>TAPTCK</sub> /T <sub>TCKTAP</sub>       | TMS and TDI setup/hold                                      | 3.00/2.00   | 3.00/2.00  | 3.00/2.00  | 3.00/2.00  | ns, Min  |
| T <sub>TCKTDO</sub>                            | TCK falling edge to TDO output                              | 7.00        | 7.00       | 7.00       | 8.50       | ns, Max  |
| F <sub>TCK</sub>                               | TCK frequency                                               | 66.00       | 66.00      | 66.00      | 50.00      | MHz, Max |
| BPI Flash Master Mode Programming Switching    |                                                             |             |            |            |            |          |
| T <sub>BPICCO</sub> <sup>(2)</sup>             | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out  | 8.50        | 8.50       | 8.50       | 10.00      | ns, Max  |
| T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>       | D[15:00] setup/hold                                         | 4.00/0.00   | 4.00/0.00  | 4.00/0.00  | 4.50/0.00  | ns, Min  |
| SPI Flash Master Mode Programming Switching    |                                                             |             |            |            |            |          |
| T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>       | D[03:00] setup/hold                                         | 3.00/0.00   | 3.00/0.00  | 3.00/0.00  | 3.00/0.00  | ns, Min  |
| T <sub>SPICCM</sub>                            | MOSI clock to out                                           | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max  |
| T <sub>SPICCF</sub>                            | FCS_B clock to out                                          | 8.00        | 8.00       | 8.00       | 9.00       | ns, Max  |

**Notes:**

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 64: eFUSE Programming Conditions<sup>(1)</sup>

| Symbol          | Description                       | Min | Typ | Max | Units |
|-----------------|-----------------------------------|-----|-----|-----|-------|
| I <sub>FS</sub> | V <sub>CCAUX</sub> supply current | —   | —   | 115 | mA    |
| t <sub>j</sub>  | Temperature range                 | 15  | —   | 125 | °C    |

**Notes:**

- The FPGA must not be configured during eFUSE programming.

## Revision History

The following table shows the revision history for this document:

| Date     | Version | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 09/26/11 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11/07/11 | 1.1     | Revised the $V_{OCM}$ specification in <a href="#">Table 11</a> . Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 13.3 software v1.02 speed specification throughout document including <a href="#">Table 12</a> and <a href="#">Table 13</a> . Added $MMCM\_T_{FBDELAY}$ while adding $MMCM\_$ to the symbol names of a few specifications in <a href="#">Table 34</a> and PLL to the symbol names in <a href="#">Table 35</a> . In <a href="#">Table 36</a> through <a href="#">Table 43</a> , updated the pin-to-pin description with the SSTL15 standard. Updated units in <a href="#">Table 46</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 02/13/12 | 1.2     | Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade.<br>Updated summary description on <a href="#">page 1</a> . In <a href="#">Table 2</a> , revised $V_{CCO}$ for the 3.3V HR I/O banks and updated $T_j$ . Updated the notes in <a href="#">Table 5</a> . Added MGTAVCC and MGTAVTT power supply ramp times to <a href="#">Table 7</a> . Rearranged <a href="#">Table 8</a> , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added <a href="#">Table 9</a> and <a href="#">Table 10</a> . Revised the specifications in <a href="#">Table 11</a> . Revised $V_{IN}$ in <a href="#">Table 47</a> . Updated the <a href="#">eFUSE Programming Conditions</a> section and removed the endurance table. Added the table. Revised $F_{TXIN}$ and $F_{RXIN}$ in <a href="#">Table 53</a> . Revised $I_{CCADC}$ and updated <a href="#">Note 1</a> in <a href="#">Table 62</a> . Revised DDR LVDS transmitter data width in <a href="#">Table 14</a> . Removed notes from <a href="#">Table 24</a> as they are no longer applicable. Updated specifications in <a href="#">Table 63</a> . Updated <a href="#">Note 1</a> in <a href="#">Table 33</a> . |
| 06/01/12 | 1.3     | Reorganized entire data sheet including adding <a href="#">Table 40</a> and <a href="#">Table 44</a> .<br>Updated $T_{SOL}$ in <a href="#">Table 1</a> . Updated $I_{BATT}$ and added $R_{IN\_TERM}$ to <a href="#">Table 3</a> . Updated <a href="#">Power-On/Off Power Supply Sequencing</a> section with regards to GTP transceivers. In <a href="#">Table 8</a> , updated many parameters including SSTL135 and SSTL135_R. Removed $V_{OX}$ column and added DIFF_HSUL_12 to <a href="#">Table 10</a> . Updated $V_{OL}$ in <a href="#">Table 11</a> . Updated <a href="#">Table 14</a> and removed notes 2 and 3. Updated <a href="#">Table 15</a> .<br>Updated the <a href="#">AC Switching Characteristics</a> based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document.<br>In <a href="#">Table 27</a> , updated <a href="#">Reset Delays</a> section including <a href="#">Note 10</a> and <a href="#">Note 11</a> . In <a href="#">Table 53</a> , replaced $F_{TXOUT}$ with $F_{GLK}$ . Updated many of the XADC specifications in <a href="#">Table 62</a> and added <a href="#">Note 2</a> . Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from <a href="#">Table 63</a> to <a href="#">Table 34</a> and <a href="#">Table 35</a> .                                                                                  |