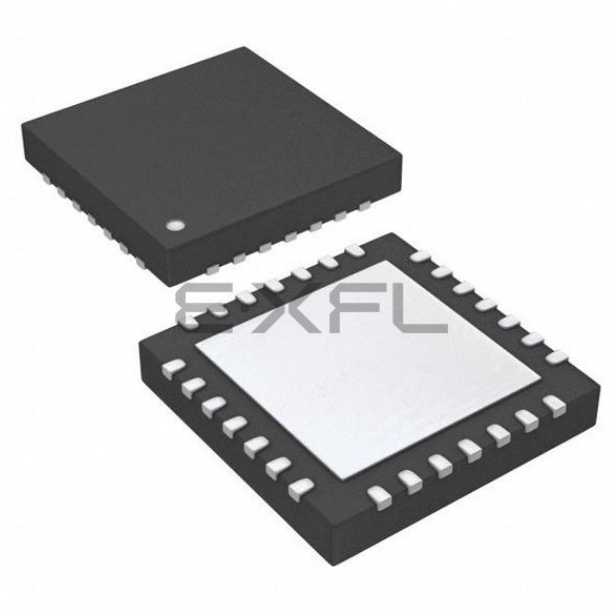

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15356-e-mv

TABLE 1-4: PIC16(L)F15385/86 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD1/AND1/SDA2(1)/SDI2(1,4)	RD1	TTL/ST	CMOS/OD	General purpose I/O.
	AND1	AN	—	ADC Channel D0 input.
	SDA2(1)	I^2C	OD	MSSP2 I^2C serial data input/output.
	SDI2(1,4)	TTL/ST	—	MSSP2 SPI serial data input (default input location, SDI2 is a PPS remappable input and output).
RD2/AND2	RD2	TTL/ST	CMOS/OD	General purpose I/O.
	AND2	AN	—	ADC Channel D0 input.
RD3/AND3	RD3	TTL/ST	CMOS/OD	General purpose I/O.
	AND3	AN	—	ADC Channel D0 input.
RD4/AND4	RD4	TTL/ST	CMOS/OD	General purpose I/O.
	AND4	AN	—	ADC Channel D0 input.
RD5/AND5	RD5	TTL/ST	CMOS/OD	General purpose I/O.
	AND5	AN	—	ADC Channel D0 input.
RD6/AND6	RD6	TTL/ST	CMOS/OD	General purpose I/O.
	AND6	AN	—	ADC Channel D0 input.
RD7/AND7	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN	—	ADC Channel D0 input.
RE0/ANE0	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN	—	ADC Channel D0 input.
RE1/ANE1	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE1	AN	—	ADC Channel D0 input.
RE2/ANE2	RE2	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel D0 input.
RE3/$\overline{\text{MCLR}}$/IOCE3	RE3	TTL/ST	—	General purpose input only (when $\overline{\text{MCLR}}$ is disabled by the Configuration bit).
	$\overline{\text{MCLR}}$	ST	—	Master clear input with internal weak pull-up resistor.
	IOCE3	TTL/ST	—	Interrupt-on-change input.
RF0/ANF0	RF0	TTL/ST	CMOS/OD	General purpose I/O.
	ANF0	AN	—	ADC Channel D0 input.
RF1/ANF1	RF1	TTL/ST	CMOS/OD	General purpose I/O.
	ANF1	AN	—	ADC Channel D0 input.
RF2/ANF2	RF2	TTL/ST	CMOS/OD	General purpose I/O.
	ANF2	AN	—	ADC Channel D0 input.
RF3/ANF3	RF3	TTL/ST	CMOS/OD	General purpose I/O.
	ANF3	AN	—	ADC Channel D0 input.
RF4/ANF4	RF4	TTL/ST	CMOS/OD	General purpose I/O.
	ANF4	AN	—	ADC Channel D0 input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-5, Table 15-6 and Table 15-7.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 16											
CPU CORE REGISTERS; see Table 4-3 for specifics											
80Ch	WDTCON0	—	—	WDTPS<4:0>					SWDTEN	--qq qqq0	--qq qqq0
80Dh	WDTCON1	—	WDTCS<2:0>			—	WINDOW<2:0>			-qqq -qqq	-qqq -qqq
80Eh	WDTPSL	PSCNT<7:0>								0000 0000	0000 0000
80Fh	WDTPSH	PSCNT<15:8>								0000 0000	0000 0000
810h	WDTTMR	—	WDTTMR<3:0>				STATE	PSCNT17	PSCNT16	xxxx x000	xxxx x000
811h	BORCON	SBOREN	—	—	—	—	—	—	BORRDY	1--- ---q	u--- ---u
812h	VREGCON	—	—	—	—	—	—	VREGPM(1)	—	---- --0-	---- --0-
813h	PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	0011 110q	qqqq qquu
814h	PCON1	—	—	—	—	—	—	$\overline{\text{MEMV}}$	—	---- --1-	---- --u-
815h	—	Unimplemented								—	—
816h	—	Unimplemented								—	—
817h	—	Unimplemented								—	—
818h	—	Unimplemented								—	—
819h	—	Unimplemented								—	—
81Ah	NVMADRL	NVMADR<7:0>								xxxx xxxx	uuuu uuuu
81Bh	NVMADRH	—	NVMADR<14:8>							-xxx xxxx	-uuu uuuu
81Ch	NVMDATL	NVMDAT<7:0>								0000 0000	0000 0000
81Dh	NVMDATH	—	—	NVMDAT<13:8>						--00 0000	--00 0000
81Eh	NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	-000 x000	-000 q000
81Fh	NVMCON2	NVMCON2<7:0>								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Present only on PIC16F15356/75/76/85/86.

5.0 DEVICE CONFIGURATION

Device configuration consists of the Configuration Words, User ID, Device ID, Device Information Area (DIA), (see **Section 6.0 "Device Information Area"**), and the Device Configuration Information (DCI) regions, (see **Section 7.0 "Device Configuration Information"**).

5.1 Configuration Words

The devices have several Configuration Words starting at address 8007h. The Configuration bits establish configuration values prior to the execution of any software; Configuration bits enable or disable device-specific features.

In terms of programming, these important Configuration bits should be considered:

1. LVP: Low-Voltage Programming Enable bit

- 1 = ON – Low-Voltage Programming is enabled. $\overline{MCLR}$/V_{PP} pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
- 0 = OFF – HV on $\overline{MCLR}$/V_{PP} must be used for programming.

2. CP: User Nonvolatile Memory (NVM) Program Memory Code Protection bit

- 1 = OFF – User NVM code protection disabled
- 0 = ON – User NVM code protection enabled

REGISTER 9-7: OSCTUNE: HFINTOSC TUNING REGISTER

U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	HFTUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5-0 **HFTUN<5:0>:** HFINTOSC Frequency Tuning bits

```
01 1111 = Maximum frequency
01 1110 =
•••
00 0001 =
00 0000 = Center frequency. Oscillator module is running at the calibrated frequency (default value).
11 1111 =
•••
10 0001 =
10 0000 = Minimum frequency.
```

REGISTER 10-14: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	—	—	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS = Hardware set

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **TRM2IF:** Timer2 Interrupt Flag bit
1 = The TMR2 postscaler overflowed, or in 1:1 mode, a TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 event has occurred

bit 0 **TRM1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 overflow occurred (must be cleared in software)
0 = No Timer1 overflow occurred

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-15: PIR5: PERIPHERAL INTERRUPT REQUEST REGISTER 5

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0
CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CLC4IF:** CLC4 Interrupt Flag bit
1 = A CLC4OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC4 interrupt event has occurred

bit 6 **CLC3IF:** CLC3 Interrupt Flag bit
1 = A CLC3OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC3 interrupt event has occurred

bit 5 **CLC2IF:** CLC2 Interrupt Flag bit
1 = A CLC2OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC2 interrupt event has occurred

bit 4 **CLC1IF:** CLC1 Interrupt Flag bit
1 = A CLC1OUT interrupt condition has occurred (must be cleared in software)
0 = No CLC1 interrupt event has occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = The Timer1 Gate has gone inactive (the acquisition is complete)
0 = The Timer1 Gate has not gone inactive

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 14-37: WPUE: WEAK PULL-UP PORTE REGISTER

U-0	U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	—	WPUE3(2)	WPUE2(1)	WPUE1(1)	WPUE0(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WPUE<3:0>:** Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Present on PIC16(L)F15375/76/85/86 only.
2: If MCLRE = 1, the weak pull-up in RE3 is always enabled; bit WPUE3 is not affected.
3: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 14-38: ODCONE: PORTE OPEN-DRAIN CONTROL REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	ODCE2	ODCE1	ODCE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ODCE<3:0>:** PORTE Open-Drain Enable bits
For RE<3:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

Note 1: Present on PIC16(L)F15375/76/85/86 only.

REGISTER 16-6: PMD5 – PMD CONTROL REGISTER 5

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
—	—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **CLC4MD:** Disable CLC4 bit
1 = CLC4 module disabled
0 = CLC4 module enabled

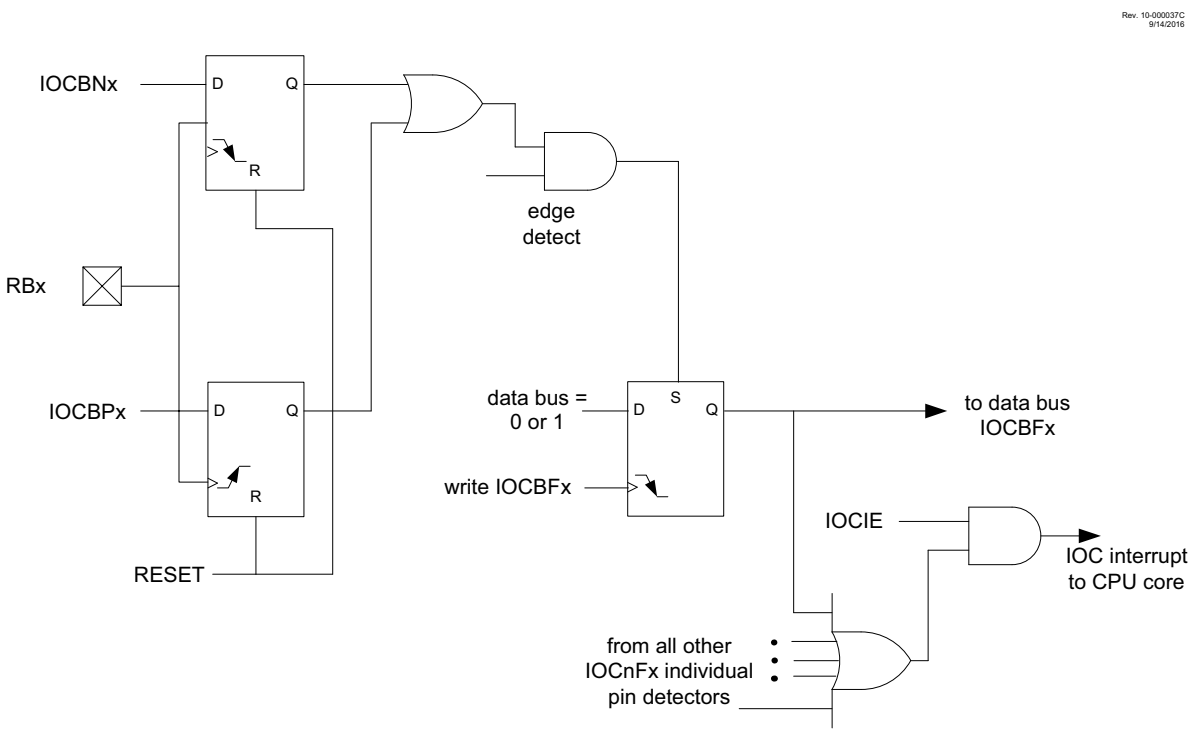
bit 3 **CLC3MD:** Disable CLC3 bit
1 = CLC3 module disabled
0 = CLC3 module enabled

bit 2 **CLC2MD:** Disable CLC2 bit
1 = CLC2 module disabled
0 = CLC2 module enabled

bit 1 **CLC1MD:** Disable CLC bit
1 = CLC1 module disabled
0 = CLC1 module enabled

bit 0 **Unimplemented**: Read as ‘0’

FIGURE 17-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTB EXAMPLE)



Note 1: See Table 8-1 for BOR Active Conditions.

TABLE 22-1: SUMMARY OF REGISTERS ASSOCIATED WITH NCO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	146
PIR7	—	—	NVMIF	NCO1IF	—	—	—	CWG1IF	162
PIE7	—	—	NVMIE	NCO1IE	—	—	—	CWG1IE	154
NCO1CON	N1EN	—	N1OUT	N1POL	—	—	—	N1PFM	294
NCO1CLK	N1PWS<2:0>			—	N1CKS<3:0>				295
NCO1ACCL	NCO1ACC<7:0>								296
NCO1ACCH	NCO1ACC<15:8>								296
NCO1ACCU	—	—	—	—	NCO1ACC<19:16>				296
NCO1INCL	NCO1INC<7:0>								297
NCO1INCH	NCO1INC<15:8>								297
NCO1INCU	—	—	—	—	NCO1AINC<19:16>				297
RxyPPS	—	—	—	RxyPPS<4:0>					242

Legend: – = unimplemented read as '0'. Shaded cells are not used for NCO module.

24.9 Register Definitions: ZCD Control

REGISTER 24-1: ZCDCON: ZERO-CROSS DETECTION CONTROL REGISTER

R/W-q/q	U-0	R-x/x	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
SEN	—	OUT	POL	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on Configuration bits

bit 7 **SEN**: Zero-Cross Detection Enable bit
1 = Zero-cross detect is enabled. ZCD pin is forced to output to source and sink current.
0 = Zero-cross detect is disabled. ZCD pin operates according to PPS and TRIS controls.

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Zero-Cross Detection Logic Level bit
POL bit = 1:
1 = ZCD pin is sourcing current
0 = ZCD pin is sinking current
POL bit = 0:
1 = ZCD pin is sinking current
0 = ZCD pin is sourcing current

bit 4 **POL:** Zero-Cross Detection Logic Output Polarity bit
1 = ZCD logic output is inverted
0 = ZCD logic output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **INTP:** Zero-Cross Positive Edge Interrupt Enable bit
1 = ZCDIF bit is set on low-to-high ZCDx_output transition
0 = ZCDIF bit is unaffected by low-to-high ZCDx_output transition

bit 0 **INTN:** Zero-Cross Negative Edge Interrupt Enable bit
1 = ZCDIF bit is set on high-to-low ZCDx_output transition
0 = ZCDIF bit is unaffected by high-to-low ZCDx_output transition

TABLE 24-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE ZCD MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	150
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	158
ZCDxCON	EN	—	OUT	POL	—	—	INTP	INTN	314

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the ZCD module.

TABLE 24-2: SUMMARY OF CONFIGURATION WORD WITH THE ZCD MODULE

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG2	13:8	—	—	$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	—	103
	7:0	BOREN <1:0>		$\overline{\text{LPBOREN}}$	—	—	—	$\overline{\text{PWRTE}}$	MCLRE	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the ZCD module.

REGISTER 25-1: T0CON0: TIMER0 CONTROL REGISTER 0

R/W-0/0	U-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **T0EN:** Timer0 Enable bit
1 = The module is enabled and operating
0 = The module is disabled and in the lowest power mode

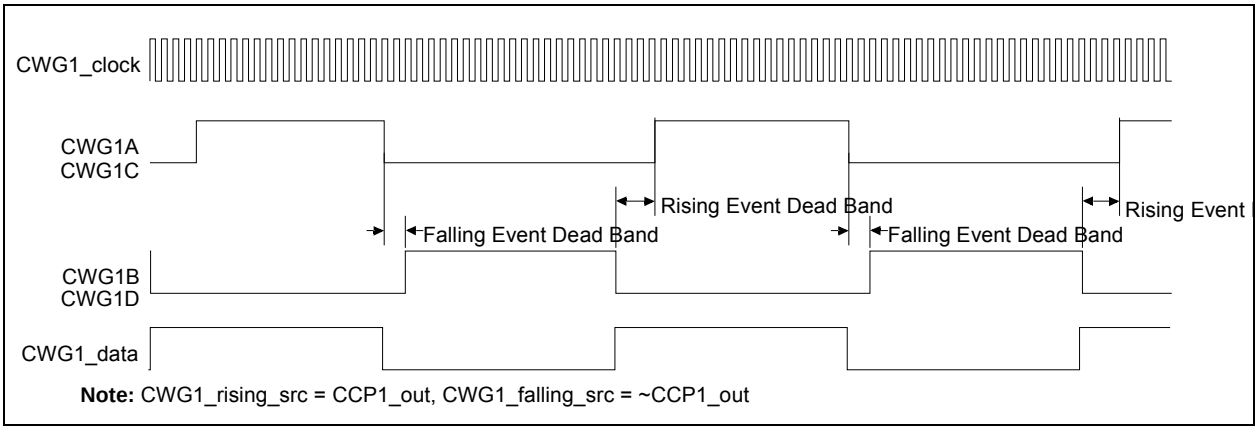
bit 6 **Unimplemented:** Read as ‘0’

bit 5 **T0OUT:** Timer0 Output bit (read-only)
Timer0 output bit

bit 4 **T016BIT:** Timer0 Operating as 16-bit Timer Select bit
1 = Timer0 is a 16-bit timer
0 = Timer0 is an 8-bit timer

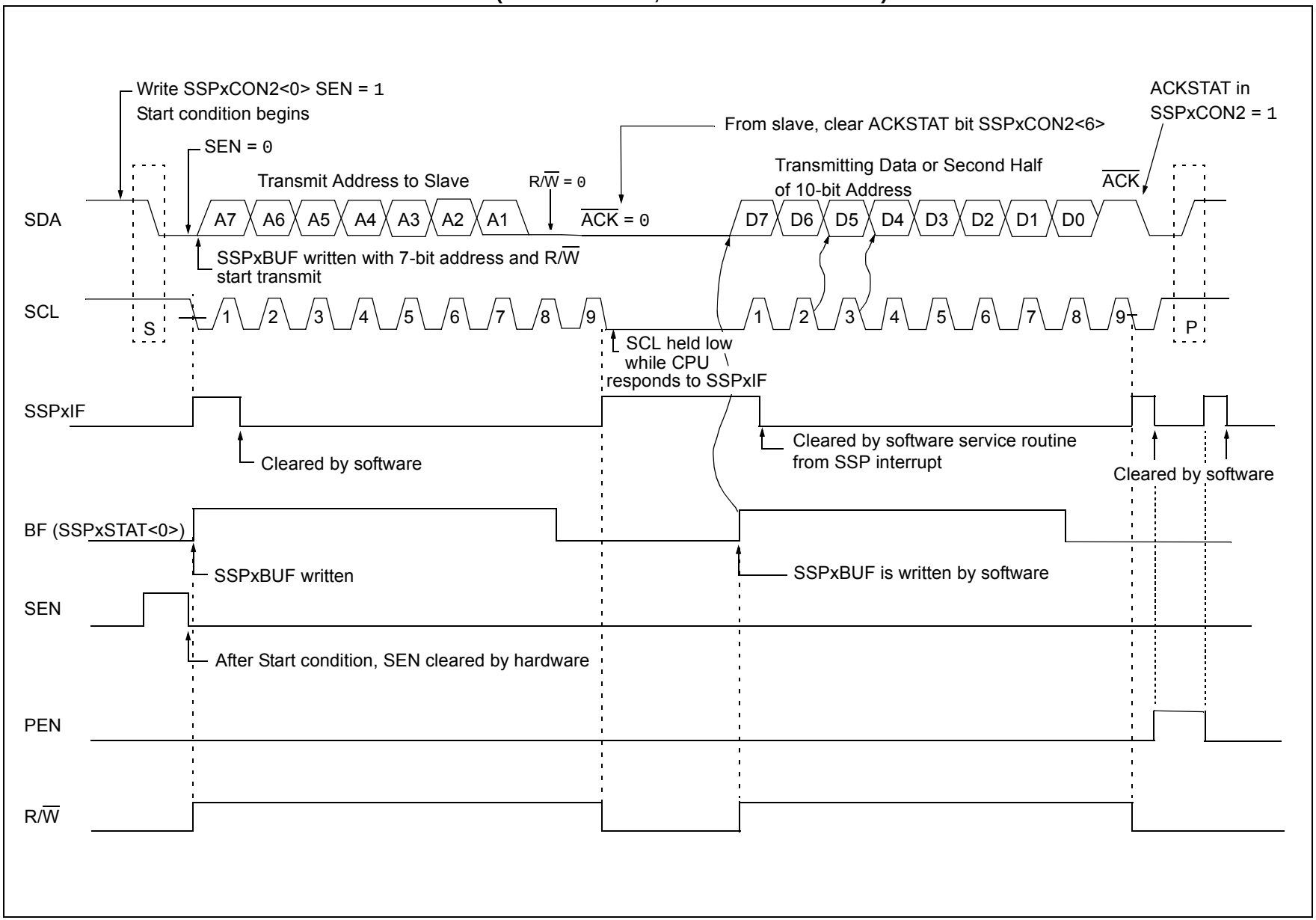
bit 3-0 **T0OUTPS<3:0>:** Timer0 output postscaler (divider) select bits
1111 = 1:16 Postscaler
1110 = 1:15 Postscaler
1101 = 1:14 Postscaler
1100 = 1:13 Postscaler
1011 = 1:12 Postscaler
1010 = 1:11 Postscaler
1001 = 1:10 Postscaler
1000 = 1:9 Postscaler
0111 = 1:8 Postscaler
0110 = 1:7 Postscaler
0101 = 1:6 Postscaler
0100 = 1:5 Postscaler
0011 = 1:4 Postscaler
0010 = 1:3 Postscaler
0001 = 1:2 Postscaler
0000 = 1:1 Postscaler

FIGURE 30-9: CWG HALF-BRIDGE MODE OPERATION



Note: CWG1_rising_src = CCP1_out, CWG1_falling_src = ~CCP1_out

FIGURE 32-28: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



32.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 32-33).

b) SCL is sampled low before SDA is asserted low (Figure 32-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the Start condition is aborted,
- the BCL1IF flag is set and
- the MSSP module is reset to its Idle state (Figure 32-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 32-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note:	The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 32-33: BUS COLLISION DURING START CONDITION (SDA ONLY)

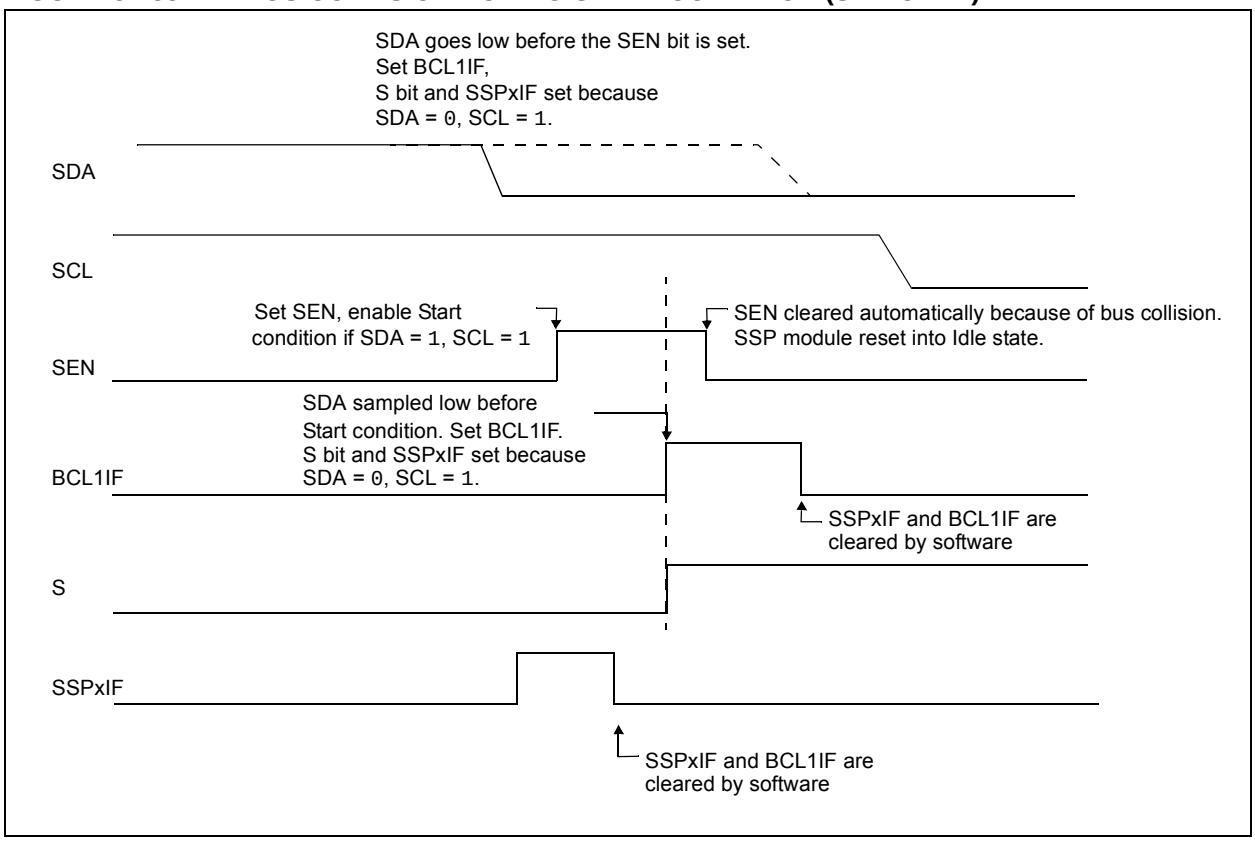
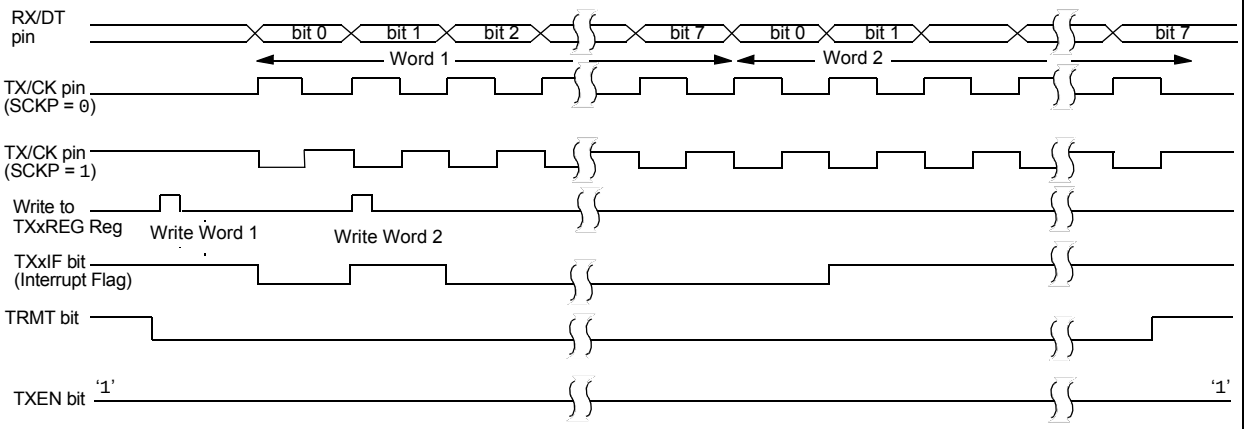
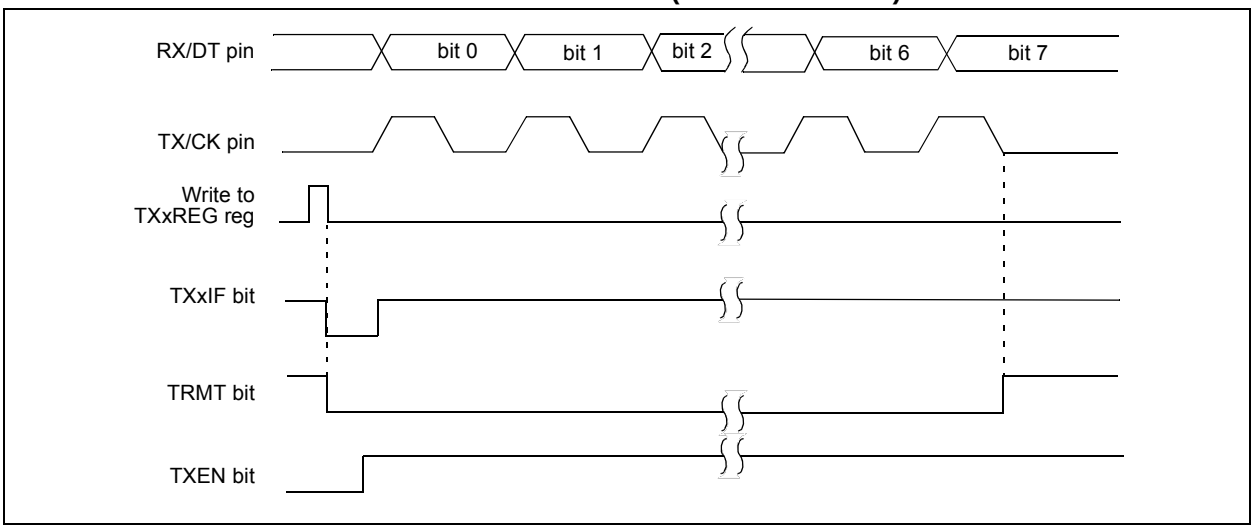


FIGURE 33-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPxBRGL = 0, continuous transmission of two 8-bit words.

FIGURE 33-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



33.4.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCxSTA register) or the Continuous Receive Enable bit (CREN of the RCxSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RXxIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCxREG. The RXxIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

35.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}/V_{PP}$
- V_{DD}
- V_{SS}

In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC16(L)F153XX Memory Programming Specification***"** (DS40001838).

35.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{MCLR}/V_{PP}$ to V_{IHH}.

35.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using V_{DD} only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

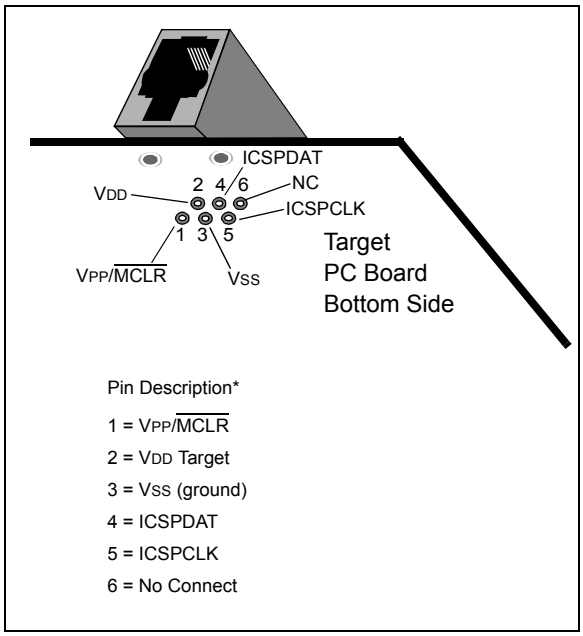
Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 8.5"MCLR"** for more information.

35.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 35-1.

FIGURE 35-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 35-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 35-3 for more information.

BCF **Bit Clear f**

Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BRA **Relative Branch**

Syntax:	[*label*] BRA label [*label*] BRA $+k
Operands:	-256 ≤ label - PC + 1 ≤ 255 -256 ≤ k ≤ 255
Operation:	(PC) + 1 + k → PC
Status Affected:	None
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + k. This instruction is a 2-cycle instruction. This branch has a limited range.

BRW **Relative Branch with W**

Syntax:	[*label*] BRW
Operands:	None
Operation:	(PC) + (W) → PC
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + (W). This instruction is a 2-cycle instruction.

BSF **Bit Set f**

Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC **Bit Test f, Skip if Clear**

Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS **Bit Test f, Skip if Set**

Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

RETLW **Return with literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

Words: 1

Cycles: 2

Example:

```
CALL TABLE;W contains table
    ;offset value
•   ;W now has table value
•
•
ADDWF PC  ;W = offset
RETLW k1  ;Begin table
RETLW k2  ;
•
•
•
RETLW kn  ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: $TOS \rightarrow PC$

Status Affected: None

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

RLF **Rotate Left f through Carry**

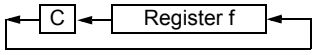
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0
After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

RRF **Rotate Right f through Carry**

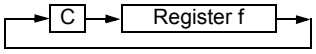
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

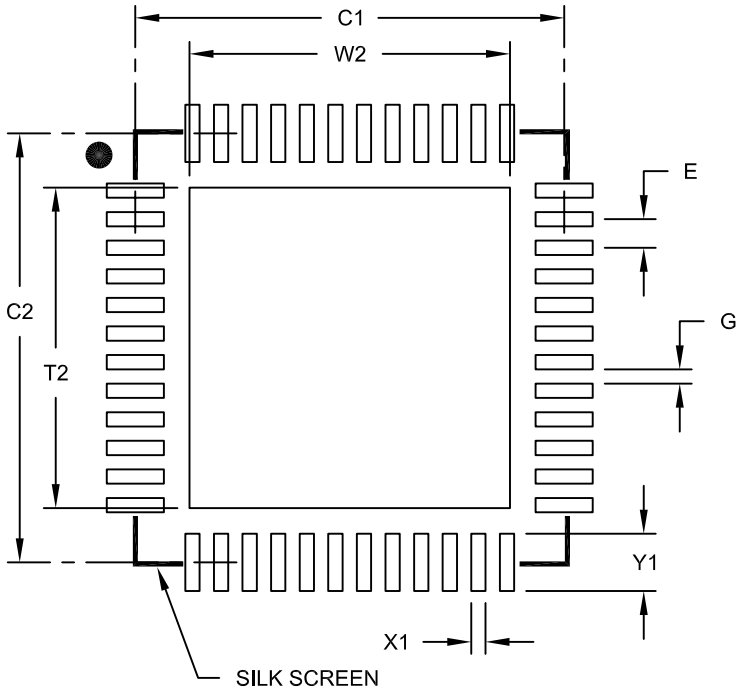
Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A