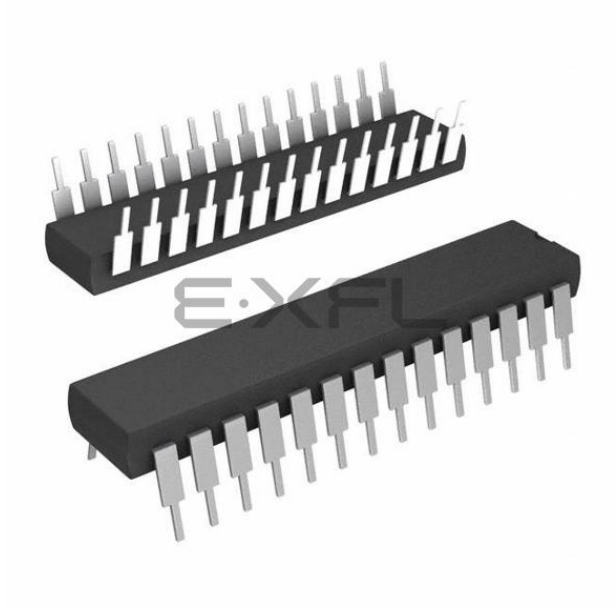

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15356-e-sp

TABLE 4-5: PIC16(L)F15356/75/76/85/86 MEMORY MAP, BANKS 8-15

	BANK 8	BANK 9	BANK 10	BANK 11	BANK 12	BANK 13	BANK 14	BANK 15
400h	Core Register (Table 4-3)							
40Bh								
40Ch	—	—	—	NCO1ACCL	CWG1CLK	—	PIR0	—
40Dh	—	—	—	NCO1ACCH	CWG1DAT	—	PIR1	—
40Eh	—	—	—	NCO1ACCU	CWG1DBR	—	PIR2	—
40Fh	—	—	—	NCO1INCL	CWG1DBF	—	PIR3	—
410h	—	—	—	NCO1INCH	CWG1CON0	—	PIR4	—
411h	—	—	—	NCO1INCU	CWG1CON1	—	PIR5	—
412h	—	—	—	NCO1CON	CWG1AS0	—	PIR6	—
413h	—	—	—	NCO1CLK	CWG1AS1	—	PIR7	—
414h	—	—	—	—	CWG1STR	—	—	—
415h	—	—	—	—	—	—	—	—
416h	—	—	—	—	—	—	PIE0	PMD0
417h	—	—	—	—	—	—	PIE1	PMD1
418h	—	—	—	—	—	—	PIE2	PMD2
419h	—	—	—	—	—	—	PIE3	PMD3
41Ah	—	—	—	—	—	—	PIE4	PMD4
41Bh	—	—	—	—	—	—	PIE5	PMD5
41Ch	—	—	—	TMR0	—	—	PIE6	—
41Dh	—	—	—	PR0	—	—	PIE7	—
41Eh	—	—	—	TMR0CON0	—	—	—	—
41Fh	—	—	—	TMR0CON1	—	—	—	—
420h	General Purpose Register 80 Bytes				General Purpose Register 48 Bytes			
46Fh								
470h	Common RAM Accesses 70h-7Fh							
47Fh								
480h		Core Register (Table 4-3)						
48Bh								
48Ch		—	—	—	—	—	—	—
48Dh		—	—	—	—	—	—	—
48Eh		—	—	—	—	—	—	—
48Fh		—	—	—	—	—	—	—
490h		—	—	—	—	—	—	—
491h		—	—	—	—	—	—	—
492h		—	—	—	—	—	—	—
493h		—	—	—	—	—	—	—
494h		—	—	—	—	—	—	—
495h		—	—	—	—	—	—	—
496h		—	—	—	—	—	—	—
497h		—	—	—	—	—	—	—
498h		—	—	—	—	—	—	—
499h		—	—	—	—	—	—	—
49Ah		—	—	—	—	—	—	—
49Bh		—	—	—	—	—	—	—
49Ch		—	—	—	—	—	—	—
49Dh		—	—	—	—	—	—	—
49Eh		—	—	—	—	—	—	—
49Fh		—	—	—	—	—	—	—
4A0h		General Purpose Register 80 Bytes						
4EFh								
4F0h		Common RAM Accesses 70h-7Fh						
4FFh								
500h			Core Register (Table 4-3)					
50Bh								
50Ch			—	—	—	—	—	—
50Dh			—	—	—	—	—	—
50Eh			—	—	—	—	—	—
50Fh			—	—	—	—	—	—
510h			—	—	—	—	—	—
511h			—	—	—	—	—	—
512h			—	—	—	—	—	—
513h			—	—	—	—	—	—
514h			—	—	—	—	—	—
515h			—	—	—	—	—	—
516h			—	—	—	—	—	—
517h			—	—	—	—	—	—
518h			—	—	—	—	—	—
519h			—	—	—	—	—	—
51Ah			—	—	—	—	—	—
51Bh			—	—	—	—	—	—
51Ch			—	—	—	—	—	—
51Dh			—	—	—	—	—	—
51Eh			—	—	—	—	—	—
51Fh			—	—	—	—	—	—
520h			General Purpose Register 80 Bytes					
56Fh								
570h			Common RAM Accesses 70h-7Fh					
57Fh								
580h				Core Register (Table 4-3)				
58Bh								
58Ch				—	—	—	—	—
58Dh				—	—	—	—	—
58Eh				—	—	—	—	—
58Fh				—	—	—	—	—
590h				—	—	—	—	—
591h				—	—	—	—	—
592h				—	—	—	—	—
593h				—	—	—	—	—
594h				—	—	—	—	—
595h				—	—	—	—	—
596h				—	—	—	—	—
597h				—	—	—	—	—
598h				—	—	—	—	—
599h				—	—	—	—	—
59Ah				—	—	—	—	—
59Bh				—	—	—	—	—
59Ch				TMR0	—	—	—	—
59Dh				PR0	—	—	—	—
59Eh				TMR0CON0	—	—	—	—
59Fh				TMR0CON1	—	—	—	—
5A0h				General Purpose Register 80 Bytes				
5EFh								
5F0h				Common RAM Accesses 70h-7Fh				
5FFh								
600h					Core Register (Table 4-3)			
60Bh								
60Ch					CWG1CLK	—	PIR0	—
60Dh					CWG1DAT	—	PIR1	—
60Eh					CWG1DBR	—	PIR2	—
60Fh					CWG1DBF	—	PIR3	—
610h					CWG1CON0	—	PIR4	—
611h					CWG1CON1	—	PIR5	—
612h					CWG1AS0	—	PIR6	—
613h					CWG1AS1	—	PIR7	—
614h					CWG1STR	—	—	—
615h					—	—	—	—
616h					—	—	PIE0	PMD0
617h					—	—	PIE1	PMD1
618h					—	—	PIE2	PMD2
619h					—	—	PIE3	PMD3
61Ah					—	—	PIE4	PMD4
61Bh					—	—	PIE5	PMD5
61Ch					—	—	PIE6	—
61Dh					—	—	PIE7	—
61Eh					—	—	—	—
61Fh					—	—	—	—
620h					General Purpose Register 48 Bytes			
64Fh								
650h					General Purpose Register 32 Bytes(2)			
66Fh								
670h					Common RAM Accesses 70h-7Fh			
67Fh								
680h						Core Register (Table 4-3)		
68Bh								
68Ch						—	PIR0	—
68Dh						—	PIR1	—
68Eh						—	PIR2	—
68Fh						—	PIR3	—
690h						—	PIR4	—
691h						—	PIR5	—
692h						—	PIR6	—
693h						—	PIR7	—
694h						—	—	—
695h						—	—	—
696h						—	PIE0	PMD0
697h						—	PIE1	PMD1
698h						—	PIE2	PMD2
699h						—	PIE3	PMD3
69Ah						—	PIE4	PMD4
69Bh						—	PIE5	PMD5
69Ch						—	PIE6	—
69Dh						—	PIE7	—
69Eh						—	—	—
69Fh						—	—	—
6A0h						General Purpose Register 80 Bytes(2)		
6EFh								
6F0h						Common RAM Accesses 70h-7Fh		
6FFh								
700h							Core Register (Table 4-3)	
70Bh								
70Ch							PIR0	—
70Dh							PIR1	—
70Eh							PIR2	—
70Fh							PIR3	—
710h							PIR4	—
711h							PIR5	—
712h							PIR6	—
713h							PIR7	—
714h							—	—
715h							—	—
716h							PIE0	PMD0
717h							PIE1	PMD1
718h							PIE2	PMD2
719h							PIE3	PMD3
71Ah							PIE4	PMD4
71Bh							PIE5	PMD5
71Ch							PIE6	—
71Dh							PIE7	—
71Eh							—	—
71Fh							—	—
720h							General Purpose Register 80 Bytes(2)	
76Fh								
770h							Common RAM Accesses 70h-7Fh	
77Fh								
780h								Core Register (Table 4-3)
78Bh								
78Ch								—
78Dh								—
78Eh								—
78Fh								—
790h								—
791h								—
792h								—
793h								—
794h								—
795h								—
796h								PMD0
797h								PMD1
798h								PMD2
799h								PMD3
79Ah								PMD4
79Bh								PMD5
79Ch								—
79Dh								—
79Eh								—
79Fh								—
7A0h								General Purpose Register 80 Bytes(2)
7EFh								
7F0h								Common RAM Accesses 70h-7Fh
7FFh								

Note 1: Unimplemented locations read as '0'.

2: Present only on PIC16(L)F15356/76/86.

TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 5											
CPU CORE REGISTERS; see Table 4-3 for specifics											
28Ch	T2TMR	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
28Dh	T2PR	TMR2 Period Register								1111 1111	1111 1111
28Eh	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
290h	T2CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
291h	T2RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
292h — 29Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

5.6 Device ID and Revision ID

The 14-bit Device ID word is located at 8006h and the 14-bit Revision ID is located at 8005h. These locations are read-only and cannot be erased or modified.

Development tools, such as device programmers and debuggers, may be used to read the Device ID, Revision ID and Configuration Words. These locations can also be read from the NVMCON register.

5.7 Register Definitions: Device and Revision

REGISTER 5-6: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

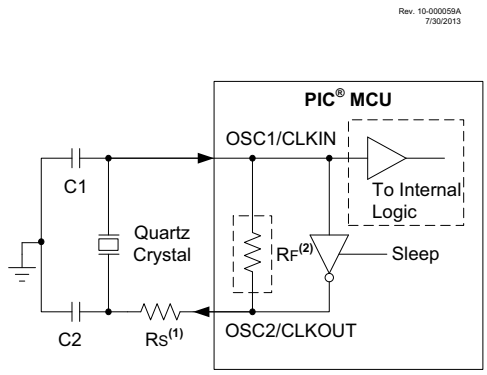
R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	
'1' = Bit is set	'0' = Bit is cleared

bit 13-0 **DEV<13:0>:** Device ID bits

Device	DEVID<13:0> Values
PIC16F15356	11 0000 1011 0000 (30B0h)
PIC16LF15356	11 0000 1011 0001 (30B1h)
PIC16F15375	11 0000 1011 0010 (30B2h)
PIC16LF15375	11 0000 1011 0011 (30B3h)
PIC16F15376	11 0000 1011 0100 (30B4h)
PIC16LF15376	11 0000 1011 0101 (30B5h)
PIC16F15385	11 0000 1011 0110 (30B6h)
PIC16LF15385	11 0000 1011 0111 (30B7h)
PIC16F15386	11 0000 1011 1000 (30B8h)
PIC16LF15386	11 0000 1011 1001 (30B9h)

FIGURE 9-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (Rs) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ and 10 MΩ).

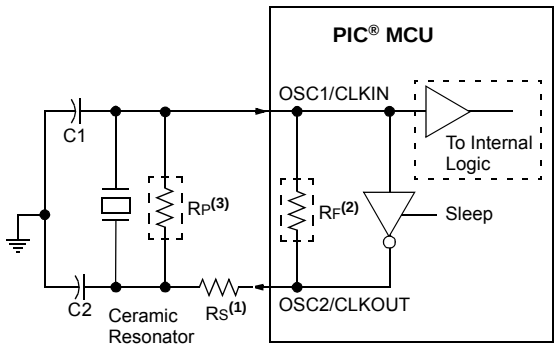
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Application Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 9-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

9.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), Brown-out Reset (BOR) or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

9.5 Register Definitions: Oscillator Control

REGISTER 9-1: OSCCON1: OSCILLATOR CONTROL REGISTER1

U-0	R/W-f/f(1)	R/W-f/f(1)	R/W-f/f(1)	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q
—	NOSC<2:0>(2,3)			NDIV<3:0>(2,3,4)			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	f = determined by fuse setting

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **NOSC<2:0>:** New Oscillator Source Request bits
The setting requests a source oscillator and PLL combination per Table 9-1.
POR value = RSTOSC (Register 5-1).

bit 3-0 **NDIV<3:0>:** New Divider Selection Request bits
The setting determines the new postscaler division ratio per Table 9-1.

Note 1: The default value (f/f) is set equal to the RSTOSC Configuration bits.
2: If NOSC is written with a reserved value (Table 9-1), the operation is ignored and neither NOSC nor NDIV is written.
3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.
4: When NOSC = 110 (HFINTOSC 4 MHz), the NDIV bits will default to ‘0010’ upon Reset; for all other NOSC settings the NDIV bits will default to ‘0000’ upon Reset.

REGISTER 9-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2

U-0	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)	R-n/n(2)
—	COSC<2:0>			CDIV<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **COSC<2:0>:** Current Oscillator Source Select bits (read-only)
Indicates the current source oscillator and PLL combination per Table 9-1.

bit 3-0 **CDIV<3:0>:** Current Divider Select bits (read-only)
Indicates the current postscaler division ratio per Table 9-1.

Note 1: The POR value is the value present when user code execution begins.
2: The Reset value (n/n) is the same as the NOSC/NDIV bits.

REGISTER 10-7: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **CLC4IE:** CLC4 Interrupt Enable bit
1 = CLC4 interrupt enabled
0 = CLC4 interrupt disabled

bit 6 **CLC3IE:** CLC3 Interrupt Enable bit
1 = CLC3 interrupt enabled
0 = CLC3 interrupt disabled

bit 5 **CLC2IE:** CLC2 Interrupt Enable bit
1 = CLC2 interrupt enabled
0 = CLC2 interrupt disabled

bit 4 **CLC1IE:** CLC1 Interrupt Enable bit
1 = CLC1 interrupt enabled
0 = CLC1 interrupt disabled

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE7.

REGISTER 12-3: WDTPSL: WDT PRESCALE SELECT LOW BYTE REGISTER

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PSCNT<7:0>**: Prescale Select Low Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 12-4: WDTPSH: WDT PRESCALE SELECT HIGH BYTE REGISTER

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
PSCNT<15:8>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PSCNT<15:8>**: Prescale Select High Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 12-5: WDTTMR: WDT TIMER REGISTER

U-0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
—	WDTTMR<3:0>				STATE	PSCNT<17:16>(1)	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **WDTTMR<3:0>**: Watchdog Timer Value bits

bit 2 **STATE**: WDT Armed Status bit
1 = WDT is armed
0 = WDT is not armed

bit 1-0 **PSCNT<17:16>**: Prescale Select Upper Byte bits(1)

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should be read during normal operation.

REGISTER 16-5: PMD4: PMD CONTROL REGISTER 4

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
UART2MD	UART1MD	MSSP2MD	MSSP1MD	—	—	—	CWG1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **UART2MD:** Disable EUSART2 bit
1 = EUSART2 module disabled
0 = EUSART2 module enabled

bit 6 **UART1MD:** Disable EUSART1 bit
1 = EUSART1 module disabled
0 = EUSART1 module enabled

bit 5 **MSSP2MD:** Disable MSSP2 bit
1 = MSSP2 module disabled
0 = MSSP2 module enabled

bit 4 **MSSP1MD:** Disable MSSP1 bit
1 = MSSP1 module disabled
0 = MSSP1 module enabled

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **CWG1MD:** Disable CWG1 bit
1 = CWG1 module disabled
0 = CWG1 module enabled

19.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The main purpose of the temperature indicator module is to provide a temperature-dependent voltage that can be measured by the Analog-to-Digital Converter.

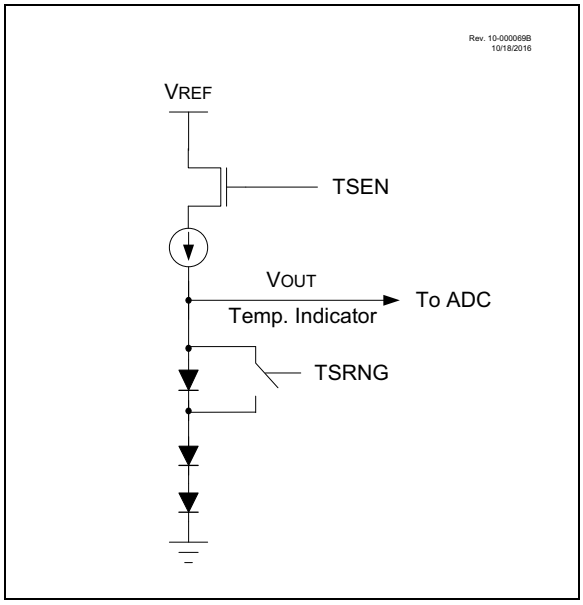
The circuit's range of operating temperature falls between -40°C and +125°C. The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately.

19.1 Module Operation

The temperature indicator module consists of a temperature-sensing circuit that provides a voltage to the device ADC. The analog voltage output, VTSENSE, varies inversely to the device temperature. The output of the temperature indicator is referred to as VOUT.

Figure 19-1 shows a simplified block diagram of the temperature indicator module.

FIGURE 19-1: TEMPERATURE INDICATOR BLOCK DIAGRAM



The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 20.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

The ON/OFF bit for the module is located in the FVRCON register. See **Section 18.0 "Fixed Voltage Reference (FVR)"** for more information. The circuit is enabled by setting the TSEN bit of the FVRCON register. When the module is disabled, the circuit draws no current.

The circuit operates in either High or Low range. Refer to **Section 19.5 "Temperature Indicator Range"** for more details on the range settings.

19.2 Estimation of Temperature

This section describes how the sensor voltage can be used to estimate the temperature of the module. To use the sensor, the output voltage, VTSENSE, is measured and the corresponding temperature is determined. Equation 19-1 provides an estimate for the die temperature based on the VTSENSE value.

EQUATION 19-1: SENSOR TEMPERATURE

$$T_{SENSE} = V_{TSENSE} \times (-Mt) + T_{OFFSET}$$

Where:
Mt = 1/Mv, where Mv = sensor voltage sensitivity (V/°C).
TOFFSET is the temperature difference between the theoretical temperature and the actual temperature.

REGISTER 23-5: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—	—	—	—	—	—	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

TABLE 23-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CMxCON0	ON	OUT	—	POL	—	—	HYS	SYNC	305
CMxCON1	—	—	—	—	—	—	INTP	INTN	306
CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	308
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		264
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	287
DAC1CON1	—	—	—	DAC1R<4:0>					287
INTCON	GIE	PEIE	—					INTEDG	146
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	149
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	157
RxyPPS	—	—	—	RxyPPS<4:0>					242
CLCINxPPS	—	—	CLCIN0PPS<5:0>						241
T1GPPS	—	—	T1GPPS<5:0>						241

Legend: — = unimplemented location, read as ‘0’. Shaded cells are unused by the comparator module.

TABLE 26-3: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	146
PIE4	—	—	—	—	—	—	TMR2IE	TMR1IE	151
PIR4	—	—	—	—	—	—	TMR2IF	TMR1IF	159
T1CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	329
T1GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	330
T1GATE	—	—	—	GSS<4:0>					332
T1CLK	—	—	—	—	CS<3:0>				331
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								321*
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								321*
T1CKIPPS	—	—	T1CKIPPS<5:0>						241
T1GPPS	—	—	T1GPPS<5:0>						241
CCPxCON	CCPxEN	CCPxOE	CCPxOUT	CCPxFMT	CCPxMODE<3:0>				366
CLCxSELy	—	—	—	LCxDyS<4:0>					412
ADACT	—	—	—	—	ADACT<3:0>				280

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the Timer1 modules.

* Page with register information.

27.5.7 EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

In Edge-Triggered Hardware Limit One-Shot modes the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge start and Reset (MODE<4:0> = 01100)
- Falling edge start and Reset (MODE<4:0> = 01101)

The timer resets and clears the ON bit when the timer value matches the PRx period value. External signal edges will have no effect until after software sets the ON bit. Figure 27-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse-width value and stay deactivated until the timer halts at the PRx period match unless an external signal edge resets the timer before the match occurs.

28.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxMODE<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR6 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 28-1 shows a simplified diagram of the capture operation.

28.1.1 CAPTURE SOURCES

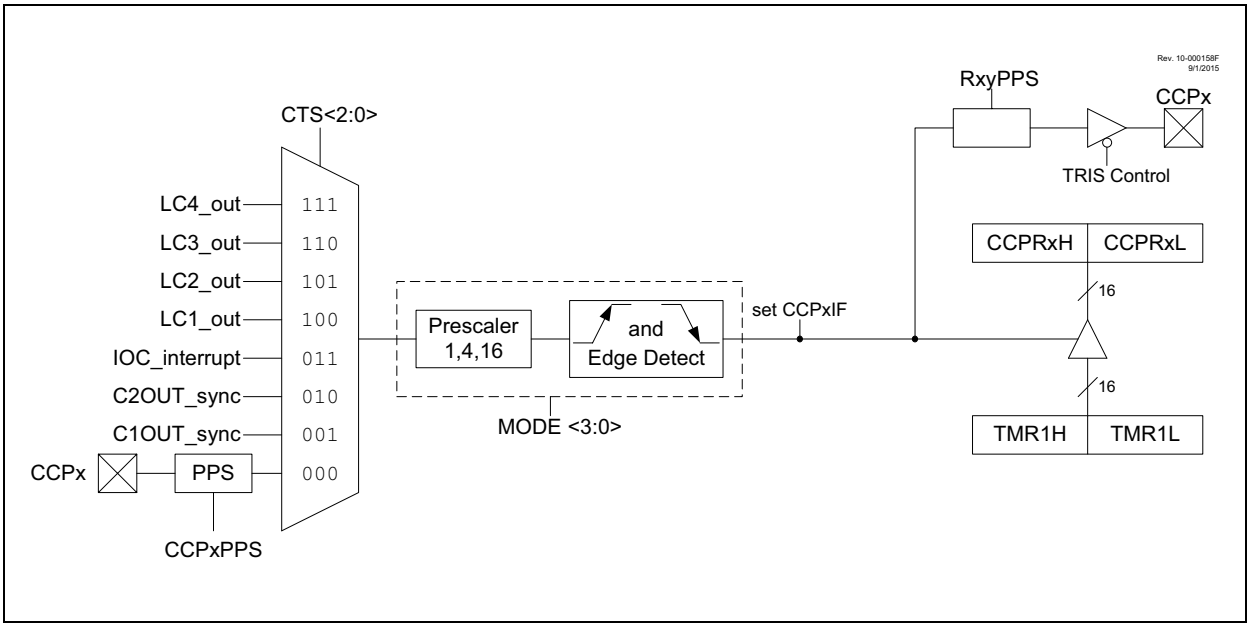
In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CCPxCTS<2:0> bits of the CCPxCAP register. The following sources can be selected:

- CCPxPPS input
- C1OUT_sync
- C2OUT_sync
- IOC_interrupt
- LC1_out
- LC2_out
- LC3_out
- LC4_out

FIGURE 28-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



REGISTER 30-5: CWG1AS0: CWG1 AUTO-SHUTDOWN CONTROL REGISTER 0

R/W/HS-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	U-0	U-0
SHUTDOWN(1, 2)	REN	LSBD<1:0>		LSAC<1:0>		—	—
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SHUTDOWN:** Auto-Shutdown Event Status bit(1, 2)
- 1 = An Auto-Shutdown state is in effect
- 0 = No Auto-shutdown event has occurred

bit 6 **REN:** Auto-Restart Enable bit
- 1 = Auto-restart enabled
- 0 = Auto-restart disabled

bit 5-4 **LSBD<1:0>:** CWG1B and CWG1D Auto-Shutdown State Control bits
- 11 =A logic '1' is placed on CWG1B/D when an auto-shutdown event is present
- 10 =A logic '0' is placed on CWG1B/D when an auto-shutdown event is present
- 01 =Pin is tri-stated on CWG1B/D when an auto-shutdown event is present
- 00 =The inactive state of the pin, including polarity, is placed on CWG1B/D after the required dead-band interval

bit 3-2 **LSAC<1:0>:** CWG1A and CWG1C Auto-Shutdown State Control bits
- 11 =A logic '1' is placed on CWG1A/C when an auto-shutdown event is present
- 10 =A logic '0' is placed on CWG1A/C when an auto-shutdown event is present
- 01 =Pin is tri-stated on CWG1A/C when an auto-shutdown event is present
- 00 =The inactive state of the pin, including polarity, is placed on CWG1A/C after the required dead-band interval

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit may be written while EN = 0 (CWG1CON0 register) to place the outputs into the shutdown configuration.

2: The outputs will remain in auto-shutdown state until the next rising edge of the input signal after this bit is cleared.

32.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 32-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPxSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and Status bits appropriately set).

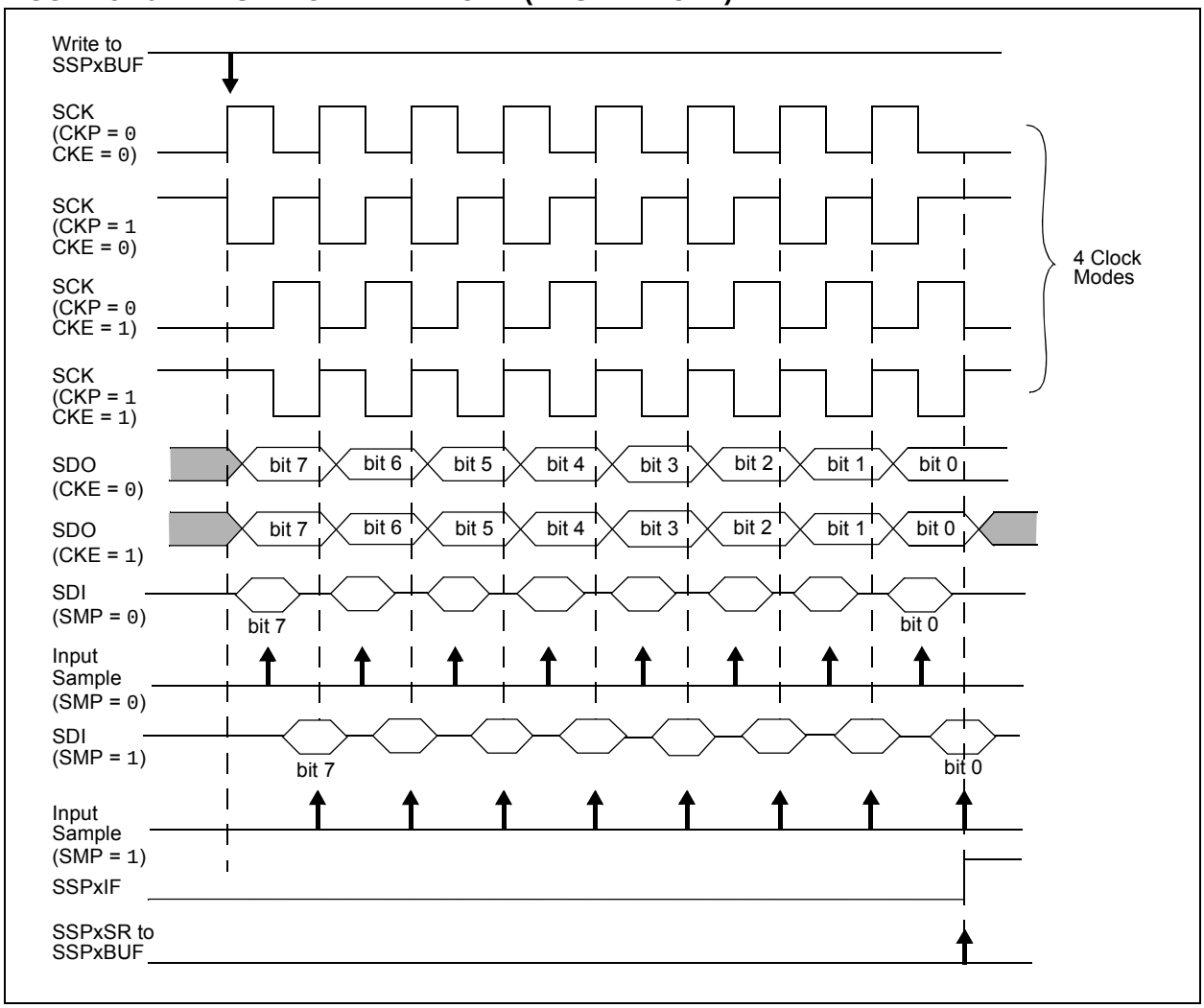
The clock polarity is selected by appropriately programming the CKP bit of the SSPxCON1 register and the CKE bit of the SSPxSTAT register. This then, would give waveforms for SPI communication as shown in Figure 32-6, Figure 32-8, Figure 32-9 and Figure 32-10, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 * TCY)
- FOSC/64 (or 16 * TCY)
- Timer2 output/2
- FOSC/(4 * (SSPxADD + 1))

Figure 32-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

FIGURE 32-6: SPI MODE WAVEFORM (MASTER MODE)



32.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allows time for the slave software to decide whether it wants to $\overline{ACK}$ the receive address or data byte.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 32-16 displays a module using both address and data holding. Figure 32-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with R/$\overline{W}$ bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the $\overline{ACK}$.
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets $\overline{ACK}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an $\overline{ACK}$, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the $\overline{ACK}$.
10. Slave clears SSPxIF.

Note:	SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{ACK}$ = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSPxSTAT register.

32.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time if an address match occurred, or if data was received properly. The status of $\overline{ACK}$ is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCL low and SDA unchanged (Figure 32-28).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/$\overline{W}$ bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the $\overline{ACK}$ bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCL low and allowing SDA to float.

32.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPxSTAT register is set when the CPU writes to SSPxBUF and is cleared when all eight bits are shifted out.

32.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

32.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPxCON2 register is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0) and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

32.6.6.4 Typical transmit sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPxBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
7. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
9. The user loads the SSPxBUF with eight bits of data.
10. Data is shifted out the SDA pin until all eight bits are transmitted.
11. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPxCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

TABLE 37-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
RST01*	TMCLR	$\overline{\text{MCLR}}$ Pulse Width Low to ensure Reset	2	—	—	µs	
RST02*	TIOZ	I/O high-impedance from Reset detection	—	—	2	µs	
RST03	TWDT	Watchdog Timer Time-out Period	—	16	—	ms	16 ms Nominal Reset Time
RST04*	TPWRT	Power-up Timer Period	—	65	—	ms	
RST05	TOST	Oscillator Start-up Timer Period(1,2)	—	1024	—	TOSC	
RST06	VBOR	Brown-out Reset Voltage(4)	2.55 2.30 1.80	2.70 2.45 1.90	2.85 2.60 2.05	V V V	BORV = 0 BORV = 1 (F devices) BORV = 1 (LF devices)
RST07	VBORHYS	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	TBORDC	Brown-out Reset Response Time	—	3	—	µs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	1.8	1.9	2.2	V	LF Devices Only

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

2: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 37-12: ANALOG-TO-DIGITAL CONVERTER (ADC) ACCURACY SPECIFICATIONS(1,2):

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD03	EDL	Differential Error	—	±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD04	EOFF	Offset Error	—	0.5	2.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD05	EGN	Gain Error	—	±0.2	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD06	VADREF	ADC Reference Voltage (ADREF+ - ADREF-)	1.8	—	VDD	V	
AD07	VAIN	Full-Scale Range	ADREF-	—	ADREF+	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	10	—	kΩ	
AD09	RVREF	ADC Voltage Reference Ladder Impedance	—	50	—	kΩ	**Note 3**

* These parameters are characterized but not tested.

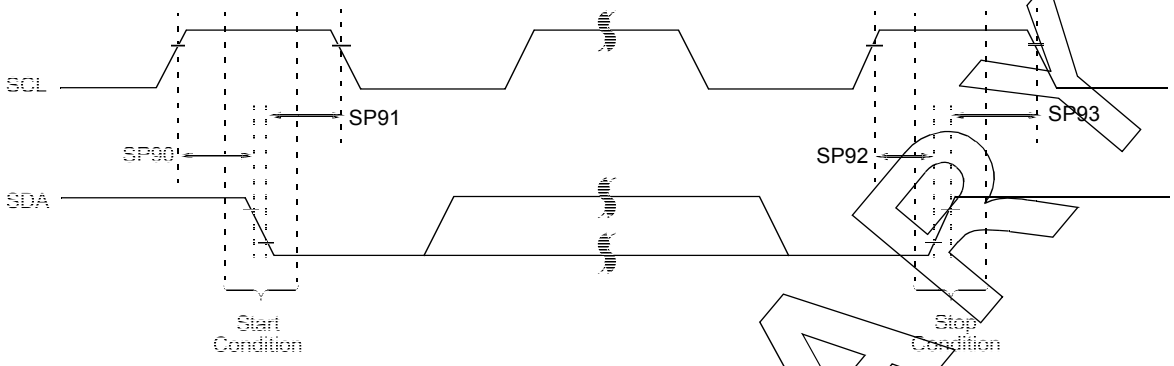
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.

2: The ADC conversion result never decreases with an increase in the input and has no missing codes.

3: This is the impedance seen by the VREF pads when the external reference pads are selected.

FIGURE 37-21: I²C BUS START/STOP BITS TIMING



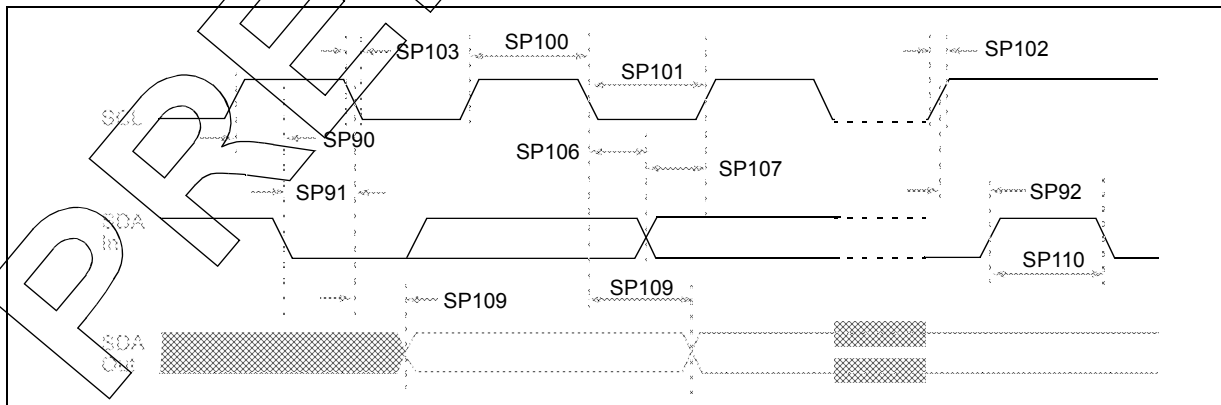
Note: Refer to Figure 37-4 for load conditions.

TABLE 37-24: I²C BUS START/STOP BITS REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
SP90*	TSU:STA	Start condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition Hold time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

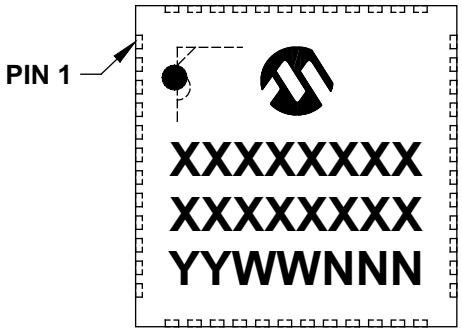
FIGURE 37-22: I²C BUS DATA TIMING



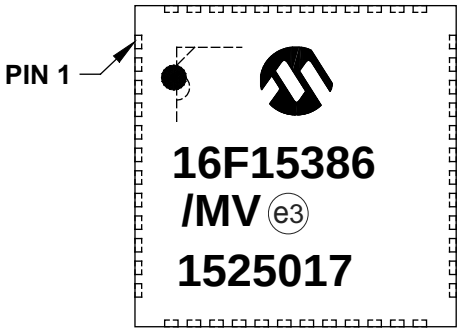
Note: Refer to Figure 37-4 for load conditions.

40.1 Package Marking Information (Continued)

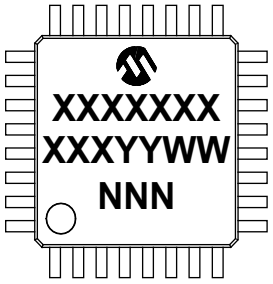
48-Lead UQFN (6x6x0.5 mm)



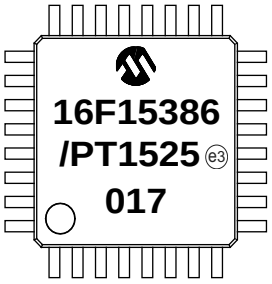
Example



48-Lead TQFP (7x7x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.