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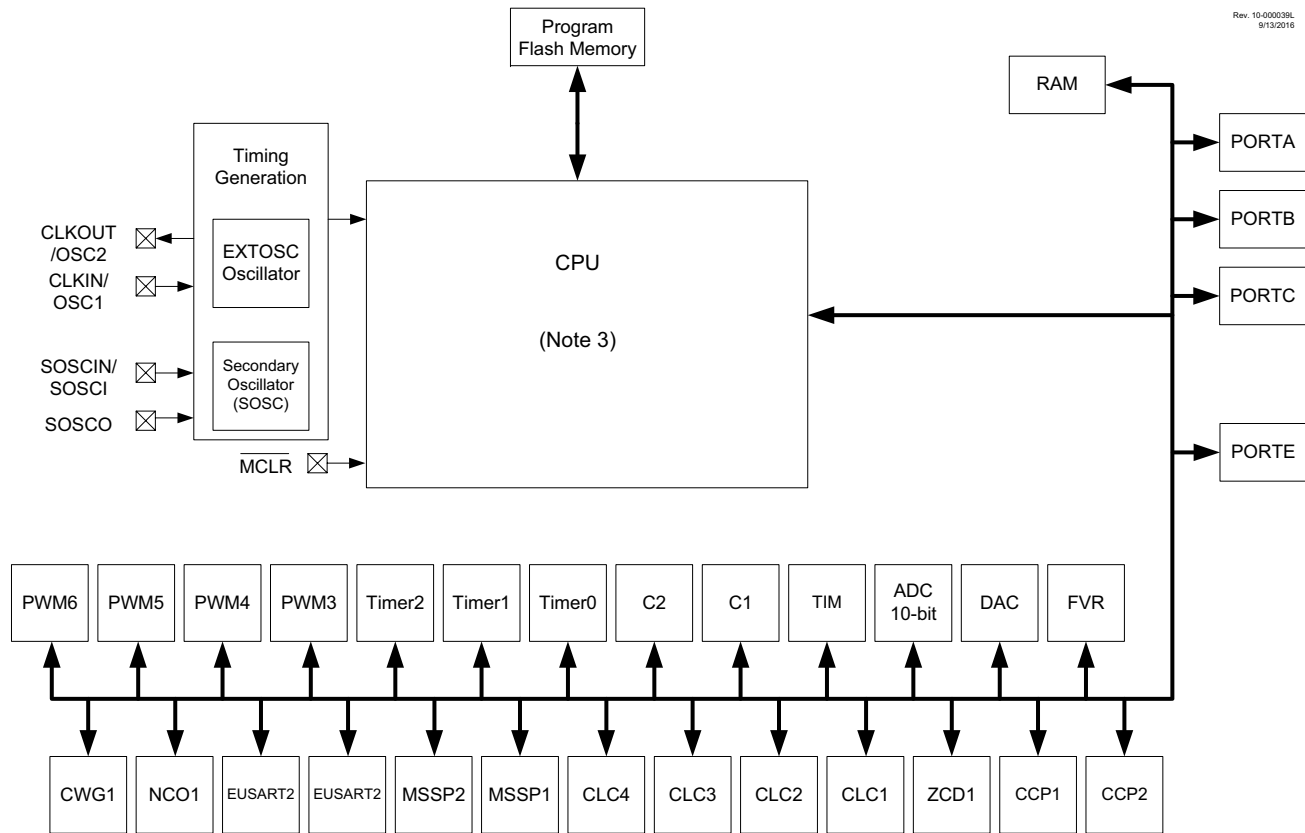
### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	44
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 43x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f15385t-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16f15385t-i-pt</a>

**FIGURE 1-1: PIC16(L)F15356 BLOCK DIAGRAM**

**Note 1:** See applicable chapters for more information on peripherals.

**2:** See Table 1-1 for peripherals available on specific devices.

**3:** See Figure 3-1.

# PIC16(L)F15356/75/76/85/86

**TABLE 1-2: PIC16(L)F15356 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RA6/ANA6/OSC2/CLKOUT/IOCA6	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	—	ADC Channel A6 input.
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
	CLKOUT	—	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	IOCA6	TTL/ST	—	Interrupt-on-change input.
RA7/ANA7/OSC1/CLKIN/IOCA7	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel A7 input.
	OSC1	XTAL	—	External Crystal/Resonator (LP, XT, HS modes) driver input.
	CLKIN	TTL/ST	—	External digital clock input.
	IOCA7	TTL/ST	—	Interrupt-on-change input.
RB0/ANB0/C2IN1+/ZCD1/ $\overline{SS}2^{(1)}$ /CWG1IN <sup>(1)</sup> /INT <sup>(1)</sup> /IOCB0	RB0	TTL/ST	CMOS/OD	General purpose I/O.
	ANB0	AN	—	ADC Channel B0 input.
	C2IN1+	AN	—	Comparator 2 positive input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	$\overline{SS}2^{(1)}$	TTL/ST	—	MSSP2 SPI slave select input.
	CWG1IN <sup>(1)</sup>	TTL/ST	—	Complementary Waveform Generator 1 input.
	INT <sup>(1)</sup>	TTL/ST	—	External interrupt request input.
	IOCB0	TTL/ST	—	Interrupt-on-change input.
RB1/ANB1/C1IN3-/C2IN3-/SCL2 <sup>(3,4)</sup> /SCK2 <sup>(1)</sup> /IOCB1	RB1	TTL/ST	CMOS/OD	General purpose I/O.
	ANB1	AN	—	ADC Channel B1 input.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	SCL2 <sup>(3,4)</sup>	I <sup>2</sup> C	OD	MSSP2 I <sup>2</sup> C clock input/output.
	SCK2 <sup>(1)</sup>	TTL/ST	CMOS/OD	MSSP2 SPI serial clock (default input location, SCK2 is a PPS remappable input and output).
	IOCB1	TTL/ST	—	Interrupt-on-change input.
RB2/ANB2/SDA2 <sup>(3,4)</sup> /SDI2 <sup>(1)</sup> /IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA2 <sup>(3,4)</sup>	I <sup>2</sup> C	OD	MSSP2 I <sup>2</sup> C serial data input/output.
	SDI2 <sup>(1)</sup>	TTL/ST	—	MSSP2 SPI serial data input.
	IOCB2	TTL/ST	—	Interrupt-on-change input.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open-Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage    XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLV register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

## 5.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory are controlled independently. Internal access to the program memory is unaffected by any code protection setting.

### 5.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the CP bit in Configuration Words. When  $\overline{CP} = 0$ , external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Self-writing the program memory is dependent upon the write protection setting. See **Section 5.4 “Write Protection”** for more information.

## 5.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The  $\overline{WRTAPP}$ ,  $\overline{WRTSAF}$ ,  $\overline{WRTB}$ ,  $\overline{WRTC}$  bits in Configuration Words (Register 5-4) define whether the corresponding region of the program memory block is protected or not.

## 5.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 13.3.6 “NVMREG Access to Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Words”** for more information on accessing these memory locations. For more information on checksum calculation, see the “PIC16(L)F153xx Memory Programming Specification” (DS40001838).

## 8.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

## 8.2 Brown-out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 8-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Words.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 8-2 for more information.

**TABLE 8-1: BOR OPERATING MODES**

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	x	X	Active	Wait for release of BOR <sup>(1)</sup> (BORRDY = 1)
10	x	Awake	Active	Waits for release of BOR (BORRDY = 1) Waits for BOR Reset release
		Sleep	Disabled	
01	1	X	Active	Waits for BOR Reset release (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	x	X	Disabled	

**Note 1:** In this specific case, “Release of POR” and “Wake-up from Sleep”, there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

### 8.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to ‘11’, the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

### 8.2.2 BOR IS OFF IN SLEEP

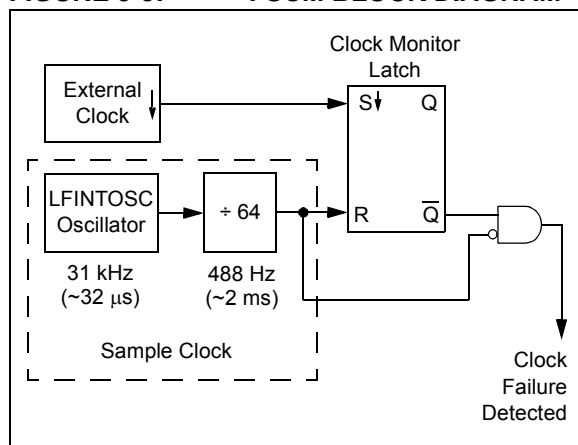
When the BOREN bits of Configuration Words are programmed to ‘10’, the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

## 9.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, ECL, ECM, ECH and Secondary Oscillator).

**FIGURE 9-9: FSCM BLOCK DIAGRAM**



### 9.4.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 9-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

### 9.4.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to the HFINTOSC at 1 MHz clock frequency and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation, by writing to the NOSC and NDIV bits of the OSCCON1 register.

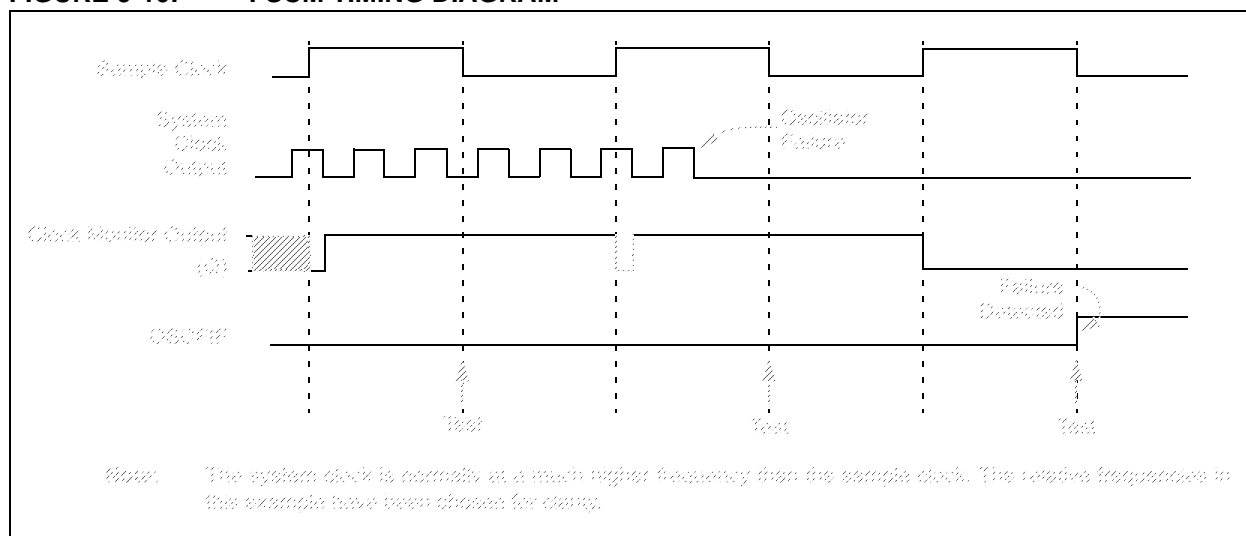
### 9.4.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the NOSC and NDIV bits of the OSCCON1 register. When switching to the external oscillator, or external oscillator and PLL, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON1. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

### 9.4.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. Therefore, the device will always be executing code while the OST is operating.

**FIGURE 9-10: FSCM TIMING DIAGRAM**



# PIC16(L)F15356/75/76/85/86

## REGISTER 10-9: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
—	—	NVMIE	NCO1IE	—	—	—	CWG1IE
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HS = Hardware set

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **NVMIE:** NVM Interrupt Enable bit

1 = NVM task complete interrupt enabled

0 = NVM interrupt not enabled

bit 4 **NCO1IE:** NCO Interrupt Enable bit

1 = NCO rollover interrupt enabled

0 = NCO rollover interrupt disabled

bit 3-1 **Unimplemented:** Read as '0'.

bit 0 **CWG1IE:** Complementary Waveform Generator (CWG) 2 Interrupt Enable bit

1 = CWG1 interrupt is enabled

0 = CWG1 interrupt disabled

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE7.

## 11.2.2 WAKE-UP USING INTERRUPTS

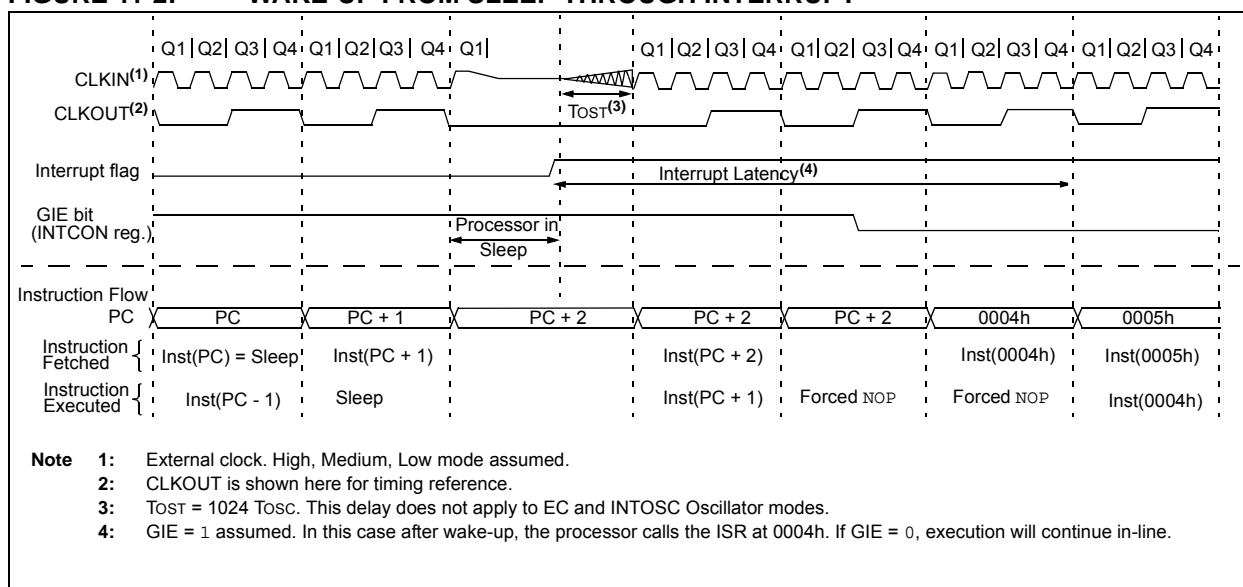
When global interrupts are disabled (GIE cleared) and any interrupt source, with the exception of the clock switch interrupt, has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a **SLEEP** instruction
  - **SLEEP** instruction will execute as a NOP
  - WDT and WDT prescaler will not be cleared
  - $\overline{TO}$  bit of the STATUS register will not be set
  - $\overline{PD}$  bit of the STATUS register will not be cleared

- If the interrupt occurs **during or after** the execution of a **SLEEP** instruction
  - **SLEEP** instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - $\overline{TO}$  bit of the STATUS register will be set
  - $\overline{PD}$  bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a **SLEEP** instruction, it may be possible for flag bits to become set before the **SLEEP** instruction completes. To determine whether a **SLEEP** instruction executed, test the  $\overline{PD}$  bit. If the  $\overline{PD}$  bit is set, the **SLEEP** instruction was executed as a NOP.

**FIGURE 11-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT**



## 11.2.3 LOW-POWER SLEEP MODE

The PIC16F15356/75/76/85/86 device contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode.

The PIC16F15356/75/76/85/86 allows the user to optimize the operating current in Sleep, depending on the application requirements.

Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. Depending on the configuration of these bits, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

### 11.2.3.1 Sleep Current vs. Wake-up Time

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking-up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The Normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.



## 12.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a `CLRWDT` instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that `CLRWDT` instructions are only accepted when they are performed within a specific window during the time-out period.

The WDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

# PIC16(L)F15356/75/76/85/86

**REGISTER 17-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER**

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4

**IOCBP<7:4>:** Interrupt-on-Change PORTB Positive Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

bit 3-0

**Unimplemented:** read as '0'

**REGISTER 17-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER**

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4

**IOCBN<7:4>:** Interrupt-on-Change PORTB Negative Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

bit 3-0

**Unimplemented:** read as '0'

# PIC16(L)F15356/75/76/85/86

## REGISTER 20-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	—	ADPREF<1:0>	
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **ADFM:** ADC Result Format Select bit  
1 = Right justified. Six Most Significant bits of ADRESH are set to '0' when the conversion result is loaded.  
0 = Left justified. Six Least Significant bits of ADRESL are set to '0' when the conversion result is loaded.
- bit 6-4      **ADCS<2:0>:** ADC Conversion Clock Select bits  
111 = ADCRC (dedicated RC oscillator)  
110 = Fosc/64  
101 = Fosc/16  
100 = Fosc/4  
011 = ADCRC (dedicated RC oscillator)  
010 = Fosc/32  
001 = Fosc/8  
000 = Fosc/2
- bit 3-2      **Unimplemented:** Read as '0'
- bit 1-0      **ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits  
11 = VREF+ is connected to internal Fixed Voltage Reference (FVR) module<sup>(1)</sup>  
10 = VREF+ is connected to external VREF+ pin<sup>(1)</sup>  
01 = Reserved  
00 = VREF+ is connected to VDD

**Note 1:** When selecting the VREF+ pin as the source of the positive reference, be aware that a minimum voltage specification exists. See Table 37-14 for details.

## 22.2 FIXED DUTY CYCLE MODE

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO\_overflow), the output is toggled at a frequency rate half of the F\_OVERFLOW. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 22-2.

The FDC mode is selected by clearing the N1PFM bit in the NCO1CON register.

## 22.3 PULSE FREQUENCY MODE

In Pulse Frequency (PF) mode, every time the Accumulator overflows, the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output. The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 22-2.

The value of the active and inactive states depends on the polarity bit, N1POL in the NCO1CON register.

The PF mode is selected by setting the N1PFM bit in the NCO1CON register.

### 22.3.1 OUTPUT PULSE WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the N1PWS<2:0> bits in the NCO1CLK register.

When the selected pulse width is greater than the Accumulator overflow time frame, then NCO1 output does not toggle.

## 22.4 OUTPUT POLARITY CONTROL

The last stage in the NCO module is the output polarity. The N1POL bit in the NCO1CON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

The NCO output signal (NCO1\_out) is available to the following peripherals:

- CLC
- CWG
- Timer1
- Timer2
- CLKR

## 22.5 Interrupts

When the accumulator overflows (NCO\_overflow), the NCO Interrupt Flag bit, NCO1IF, of the PIR7 register is set. To enable the interrupt event (NCO\_interrupt), the following bits must be set:

- N1EN bit of the NCO1CON register
- NCO1IE bit of the PIE7 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt must be cleared by software by clearing the NCO1IF bit in the Interrupt Service Routine.

## 22.6 Effects of a Reset

All of the NCO registers are cleared to zero as the result of a Reset.

## 22.7 Operation in Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

# PIC16(L)F15356/75/76/85/86

## REGISTER 29-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWMxDC<9:2>							
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PWMxDC<9:2>**: PWM Duty Cycle Most Significant bits  
These bits are the MSBs of the PWM duty cycle. The two LSBs are found in PWMxDCL Register.

## REGISTER 29-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxDC<1:0>		—	—	—	—	—	—
bit 7				bit 0			

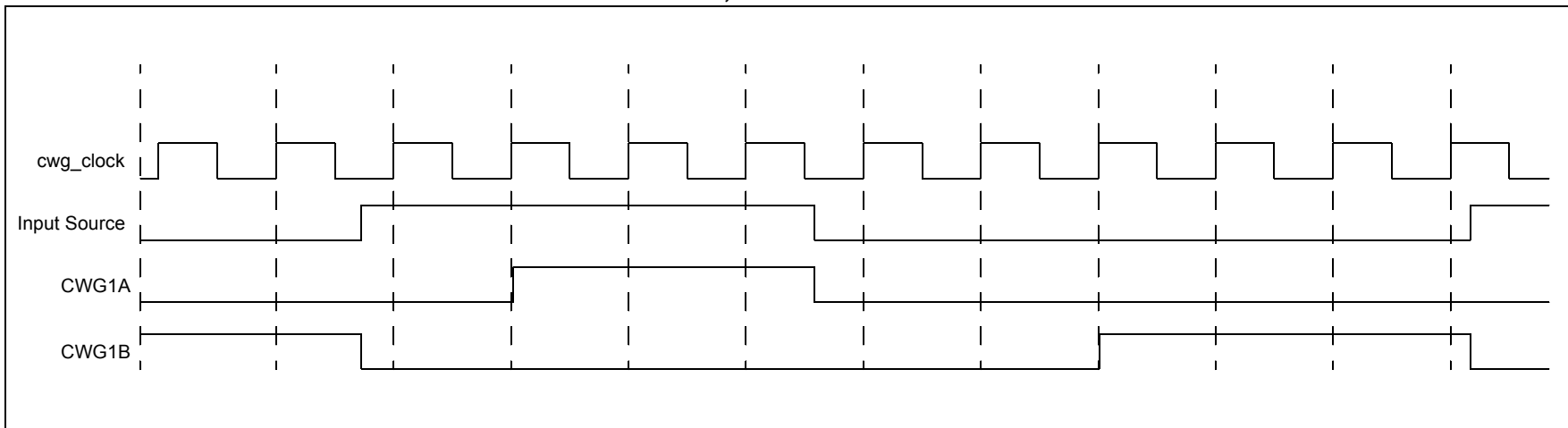
### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

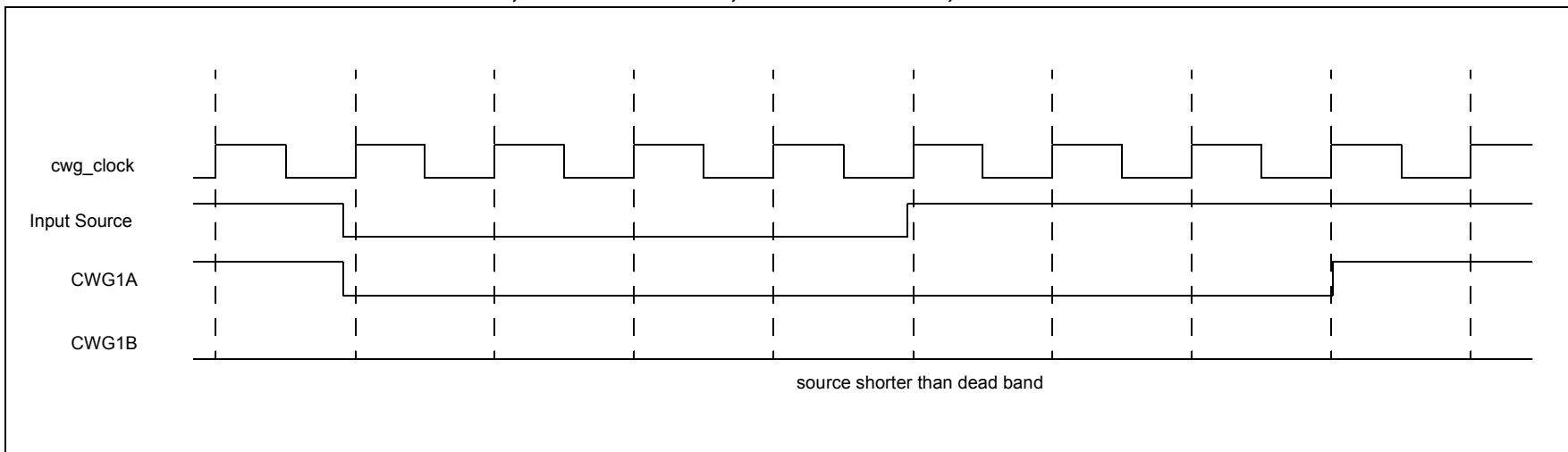
bit 7-6 **PWMxDC<1:0>**: PWM Duty Cycle Least Significant bits  
These bits are the LSBs of the PWM duty cycle. The MSBs are found in PWMxDCH Register.

bit 5-0 **Unimplemented**: Read as '0'

**FIGURE 30-6: DEAD-BAND OPERATION CWG1DBR = 0X01, CWG1DBF = 0X02**



**FIGURE 30-7: DEAD-BAND OPERATION, CWG1DBR = 0X03, CWG1DBF = 0X04, SOURCE SHORTER THAN DEAD BAND**



## 30.12 Configuring the CWG

The following steps illustrate how to properly configure the CWG.

1. Ensure that the TRIS control bits corresponding to the desired CWG pins for your application are set so that the pins are configured as inputs.
2. Clear the EN bit, if not already cleared.
3. Set desired mode of operation with the MODE bits.
4. Set desired dead-band times, if applicable to mode, with the CWG1DBR and CWG1DBF registers.
5. Setup the following controls in the CWG1AS0 and CWG1AS1 registers.
  - a. Select the desired shutdown source.
  - b. Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
  - c. Set which pins will be affected by auto-shutdown with the CWG1AS1 register.
  - d. Set the SHUTDOWN bit and clear the REN bit.
6. Select the desired input source using the CWG1ISM register.
7. Configure the following controls.
  - a. Select desired clock source using the CWG1CLKCON register.
  - b. Select the desired output polarities using the CWG1CON1 register.
  - c. Set the output enables for the desired outputs.
8. Set the EN bit.
9. Clear TRIS control bits corresponding to the desired output pins to configure these pins as outputs.
10. If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit to start the CWG.

### 30.12.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the LSB and LSAC bits of the CWG1AS0 register. LSB<1:0> controls the CWG1B and D override levels and LSAC<1:0> controls the CWG1A and C override levels. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not affect the override level.

### 30.12.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the REN bit of the CWG1CON2 register. Waveforms of software controlled and automatic restarts are shown in Figure 30-13 and Figure 30-14.

#### 30.12.2.1 Software Controlled Restart

When the REN bit of the CWG1AS0 register is cleared, the CWG must be restarted after an auto-shutdown event by software. Clearing the shutdown state requires all selected shutdown inputs to be low, otherwise the SHUTDOWN bit will remain set. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

#### 30.12.2.2 Auto-Restart

When the REN bit of the CWG1CON2 register is set, the CWG will restart from the auto-shutdown state automatically. The SHUTDOWN bit will clear automatically when all shutdown sources go low. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

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## REGISTER 30-2: CWG1CON1: CWG1 CONTROL REGISTER 1

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IN	—	POLD	POLC	POLB	POLA
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7-6	<b>Unimplemented:</b> Read as '0'
bit 5	<b>IN:</b> CWG Input Value bit
bit 4	<b>Unimplemented:</b> Read as '0'
bit 3	<b>POLD:</b> CWG1D Output Polarity bit 1 = Signal output is inverted polarity 0 = Signal output is normal polarity
bit 2	<b>POLC:</b> CWG1C Output Polarity bit 1 = Signal output is inverted polarity 0 = Signal output is normal polarity
bit 1	<b>POLB:</b> CWG1B Output Polarity bit 1 = Signal output is inverted polarity 0 = Signal output is normal polarity
bit 0	<b>POLA:</b> CWG1A Output Polarity bit 1 = Signal output is inverted polarity 0 = Signal output is normal polarity



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**REGISTER 30-5: CWG1AS0: CWG1 AUTO-SHUTDOWN CONTROL REGISTER 0**

R/W/HS-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	U-0	U-0
SHUTDOWN <sup>(1,2)</sup>	REN	LSBD<1:0>		LSAC<1:0>		—	—
bit 7							bit 0

**Legend:**

HC = Bit is cleared by hardware

HS = Bit is set by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7 **SHUTDOWN:** Auto-Shutdown Event Status bit<sup>(1,2)</sup>

1 = An Auto-Shutdown state is in effect

0 = No Auto-shutdown event has occurred

bit 6 **REN:** Auto-Restart Enable bit

1 = Auto-restart enabled

0 = Auto-restart disabled

bit 5-4 **LSBD<1:0>:** CWG1B and CWG1D Auto-Shutdown State Control bits

11 =A logic '1' is placed on CWG1B/D when an auto-shutdown event is present

10 =A logic '0' is placed on CWG1B/D when an auto-shutdown event is present

01 =Pin is tri-stated on CWG1B/D when an auto-shutdown event is present

00 =The inactive state of the pin, including polarity, is placed on CWG1B/D after the required dead-band interval

bit 3-2 **LSAC<1:0>:** CWG1A and CWG1C Auto-Shutdown State Control bits

11 =A logic '1' is placed on CWG1A/C when an auto-shutdown event is present

10 =A logic '0' is placed on CWG1A/C when an auto-shutdown event is present

01 =Pin is tri-stated on CWG1A/C when an auto-shutdown event is present

00 =The inactive state of the pin, including polarity, is placed on CWG1A/C after the required dead-band interval

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This bit may be written while EN = 0 (CWG1CON0 register) to place the outputs into the shutdown configuration.

**2:** The outputs will remain in auto-shutdown state until the next rising edge of the input signal after this bit is cleared.

## 32.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allows time for the slave software to decide whether it wants to ACK the receive address or data byte.

This list describes the steps that need to be taken by slave software to use these options for I<sup>2</sup>C communication. Figure 32-16 displays a module using both address and data holding. Figure 32-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the ACK.
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets ACK value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an ACK, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the ACK.
10. Slave clears SSPxIF.

<p><b>Note:</b> SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set</p>
--

11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSPxSTAT register.

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## REGISTER 32-4: SSPxCON3: SSPx CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM <sup>(3)</sup>	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **ACKTIM:** Acknowledge Time Status bit (I<sup>2</sup>C mode only)<sup>(3)</sup>  
1 = Indicates the I<sup>2</sup>C bus is in an Acknowledge sequence, set on 8<sup>th</sup> falling edge of SCL clock  
0 = Not an Acknowledge sequence, cleared on 9<sup>th</sup> rising edge of SCL clock
- bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I<sup>2</sup>C mode only)  
1 = Enable interrupt on detection of Stop condition  
0 = Stop detection interrupts are disabled<sup>(2)</sup>
- bit 5 **SCIE:** Start Condition Interrupt Enable bit (I<sup>2</sup>C mode only)  
1 = Enable interrupt on detection of Start or Restart conditions  
0 = Start detection interrupts are disabled<sup>(2)</sup>
- bit 4 **BOEN:** Buffer Overwrite Enable bit  
In SPI Slave mode:<sup>(1)</sup>  
1 = SSPxBUF updates every time that a new data byte is shifted in ignoring the BF bit  
0 = If new byte is received with BF bit of the SSPxSTAT register already set, SSPOV bit of the SSPxCON1 register is set, and the buffer is not updated  
In I<sup>2</sup>C Master mode and SPI Master mode:  
This bit is ignored.  
In I<sup>2</sup>C Slave mode:  
1 = SSPxBUF is updated and ACK is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0.  
0 = SSPxBUF is only updated when SSPOV is clear
- bit 3 **SDAHT:** SDA Hold Time Selection bit (I<sup>2</sup>C mode only)  
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL  
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL
- bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I<sup>2</sup>C Slave mode only)  
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR3 register is set, and bus goes idle  
1 = Enable slave bus collision interrupts  
0 = Slave bus collision interrupts are disabled
- bit 1 **AHEN:** Address Hold Enable bit (I<sup>2</sup>C Slave mode only)  
1 = Following the eighth falling edge of SCL for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCL will be held low.  
0 = Address holding is disabled
- bit 0 **DHEN:** Data Hold Enable bit (I<sup>2</sup>C Slave mode only)  
1 = Following the eighth falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSPxCON1 register and SCL is held low.  
0 = Data holding is disabled

- Note 1:** For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.
- 2:** This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.
- 3:** The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

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**TABLE 37-6: THERMAL CHARACTERISTICS**

Standard Operating Conditions (unless otherwise stated)					
Param. No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	$\theta_{JA}$	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package
			80	°C/W	28-pin SOIC package
			90	°C/W	28-pin SSOP package
			48	°C/W	28-pin UQFN 4x4mm package
			47.2	°C/W	40-pin PDIP package
			41.0	°C/W	40-pin UQFN 5x5 package
			46.0	°C/W	44-pin TQFP package
			24.4	°C/W	44-pin QFN 8x8mm package
			27.6	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
			—	°C/W	48-pin QFN 8x8mm package
TH02	$\theta_{JC}$	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package
			24	°C/W	28-pin SOIC package
			24	°C/W	28-pin SSOP package
			12	°C/W	28-pin UQFN 4x4mm package
			24.70	°C/W	40-pin PDIP package
			5.5	°C/W	40-pin UQFN 5x5 package
			14.5	°C/W	44-pin TQFP package
			20.0	°C/W	44-pin QFN 8x8mm package
			6.7	°C/W	48-pin UQFN 6x6 package
			—	°C/W	48-pin TQFP 7x7 package
TH03	T <sub>JMAX</sub>	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	PD = P <sub>INTERNAL</sub> + P <sub>I/O</sub>
TH05	P <sub>INTERNAL</sub>	Internal Power Dissipation	—	W	P <sub>INTERNAL</sub> = I <sub>DD</sub> × V <sub>DD</sub> <sup>(1)</sup>
TH06	P <sub>I/O</sub>	I/O Power Dissipation	—	W	P <sub>I/O</sub> = $\Sigma (I_{OL} \times V_{OL}) + \Sigma (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	P <sub>DER</sub>	Derated Power	—	W	P <sub>DER</sub> = P <sub>DMAX</sub> (T <sub>J</sub> - T <sub>A</sub> )/ $\theta_{JA}$ <sup>(2)</sup>

**Note 1:** I<sub>DD</sub> is current to run the chip alone without driving any load on the output pins.

**2:** T<sub>A</sub> = Ambient Temperature, T<sub>J</sub> = Junction Temperature

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