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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15356-i-ss

TABLE 1-3: PIC16(L)F15375/76 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0-/C2IN0-/CLCIN0(1)/IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0-	AN	—	Comparator negative input.
	C2IN0-	AN	—	Comparator negative input.
	CLCIN0(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/C1IN1-/C2IN1-/CLCIN1(1)/IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	C1IN1-	AN	—	Comparator negative input.
	C2IN1-	AN	—	Comparator negative input.
	CLCIN1(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/C1IN0+/C2IN0+/DAC1OUT1/IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	C1IN0+	AN	—	Comparator positive input.
	C2IN0+	AN	—	Comparator positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
RA3/ANA3/C1IN1+/VREF+/DACREF+/IOCA3	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN	—	ADC Channel A3 input.
	C1IN1+	AN	—	Comparator positive input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
RA4/ANA4/T0CKI(1)/IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T0CKI(1)	TTL/ST	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
RA5/ANA5/$\overline{SS1}$(1)/T1G(1)/IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	$\overline{SS1}$(1)	TTL/ST	—	MSSP1 SPI slave select input.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C
HV = High Voltage; XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-5, Table 15-6 and Table 15-6.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

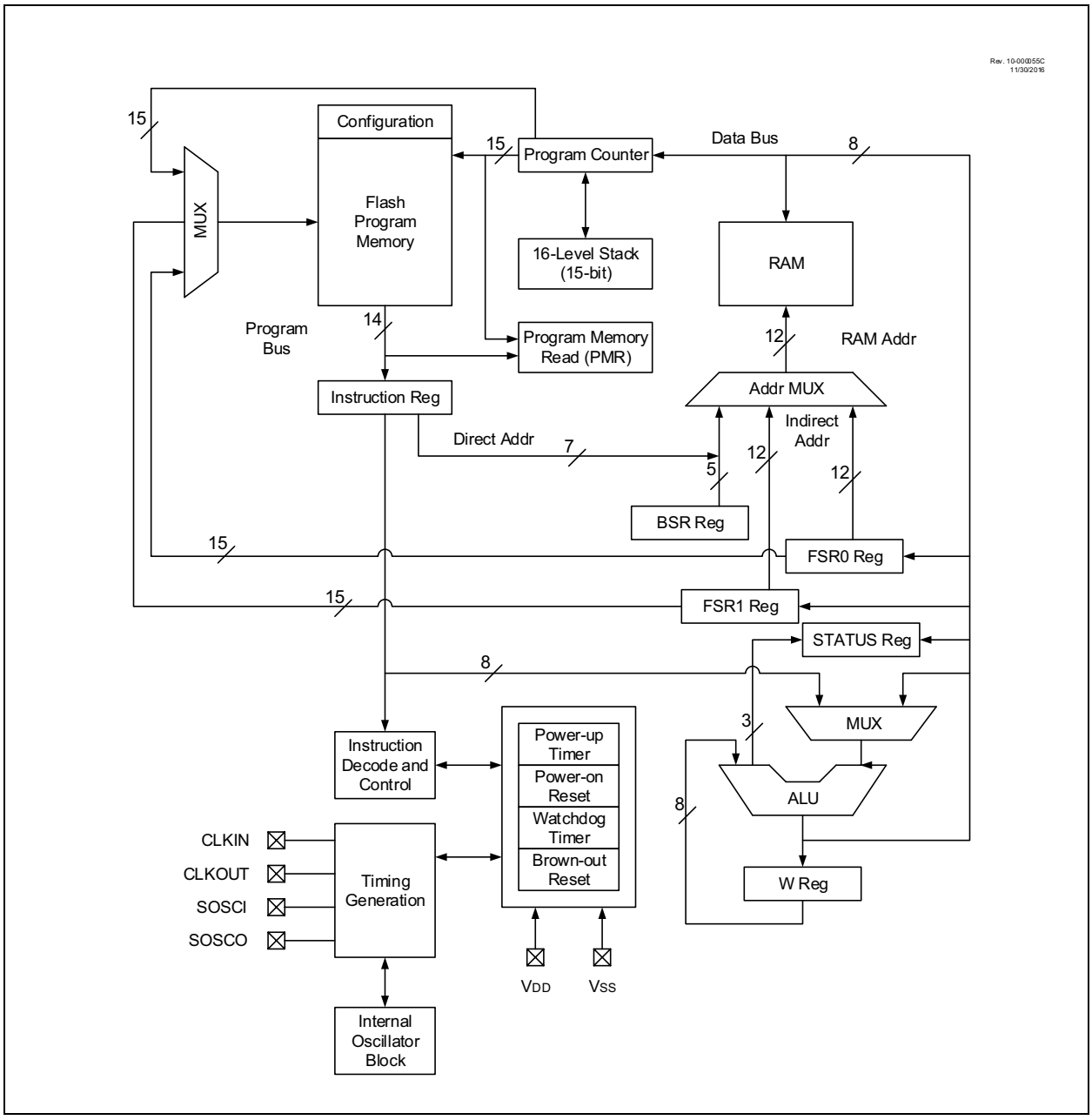
4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving.

The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH DIAGRAM



3.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 10.5 "Automatic Context Saving"** for more information.

3.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 4.5 "Stack"** for more details.

3.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. See **Section 4.6 "Indirect Addressing"** for more details.

3.4 Instruction Set

There are 48 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 36.0 "Instruction Set Summary"** for more details.

TABLE 4-9: PIC16(L)F15356/75/76/85/86 MEMORY MAP, BANKS 60, 61, 62, AND 63

	Bank 60		Bank 61		Bank 62		Bank 63
1E0Ch	—	1E8Ch	RF7PPS(2)	1F0Ch	—	1F8Ch	—
1E0Dh	—	1E8Dh	—	1F0Dh	—	1F8Dh	—
1E0Eh	—	1E8Eh	—	1F0Eh	—	1F8Eh	—
1E0Fh	CLCDATA	1E8Fh	PPSLOCK	1F0Fh	—	1F8Fh	—
1E10h	CLC1CON	1E90h	INTPPS	1F10h	RA0PPS	1F90h	—
1E11h	CLC1POL	1E91h	T0CKIPPS	1F11h	RA1PPS	1F91h	—
1E12h	CLC1SEL0	1E92h	T1CKIPPS	1F12h	RA2PPS	1F92h	—
1E13h	CLC1SEL1	1E93h	T1GPPS	1F13h	RA3PPS	1F93h	—
1E14h	CLC1SEL2	1E94h	—	1F14h	RA4PPS	1F94h	—
1E15h	CLC1SEL3	1E95h	—	1F15h	RA5PPS	1F95h	—
1E16h	CLC1GLS0	1E96h	—	1F16h	RA6PPS	1F96h	—
1E17h	CLC1GLS1	1E97h	—	1F17h	RA7PPS	1F97h	—
1E18h	CLC1GLS2	1E98h	—	1F18h	RB0PPS	1F98h	—
1E19h	CLC1GLS3	1E99h	—	1F19h	RB1PPS	1F99h	—
1E1Ah	CLC2CON	1E9Ah	—	1F1Ah	RB2PPS	1F9Ah	—
1E1Bh	CLC2POL	1E9Bh	—	1F1Bh	RB3PPS	1F9Bh	—
1E1Ch	CLC2SEL0	1E9Ch	T2INPPS	1F1Ch	RB4PPS	1F9Ch	—
1E1Dh	CLC2SEL1	1E9Dh	—	1F1Dh	RB5PPS	1F9Dh	—
1E1Eh	CLC2SEL2	1E9Eh	—	1F1Eh	RB6PPS	1F9Eh	—
1E1Fh	CLC2SEL3	1E9Fh	—	1F1Fh	RB7PPS	1F9Fh	—
1E20h	CLC2GLS0	1EA0h	—	1F20h	RC0PPS	1FA0h	—
1E21h	CLC2GLS1	1EA1h	CCP1PPS	1F21h	RC1PPS	1FA1h	—
1E22h	CLC2GLS2	1EA2h	CCP2PPS	1F22h	RC2PPS	1FA2h	—
1E23h	CLC2GLS3	1EA3h	—	1F23h	RC3PPS	1FA3h	—
1E24h	CLC3CON	1EA4h	—	1F24h	RC4PPS	1FA4h	—
1E25h	CLC3POL	1EA5h	—	1F25h	RC5PPS	1FA5h	—
1E26h	CLC3SEL0	1EA6h	—	1F26h	RC6PPS	1FA6h	—
1E27h	CLC3SEL1	1EA7h	—	1F27h	RC7PPS	1FA7h	—
1E28h	CLC3SEL2	1EA8h	—	1F28h	RD0PPS(1)	1FA8h	—
1E29h	CLC3SEL3	1EA9h	—	1F29h	RD1PPS(1)	1FA9h	—
1E2Ah	CLC3GLS0	1EAAh	—	1F2Ah	RD2PPS(1)	1FAAh	—
1E2Bh	CLC3GLS1	1EABh	—	1F2Bh	RD3PPS(1)	1FABh	—
1E2Ch	CLC3GLS2	1EACh	—	1F2Ch	RD4PPS(1)	1FACh	—
1E2Dh	CLC3GLS3	1EADh	—	1F2Dh	RD5PPS(1)	1FADh	—
1E2Eh	CLC4CON	1EAEh	—	1F2Eh	RD6PPS(1)	1FAEh	—
1E2Fh	CLC4POL	1EAFh	—	1F2Fh	RD7PPS(1)	1FAFh	—
1E30h	CLC4SEL0	1EB0h	—	1F30h	RE0PPS(1)	1FB0h	—
1E31h	CLC4SEL1	1EB1h	CWG1PPS	1F31h	RE1PPS(1)	1FB1h	—
1E32h	CLC4SEL2	1EB2h	—	1F32h	RE2PPS(1)	1FB2h	—
1E33h	CLC4SEL3	1EB3h	—	1F33h	—	1FB3h	—
1E34h	CLC4GLS0	1EB4h	—	1F34h	—	1FB4h	—
1E35h	CLC4GLS1	1EB5h	—	1F35h	—	1FB5h	—
1E36h	CLC4GLS2	1EB6h	—	1F36h	—	1FB6h	—
1E37h	CLC4GLS3	1EB7h	—	1F37h	—	1FB7h	—
1E38h	RF0PPS(2)	1EB8h	—	1F38h	ANSELA	1FB8h	—
1E39h	RF1PPS(2)	1EB9h	—	1F39h	WPUA	1FB9h	—
1E3Ah	RF2PPS(2)	1EBAh	—	1F3Ah	ODCONA	1FBAh	—
1E3Bh	RF3PPS(2)	1EBBh	CLCIN0PPS	1F3Bh	SLRCONA	1FBBh	—
1E3Ch	RF4PPS(2)	1EBCh	CLCIN1PPS	1F3Ch	INLVLA	1FBCh	—
1E3Dh	RF5PPS(2)	1EBDh	CLCIN2PPS	1F3Dh	IOCAP	1FBDh	—
1E3Eh	RF6PPS(2)	1EBEh	CLCIN3PPS	1F3Eh	IOCAN	1FBEh	—

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Present only on PIC16(L)F15375/76/85/86.

2: Present only on PIC16(L)F15385/86

REGISTER 9-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	U-0	R-q/q
EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **EXTOR:** EXTOSC (external) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 6 **HFOR:** HFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 5 **MFOR:** MFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 4 **LFOR:** LFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 3 **SOR:** Secondary (Timer1) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 2 **ADOR:** CRC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used.

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **PLLR:** PLL is Ready bit
1 = The PLL is ready to be used
0 = The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

12.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that CLRWDT instructions are only accepted when they are performed within a specific window during the time-out period.

The WDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

14.0 I/O PORTS

TABLE 14-1: PORT AVAILABILITY PER DEVICE

Device	PORTA	PORTB	PORTC	PORTD	PORTE	PORTF
PIC16(L)F15356	●	●	●		●	
PIC16(L)F15375/76	●	●	●	●	●	
PIC16(L)F15385/86	●	●	●	●	●	●

Each port has ten standard registers for its operation. These registers are:

- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUx registers (weak pull-up)
- INLVLx (input level control)
- SLRCONx registers (slew rate)
- ODCONx registers (open-drain)

Most port pins share functions with device peripherals, both analog and digital. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output; however, the pin can still be read.

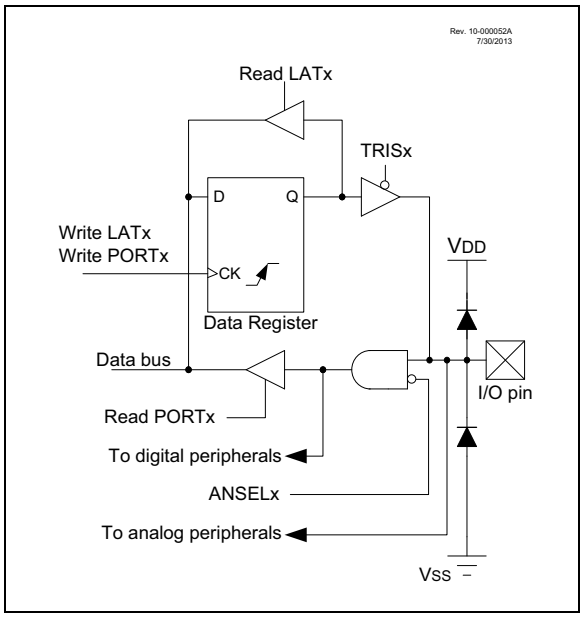
The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 14-1.

FIGURE 14-1: GENERIC I/O PORT OPERATION



14.1 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over the digital outputs and force the digital output driver to the high-impedance state.

TABLE 15-6: PPS OUTPUT SIGNAL ROUTING OPTIONS (PIC16(L)F15375/76)

Output Signal Name	RxyPPS Register Value	Remappable to Pins of PORTx				
		PIC16(L)F15375/76				
		PORTA	PORTB	PORTC	PORTD	PORTE
CLKR	0x1B		•	•		
NCO1OUT	0x1A	•			•	
TMR0	0x19		•	•		
SDO2/SDA2	0x18		•		•	
SCK2/SCL2	0x17		•		•	
SDO1/SDA1	0x16		•	•		
SCK1/SCL1	0x15		•	•		
C2OUT	0x14	•				•
C1OUT	0x13	•			•	
DT2	0x12		•		•	
TX2/CK2	0x11		•		•	
DT1	0x10		•	•		
TX1/CK1	0x0F		•	•		
PWM6OUT	0x0E	•			•	
PWM5OUT	0x0D	•		•		
PWM4OUT	0x0C		•		•	
PWM3OUT	0x0B		•		•	
CCP2	0x0A		•	•		
CCP1	0x09		•	•		
CWG1D	0x08		•		•	
CWG1C	0x07		•		•	
CWG1B	0x06		•		•	
CWG1A	0x05		•	•		
CLC4OUT	0x04		•		•	
CLC3OUT	0x03		•		•	
CLC2OUT	0x02	•		•		
CLC1OUT	0x01	•		•		

15.8 Register Definitions: PPS Input Selection

REGISTER 15-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION(1)

U-0	U-0	R/W-q/u	R/W-q/u	R/W/q/u	R/W-q/u	R/W-q/u	R/W-q/u
—	—	xxxPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = value depends on peripheral

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **xxxPPS<5:0>:** Peripheral xxx Input Selection bits
See Tables 15-1 through 15-3.

Note 1: The “xxx” in the register name “xxxPPS” represents the input signal function name, such as “INT”, “T0CKI”, “RX”, etc. This register summary shown here is only a prototype of the array of actual registers, as each input function has its own dedicated SFR (ex: INTPPS, T0CKIPPS, RXPPS, etc.).

2: Each specific input signal may only be mapped to a subset of these I/O pins, as shown in Table 15-4. Attempting to map an input signal to a non-supported I/O pin will result in undefined behavior. For example, the “INT” signal map be mapped to any PORTA or PORTB pin. Therefore, the INTPPS register may be written with values from 0x00-0x0F (corresponding to RA0-RB7). Attempting to write 0x10 or higher to the INTPPS register is not supported and will result in undefined behavior.

20.2 ADC Operation

20.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/$\overline{\text{DONE}}$ bit will not be set in the same instruction that turns on the ADC. Refer to **Section 20.2.6 "ADC Conversion Procedure"**.

20.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF Interrupt Flag bit
- Update the ADRESH and ADRESL registers with new conversion result

20.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH and ADRESL registers will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

20.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the ADCRC option. When the ADCRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than ADCRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

20.2.5 AUTO-CONVERSION TRIGGER

The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware.

The Auto-conversion Trigger source is selected with the ADACT<3:0> bits of the ADACT register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See Table 20-2 for auto-conversion sources.

TABLE 20-2: ADC AUTO-CONVERSION TABLE

ADACT VALUE	SOURCE/ PERIPHERAL	DESCRIPTION
0x00	Disabled	External Trigger Disabled
0x01	ADACTPPS	Pin Selected by ADACTPPS
0x02	TMR0	Timer0 overflow condition
0x03	TMR1	Timer1 overflow condition
0x04	TMR2	Match between Timer2 postscaled value and PR2
0x05	CCP1	CCP1 output
0x06	CCP2	CCP2 output
0x07	PWM3	PWM3 output
0x08	PWM4	PWM4 output
0x09	PWM5	PWM5 output
0x0A	PWM6	PWM6 output
0x0B	NCO1	NCO1 output
0x0C	C1OUT	Comparator C1 output
0x0D	C2OUT	Comparator C2 output
0x0E	IOCIF	Interrupt-on change flag trigger
0x0F	CLC1	CLC1 output
0x10	CLC2	CLC2 output
0x11	CLC3	CLC3 output
0x12	CLC4	CLC4 output
0x13-0xFF	Reserved	Reserved, do not use

REGISTER 22-6: NCO1INCL: NCO1 INCREMENT REGISTER – LOW BYTE(1,2)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1
NCO1INC<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **NCO1INC<7:0>:** NCO1 Increment, Low Byte

Note 1: The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.
2: DDSINC is double-buffered as INCBUF; INCBUF is updated on the next falling edge of NCOCLK after writing to NCO1INCL; NCO1INCU and NCO1INCH should be written prior to writing NCO1INCL.

REGISTER 22-7: NCO1INCH: NCO1 INCREMENT REGISTER – HIGH BYTE(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
NCO1INC<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **NCO1INC<15:8>:** NCO1 Increment, High Byte

Note 1: The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.

REGISTER 22-8: NCO1INCU: NCO1 INCREMENT REGISTER – UPPER BYTE(1)

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	NCO1INC<19:16>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’
bit 3-0 **NCO1INC<19:16>:** NCO1 Increment, Upper Byte

Note 1: The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.

27.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except Fosc/4 and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using Fosc/4, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 28.0 "Capture/Compare/PWM Modules"**. The signals are not a part of the Timer2 module.

27.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 27-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

29.0 PULSE-WIDTH MODULATION (PWM)

The PWMx modules generate Pulse-Width Modulated (PWM) signals of varying frequency and duty cycle.

In addition to the CCP modules, the PIC16(L)F15356/75/76/85/86 devices contain four 10-bit PWM modules (PWM3, PWM4, PWM5 and PWM6). The PWM modules reproduce the PWM capability of the CCP modules.

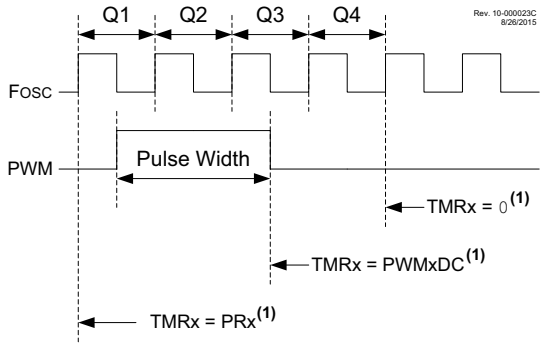
Note:	The PWM3/4/5/6 modules are four instances of the same PWM module design. Throughout this section, the lower case 'x' in register and bit names is a generic reference to the PWM module number (which should be substituted with 3, or 4, or, 5 or 6 during code development). For example, the control register is generically described in this chapter as PWMxCON, but the actual device registers are PWM3CON, PWM4CON, PWM5CON and PWM6CON. Similarly, the PWMxEN bit represents the PWM3EN, PWM4EN, PWM5EN and PWM6EN bits.

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the 'on' state (pulse width), and the low portion of the signal is considered the 'off' state. The term duty cycle describes the proportion of the 'on' time to the 'off' time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and, in turn, the power that is applied to the load.

Figure 29-1 shows a typical waveform of the PWM signal.

FIGURE 29-1: PWM OUTPUT



Note 1: Timer dependent on PWMTMRS register settings.

TABLE 29-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				355
T2TMR	Holding Register for the 8-bit TMR2 Register								335*
T2PR	TMR2 Period Register								335*
RxyPPS	—	—	—	RxyPPS<4:0>					242
CWG1ISM	—	—	—	—	IS<3:0>				401
CLCxSELy	—	—	LCxDyS<5:0>						412
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	200
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	211

Legend: - = Unimplemented locations, read as '0'. Shaded cells are not used by the PWMx module.

* Page with Register information.

TABLE 31-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx (continued)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CLC4GLS1	—	—	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	414
CLC4GLS2	—	—	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	415
CLC4GLS3	—	—	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	416
CLCIN0PPS	—	—	CLCIN0PPS<5:0>						241
CLCIN1PPS	—	—	CLCIN1PPS<5:0>						241
CLCIN2PPS	—	—	CLCIN2PPS<5:0>						241
CLCIN3PPS	—	—	CLCIN3PPS<5:0>						241

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

32.6 I²C Master Mode

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPxCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit, SSPxIF, to be set (SSP interrupt, if enabled):

- Start condition generated
- Stop condition generated
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

Note 1: The MSSP module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur

2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

32.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See **Section 32.7 "Baud Rate Generator"** for more detail.

TABLE 36-3: INSTRUCTION SET (CONTINUED)

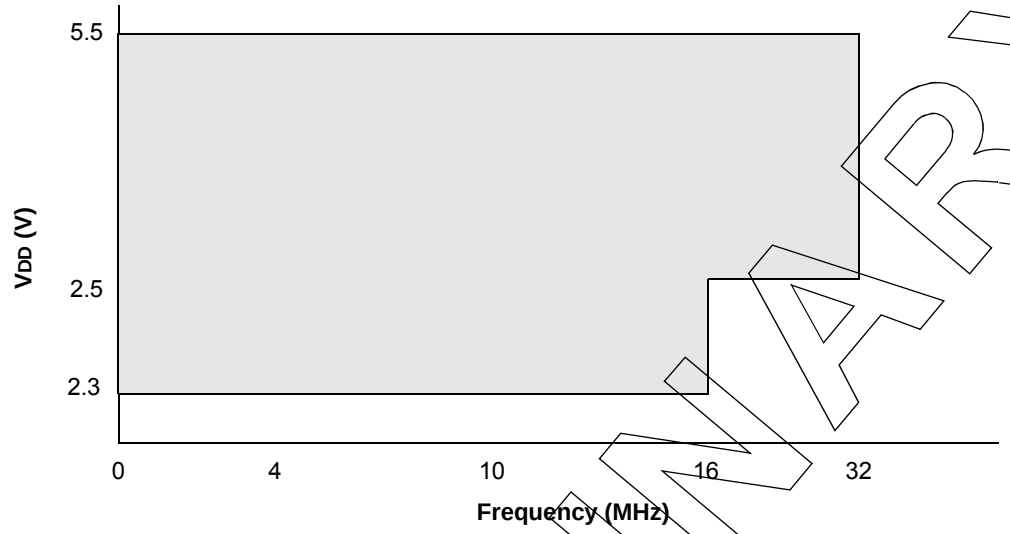
Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
CONTROL OPERATIONS						
BRA	k	Relative Branch	2	11 001k kkkk kkkk		
BRW	–	Relative Branch with W	2	00 0000 0000 1011		
CALL	k	Call Subroutine	2	10 0kkk kkkk kkkk		
CALLW	–	Call Subroutine with W	2	00 0000 0000 1010		
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
RETFIE	k	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 0100 kkkk kkkk		
RETURN	–	Return from Subroutine	2	00 0000 0000 1000		
INHERENT OPERATIONS						
CLRWDT	–	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$, $\overline{PD}$	
NOP	–	No Operation	1	00 0000 0000 0000		
RESET	–	Software device Reset	1	00 0000 0000 0001		
SLEEP	–	Go into Standby or IDLE mode	1	00 0000 0110 0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register with W	1	00 0000 0110 0fff		
C-COMPILER OPTIMIZED						
ADDFSR	n, k	Add Literal k to FSRn	1	11 0001 0nkk kkkk		
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec modifier, mm	1	00 0000 0001 0nmm	Z	**2, 3**
	k[n]	Move INDFn to W, Indexed Indirect.	1	11 1111 0nkk kkkk	Z	**2**
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec modifier, mm	1	00 0000 0001 1nmm		**2, 3**
	k[n]	Move W to INDFn, Indexed Indirect.	1	11 1111 1nkk kkkk		**2**

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

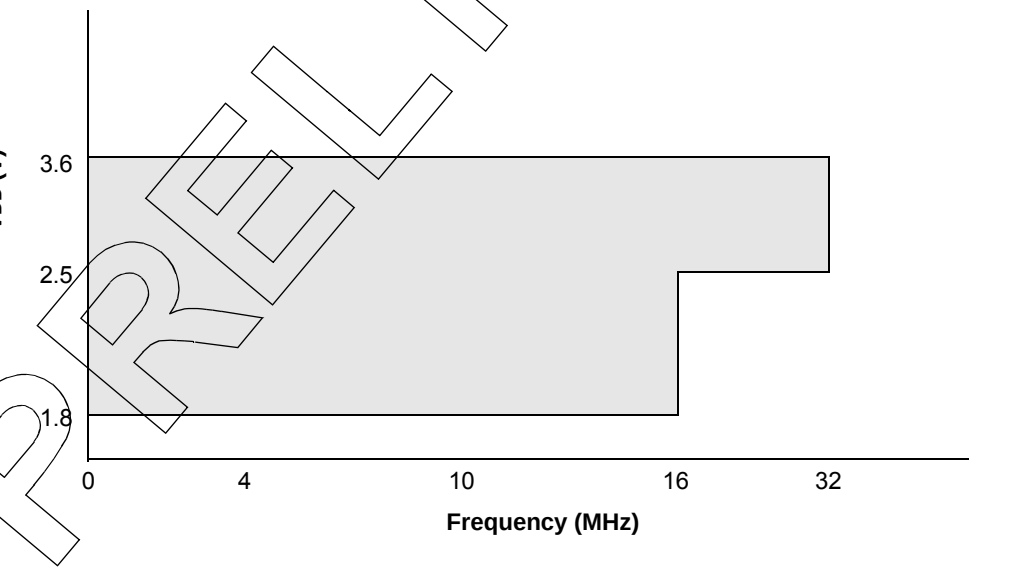
3: See Table in the MOVIW and MOVWI instruction descriptions.

FIGURE 37-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16F15356/75/76/85/86 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 37-7 for each Oscillator mode's supported frequencies.

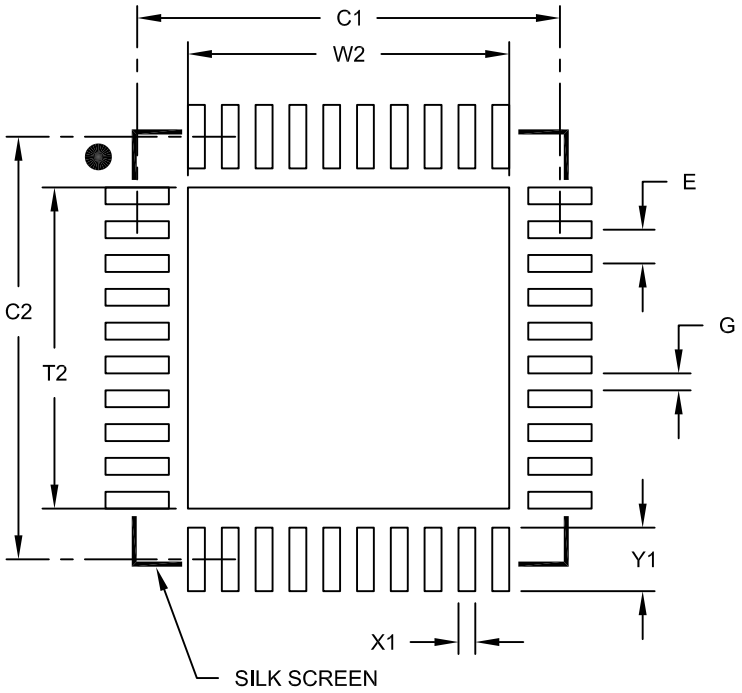
FIGURE 37-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16LF15356/75/76/85/86 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 37-7 for each Oscillator mode's supported frequencies.

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

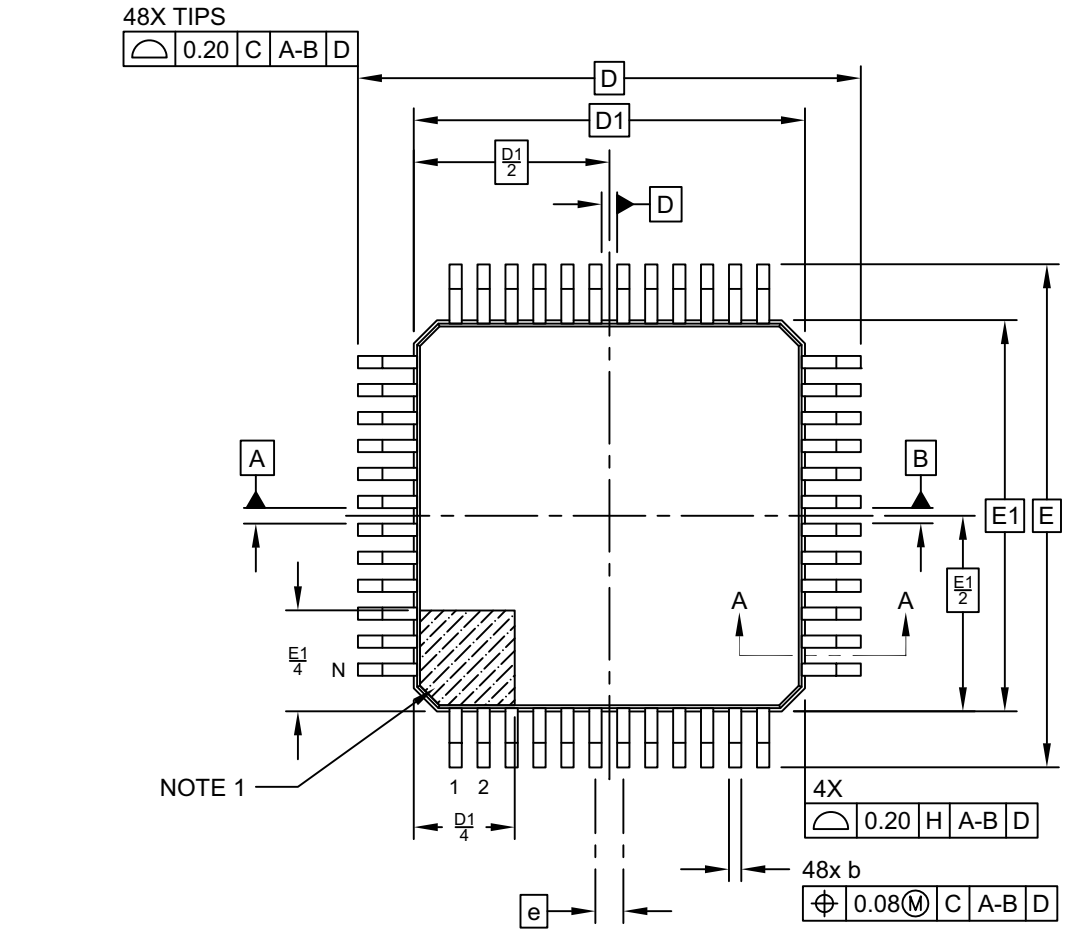
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

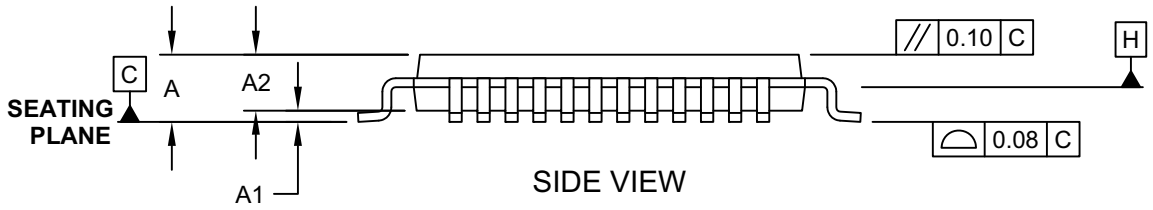
Microchip Technology Drawing No. C04-2156B

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-300-PT Rev A Sheet 1 of 2