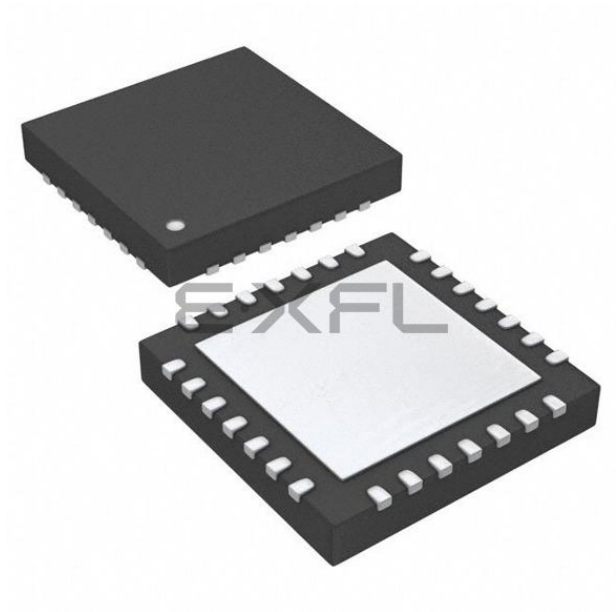


**Welcome to E-XFL.COM**

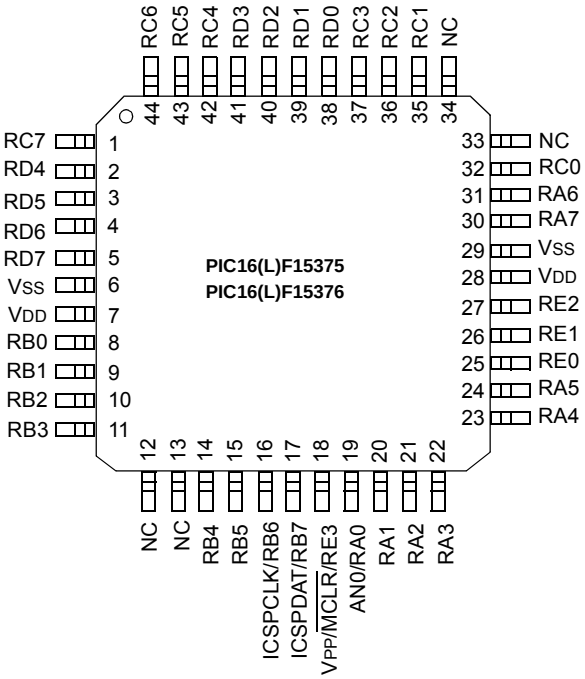
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 28KB (16K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 224 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15356t-i-ml |

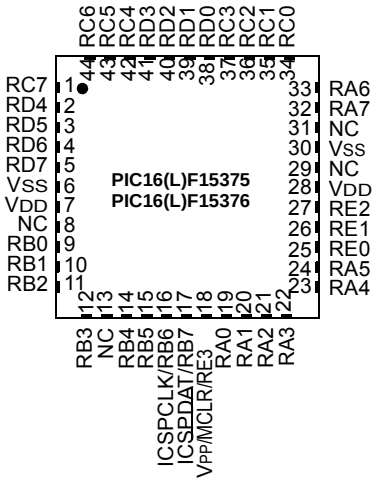
**44-PIN TQFP (10x10)**




**Note 1:** See Table 4 for location of all peripheral functions.

**2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

**44-PIN QFN (8x8x0.9)**




**Note 1:** See Table 4 for location of all peripheral functions.

**2:** All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to fl may result in degraded electrical performance or non-functionality.

**3:** The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

**TABLE 1-2: PIC16(L)F15356 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB3/ANB3/C1IN2-/C2IN2-/IOCB3 | RB3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB3 | AN | — | ADC Channel B3 input. |
| | C1IN2- | AN | — | Comparator 1 negative input. |
| | C2IN2- | AN | — | Comparator 2 negative input. |
| | IOCB3 | TTL/ST | — | Interrupt-on-change input. |
| RB4/ANB4/ADACT(1)/IOCB4 | RB4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB4 | AN | — | ADC Channel B4 input. |
| | ADACT(1) | TTL/ST | — | ADC Auto-Conversion Trigger input. |
| | IOCB4 | TTL/ST | — | Interrupt-on-change input. |
| RB5/ANB5/T1G(1)/IOCB5 | RB5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB5 | AN | — | ADC Channel B5 input. |
| | T1G(1) | ST | — | Timer1 Gate input. |
| | IOCB5 | TTL/ST | — | Interrupt-on-change input. |
| RB6/ANB6/CLCIN2(1)/IOCB6/TX2/CK2(3)/ICSPCLK | RB6 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB6 | AN | — | ADC Channel B6 input. |
| | CLCIN2(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCB6 | TTL/ST | — | Interrupt-on-change input. |
| | TX2 | — | CMOS | EUSART2 asynchronous. |
| | CK2(3) | TTL/ST | CMOS/OD | EUSART2 synchronous mode clock input/output. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming™ and debugging clock input. |
| RB7/ANB7/RX2/DT2/CLCIN3(1)/IOCB7/DAC1OUT2/ICSPDAT | RB7 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB7 | AN | — | ADC Channel B7 input. |
| | CLCIN3(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCB7 | TTL/ST | — | Interrupt-on-change input. |
| | RX2(1) | TTL/ST | — | EUSART2 Asynchronous mode receiver data input. |
| | DT2(3) | TTL/ST | CMOS/OD | EUSART2 Synchronous mode data input/output. |
| | DAC1OUT2 | — | AN | Digital-to-Analog Converter output. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming™ and debugging data input/output. |
| RC0/ANC0/T1CKI(1)/IOCC0/SOSCO | RC0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC0 | AN | — | ADC Channel C0 input. |
| | T1CKI(1) | TTL/ST | — | Timer1 external digital clock input. |
| | IOCC0 | TTL/ST | — | Interrupt-on-change input. |
| | SOSCO | — | AN | 32.768 kHz secondary oscillator crystal driver output. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 1-3: PIC16(L)F15375/76 PINOUT DESCRIPTION**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RA0/ANA0/C1IN0-/C2IN0-/CLCIN0(1)/IOCA0 | RA0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA0 | AN | — | ADC Channel A0 input. |
| | C1IN0- | AN | — | Comparator negative input. |
| | C2IN0- | AN | — | Comparator negative input. |
| | CLCIN0(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCA0 | TTL/ST | — | Interrupt-on-change input. |
| RA1/ANA1/C1IN1-/C2IN1-/CLCIN1(1)/IOCA1 | RA1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA1 | AN | — | ADC Channel A1 input. |
| | C1IN1- | AN | — | Comparator negative input. |
| | C2IN1- | AN | — | Comparator negative input. |
| | CLCIN1(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | IOCA1 | TTL/ST | — | Interrupt-on-change input. |
| RA2/ANA2/C1IN0+/C2IN0+/DAC1OUT1/IOCA2 | RA2 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA2 | AN | — | ADC Channel A2 input. |
| | C1IN0+ | AN | — | Comparator positive input. |
| | C2IN0+ | AN | — | Comparator positive input. |
| | DAC1OUT1 | — | AN | Digital-to-Analog Converter output. |
| | IOCA2 | TTL/ST | — | Interrupt-on-change input. |
| RA3/ANA3/C1IN1+/VREF+/DACREF+/IOCA3 | RA3 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA3 | AN | — | ADC Channel A3 input. |
| | C1IN1+ | AN | — | Comparator positive input. |
| | VREF+ | AN | — | External ADC and/or DAC positive reference input. |
| | IOCA3 | TTL/ST | — | Interrupt-on-change input. |
| RA4/ANA4/T0CKI(1)/IOCA4 | RA4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA4 | AN | — | ADC Channel A4 input. |
| | T0CKI(1) | TTL/ST | — | Timer0 clock input. |
| | IOCA4 | TTL/ST | — | Interrupt-on-change input. |
| RA5/ANA5/$\overline{SS1}$(1)/T1G(1)/IOCA5 | RA5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANA5 | AN | — | ADC Channel A5 input. |
| | $\overline{SS1}$(1) | TTL/ST | — | MSSP1 SPI slave select input. |
| | T1G(1) | TTL/ST | — | Timer1 gate input. |
| | IOCA5 | TTL/ST | — | Interrupt-on-change input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-5, Table 15-6 and Table 15-6.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on: MCLR |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 62 (Continued)** | | | | | | | | | | | |
| 1F2Ah | RD2PPS(1) | — | — | — | RD2PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F2Bh | RD3PPS(1) | — | — | — | RD3PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F2Ch | RD4PPS(1) | — | — | — | RD4PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F2Dh | RD5PPS(1) | — | — | — | RD5PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F2Eh | RD6PPS(1) | — | — | — | RD6PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F2Fh | RD7PPS(1) | — | — | — | RD7PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F30h | RE0PPS | — | — | — | RD5PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F31h | RE1PPS | — | — | — | RD6PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F32h | RE2PPS | — | — | — | RD7PPS<4:0> | | | | | --00 0000 | --uu uuuu |
| 1F33h — 1F37h | — | Unimplemented | | | | | | | | — | — |

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.
**Note 1:** Present only on PIC16(L)F15375/76/85/86.

© 2016 Microchip Technology Inc.

**REGISTER 9-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-q/q | R/W-q/q | R/W-q/q |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | HFFRQ<2:0>(1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **HFFRQ<2:0>:** HFINTOSC Frequency Selection bits
Nominal Freq (MHz):
111 = Reserved
110 = 32
101 = 16
100 = 12
011 = 8
010 = 4
001 = 2
000 = 1

**Note 1:** When RSTOSC=110 (HFINTOSC 1 MHz), the HFFRQ bits will default to '010' upon Reset; when RSTOSC = 001 (HFINTOSC 32 MHz), the HFFRQ bits will default to '101' upon Reset.

**REGISTER 10-9: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7**

| U-0 | U-0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | NVMIE | NCO1IE | — | — | — | CWG1IE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HS = Hardware set |

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **NVMIE:** NVM Interrupt Enable bit
- 1 = NVM task complete interrupt enabled
- 0 = NVM interrupt not enabled

bit 4 **NCO1IE:** NCO Interrupt Enable bit
- 1 = NCO rollover interrupt enabled
- 0 = NCO rollover interrupt disabled

bit 3-1 **Unimplemented:** Read as '0'.

bit 0 **CWG1IE:** Complementary Waveform Generator (CWG) 2 Interrupt Enable bit
- 1 = CWG1 interrupt is enabled
- 0 = CWG1 interrupt disabled

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE7.

**REGISTER 10-14: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W/HS-0/0 | R/W/HS-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | TMR2IF | TMR1IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | HS = Hardware set |

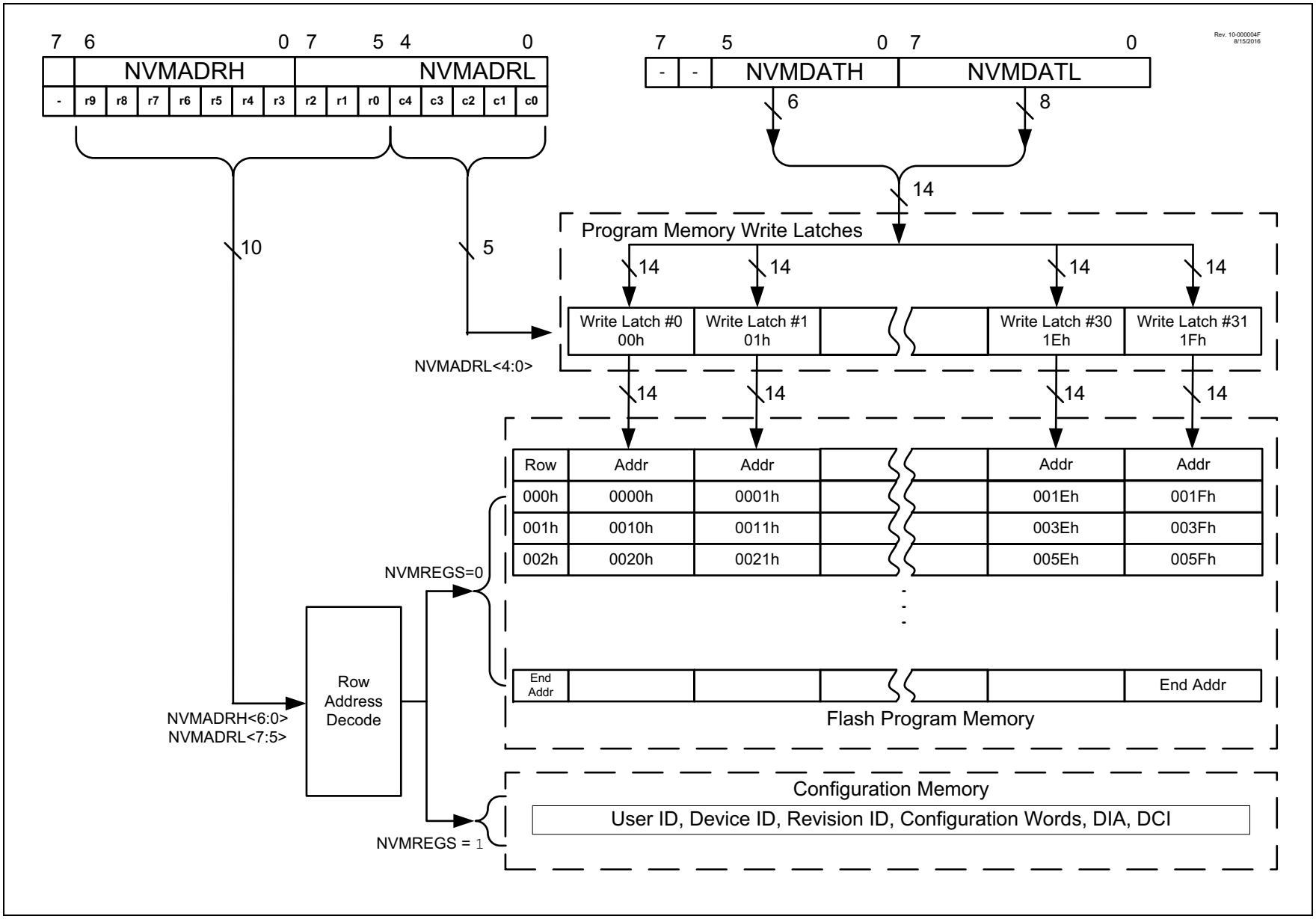
bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **TRM2IF:** Timer2 Interrupt Flag bit
1 = The TMR2 postscaler overflowed, or in 1:1 mode, a TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 event has occurred

bit 0 **TRM1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 overflow occurred (must be cleared in software)
0 = No Timer1 overflow occurred

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**FIGURE 13-4: NVMREGS WRITES TO PROGRAM FLASH MEMORY WITH 32 WRITE LATCHES**




© 2016 Microchip Technology Inc.

## 14.11 Register Definitions: PORTE

**REGISTER 14-33: PORTE: PORTE REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-x/u | R-x/u | R-x/u | R-x/u |
|---|---|---|---|---|---|---|---|
| — | — | — | — | RE3 | RE2(1) | RE1(1) | RE0(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **RE<3:0>**: PORTE Input Pin bits
1 = Port pin is > VIH
0 = Port pin is < VIL

**Note 1:** Present on PIC16(L)F15375/76/85/86 only.

**REGISTER 14-34: TRISE: PORTE TRI-STATE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | —(2) | TRISE2(1) | TRISE1(1) | TRISE0(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **Unimplemented:** Read as '1'

bit 2-0 **TRISA<2:0>:** PORTA Tri-State Control bit(1)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

**Note 1:** Present on PIC16(L)F15375/76/85/86 only.
**2:** Unimplemented, read as '1'.

## 20.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 20-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

**FIGURE 20-1: ADC BLOCK DIAGRAM**

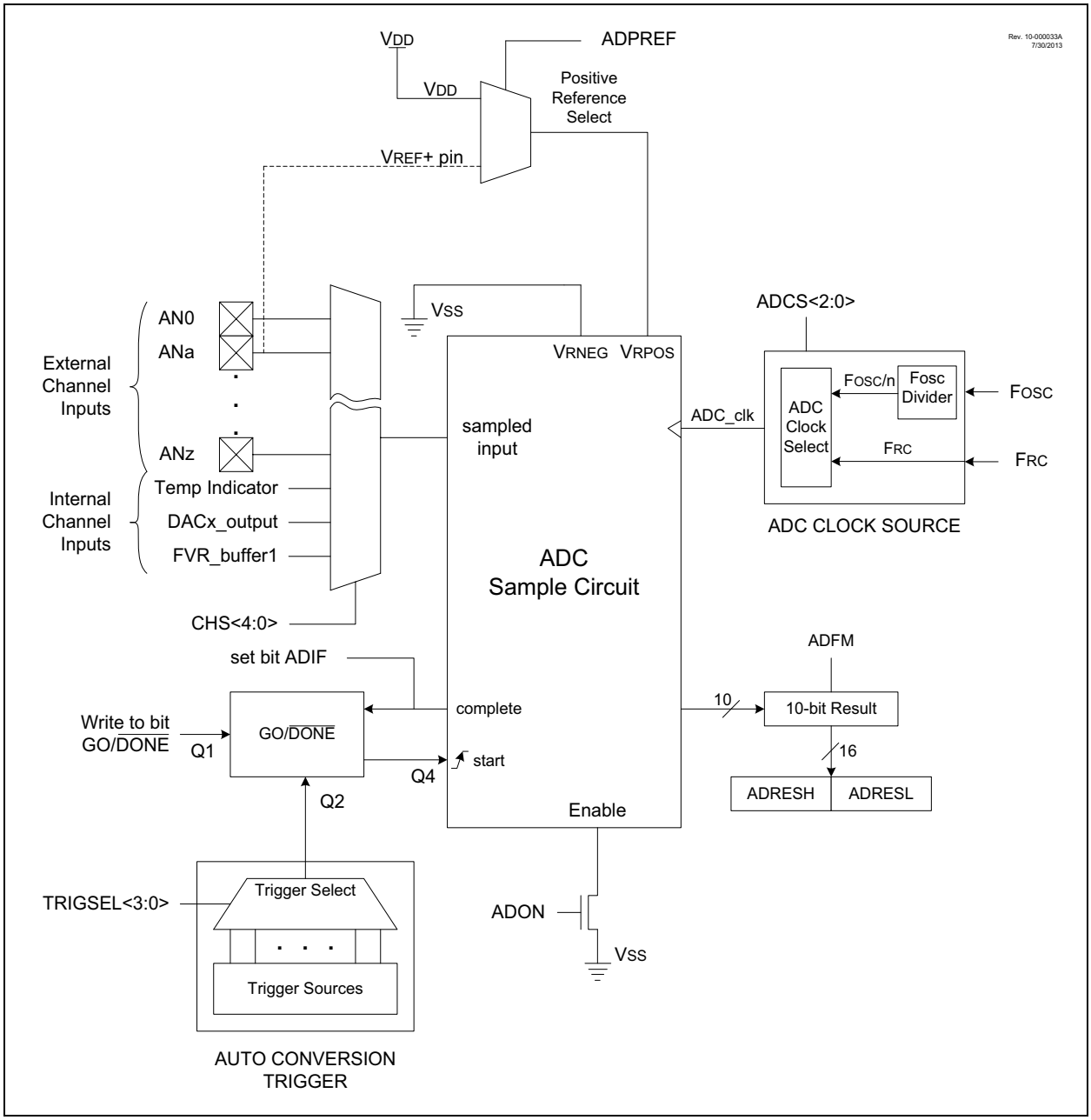
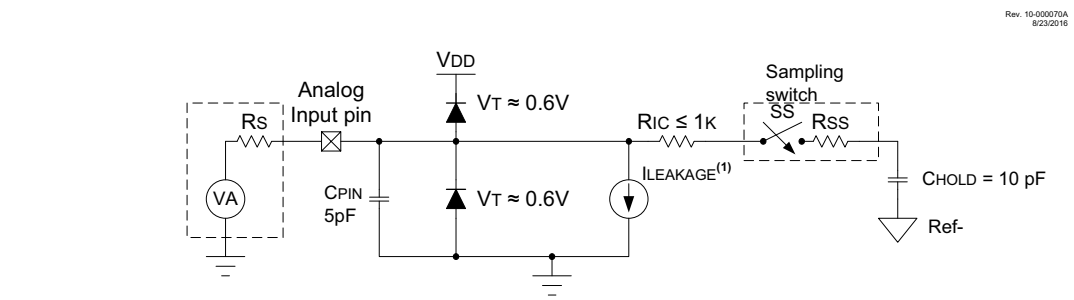
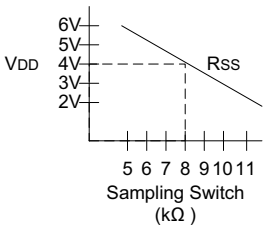


**FIGURE 20-4: ANALOG INPUT MODEL**




**Legend:** CHOLD = Sample/Hold Capacitance
CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to varies injunctions
RIC = Interconnect Resistance
RSS = Resistance of Sampling switch
SS = Sampling Switch
VT = Threshold Voltage
RS = Source Resistance




**Note 1:** See Refer to **Section 37.0 "Electrical Specifications"**.

**FIGURE 20-5: ADC TRANSFER FUNCTION**

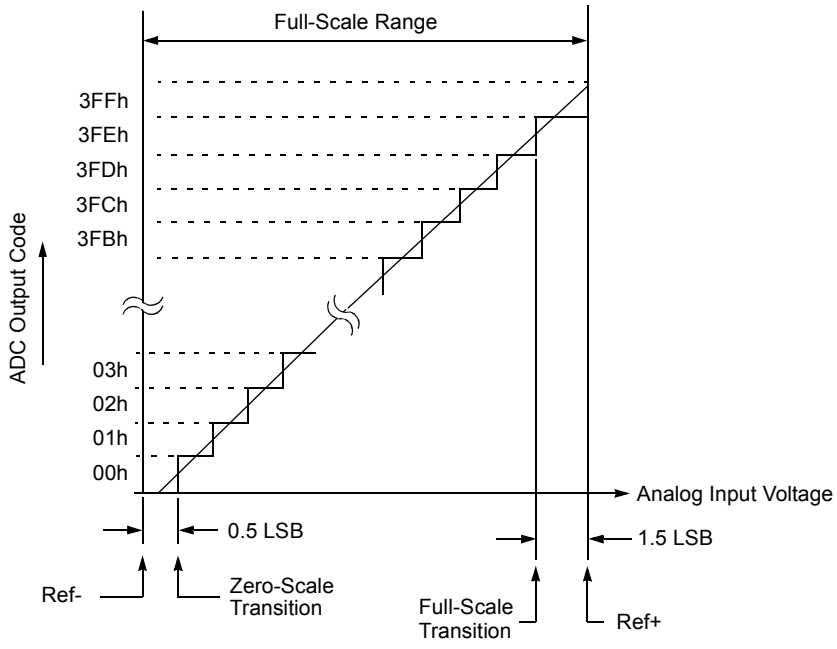


**FIGURE 25-1: BLOCK DIAGRAM OF TIMER0**

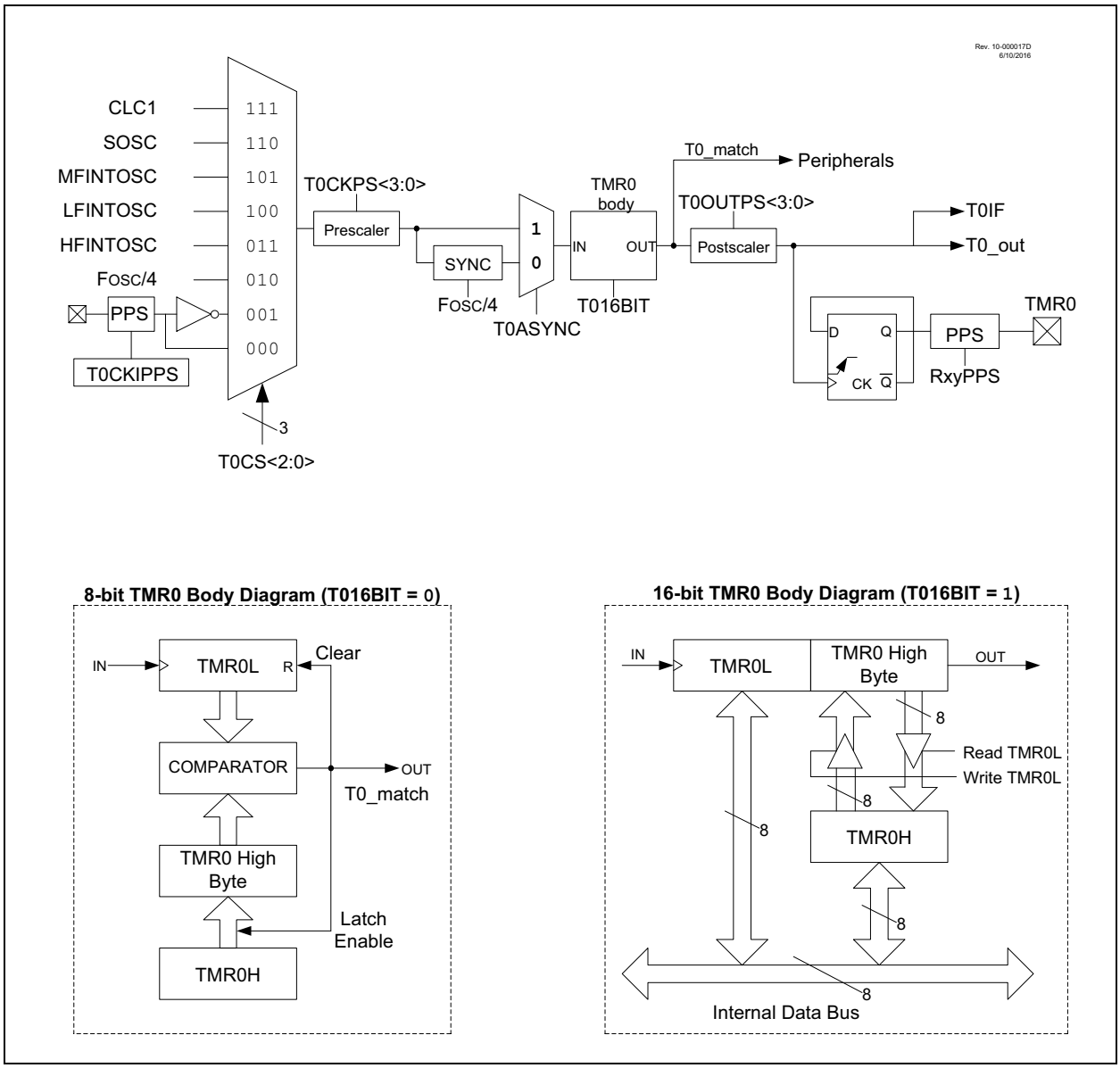
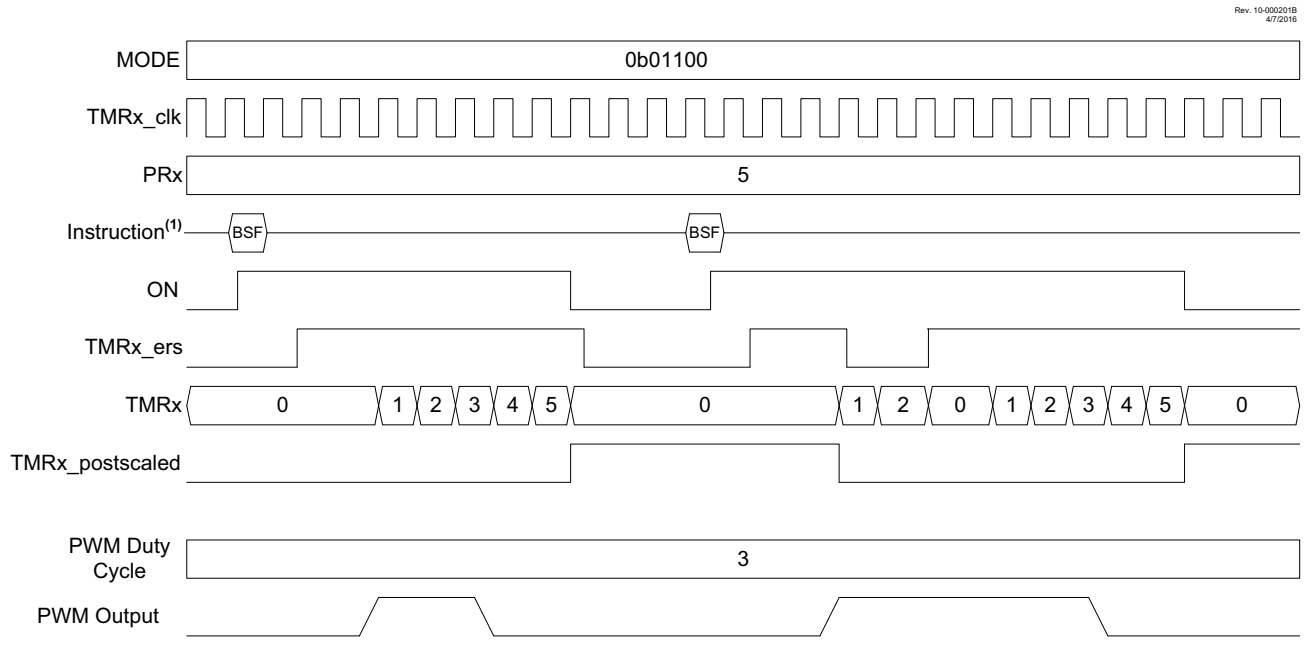


**FIGURE 27-10: EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01100)**




Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

© 2016 Microchip Technology Inc.

#### 28.2.1 CCPX PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more details.

The CCP output can also be used as an input for other peripherals.

| | |
|---|---|
| **Note:** | Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch. |

#### 28.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 26.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

| | |
|---|---|
| **Note:** | Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source. |

#### 28.2.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set and a match occurs, an Auto-conversion Trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to **Section 20.2.5 "Auto-Conversion Trigger"** for more information.

| | |
|---|---|
| **Note:** | Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring |

#### 28.2.4 COMPARE DURING SLEEP

Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

### 28.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 28-3 shows a typical waveform of the PWM signal.

#### 28.3.1 STANDARD PWM OPERATION

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 28-4 shows a simplified block diagram of PWM operation.

| | |
|---|---|
| **Note:** | The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin. |

**FIGURE 28-3: CCP PWM OUTPUT SIGNAL**

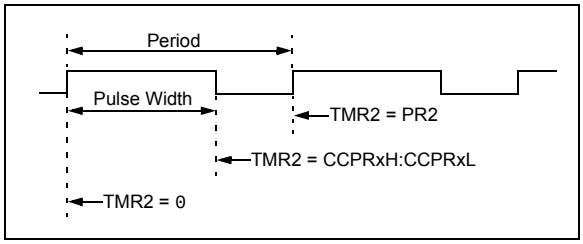


**FIGURE 30-13: SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (REN = 0, LSAC = 01, LSBD = 01)**

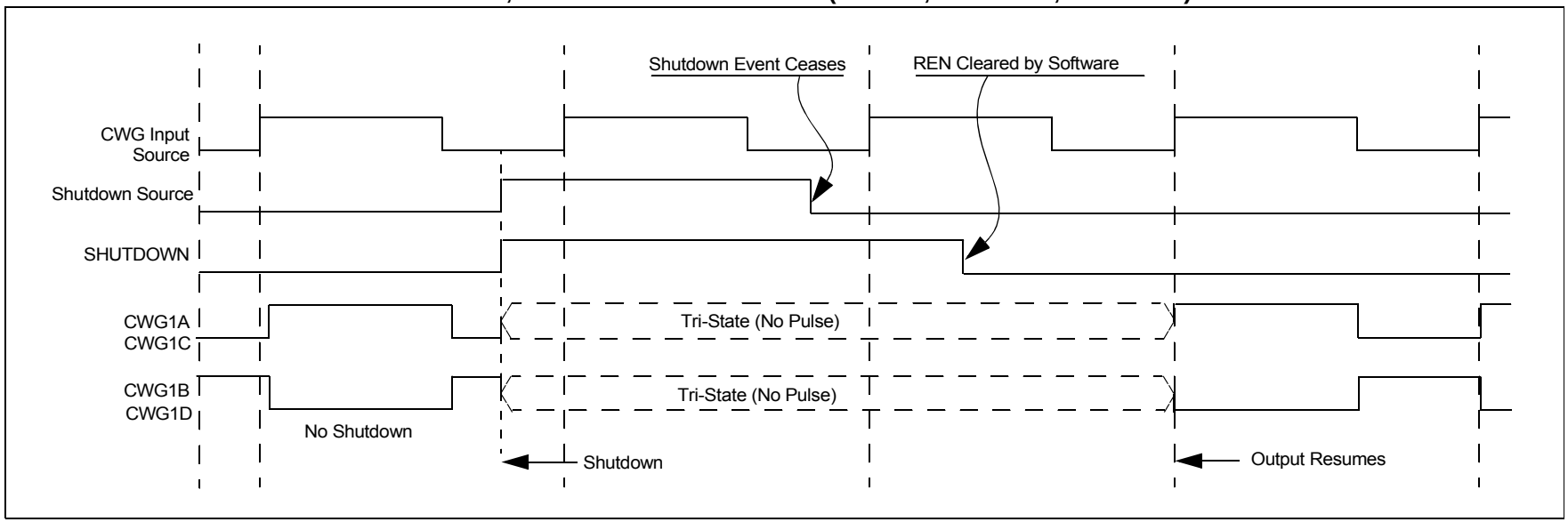
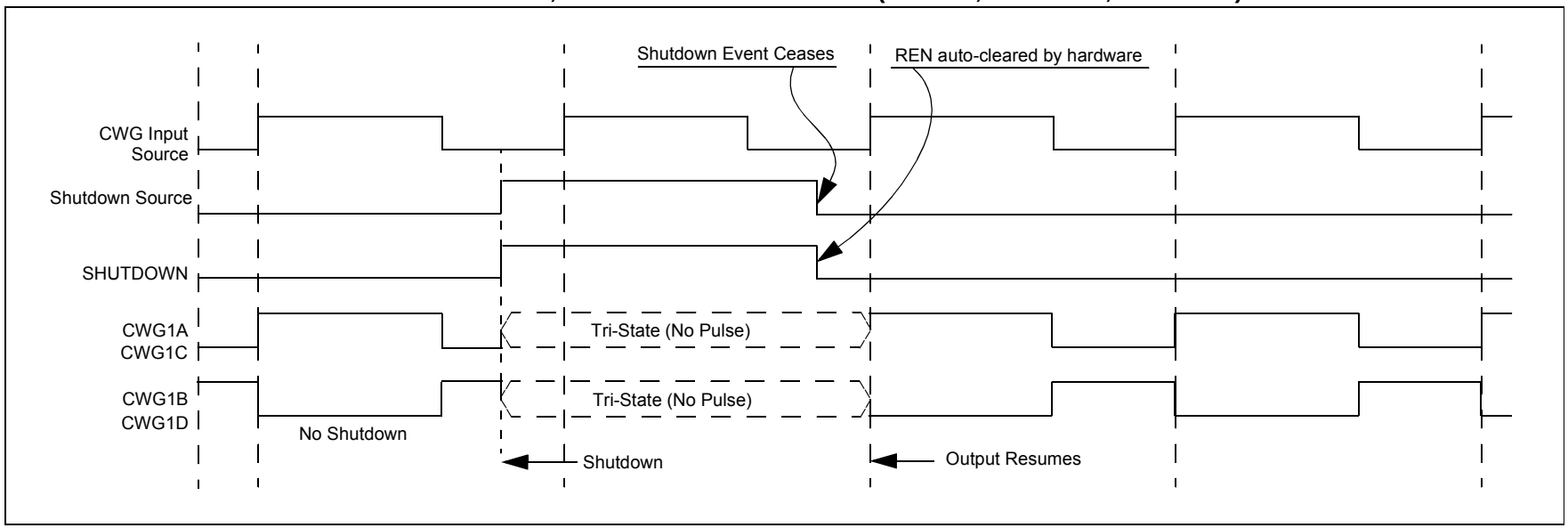



**FIGURE 30-14: SHUTDOWN FUNCTIONALITY, AUTO-RESTART ENABLED (REN = 1, LSAC = 01, LSBD = 01)**




© 2016 Microchip Technology Inc.

### 32.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 32-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

**Note 1:** If RSEN is programmed while any other event is in progress, it will not take effect.

**2:** A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

**FIGURE 32-27: REPEATED START CONDITION WAVEFORM**

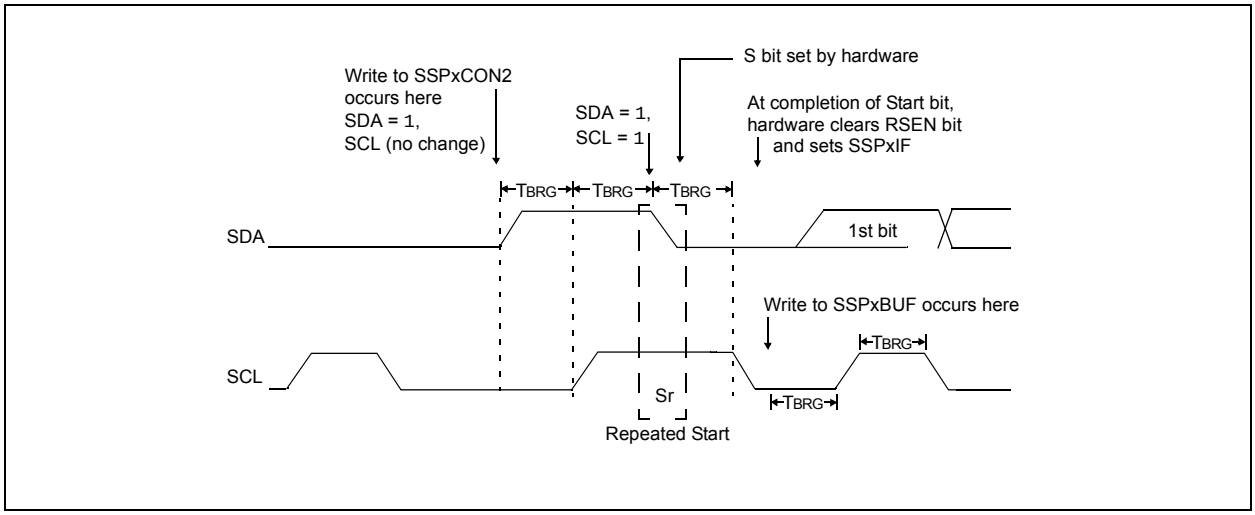
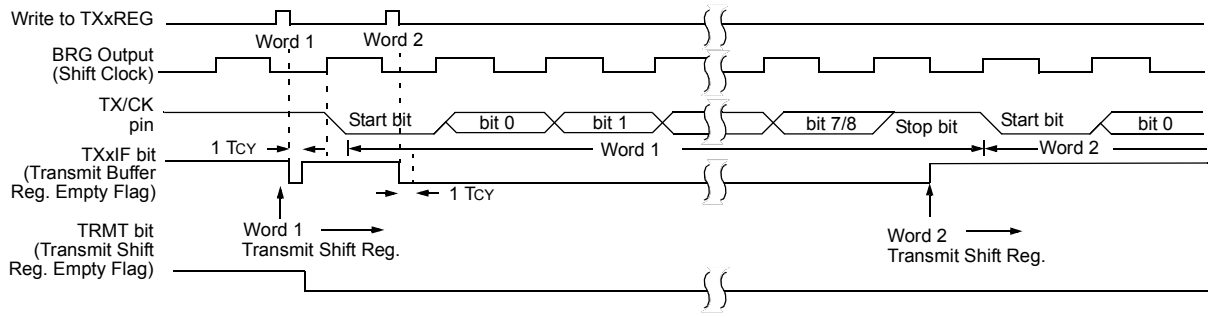


**FIGURE 33-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)**




**Note:** This timing diagram shows two consecutive transmissions.

### 33.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 33-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCxREG register.

#### 33.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCxSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXxSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCxSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

| **Note:** | If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function. |
|---|---|

#### 33.1.2.2 Receiving Data

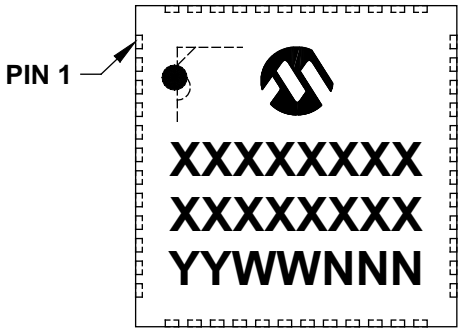
The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 33.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RXxIF interrupt flag bit of the PIR3 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCxREG register.

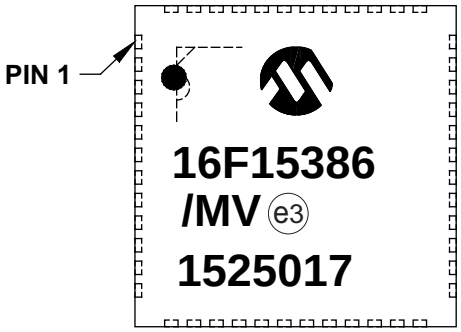
| **Note:** | If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 33.1.2.5 "Receive Overrun Error"** for more information on overrun errors. |
|---|---|

### 40.1 Package Marking Information (Continued)

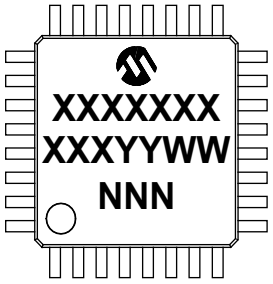
48-Lead UQFN (6x6x0.5 mm)



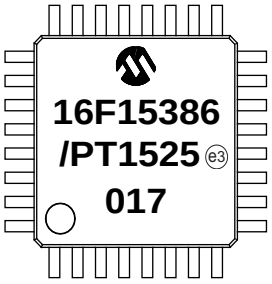

Example




48-Lead TQFP (7x7x1 mm)




Example

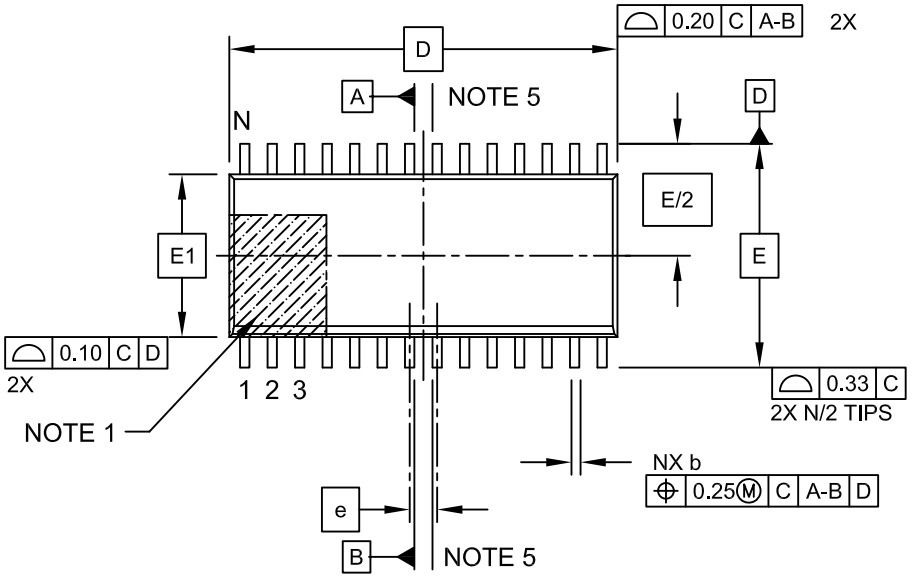



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

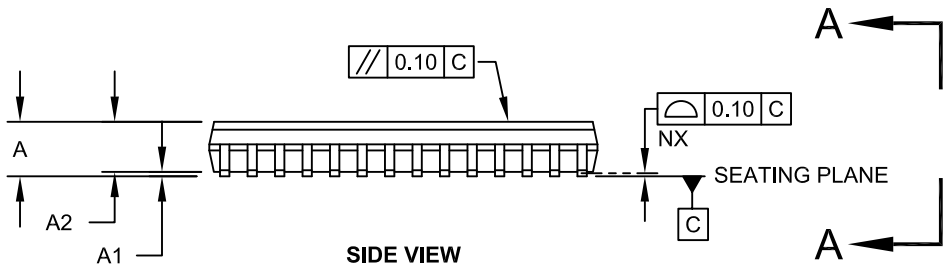
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

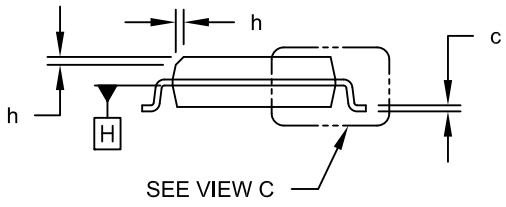
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**

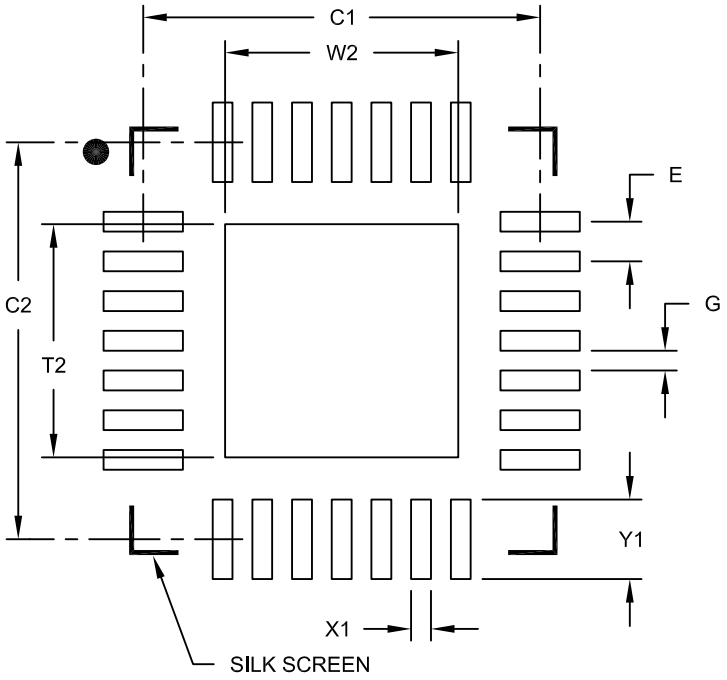



**VIEW A-A**

Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Optional Center Pad Width | W2 | | | 2.35 |
| Optional Center Pad Length | T2 | | | 2.35 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Spacing | C2 | | 4.00 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A