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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15376-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RA6/ANA6/CLKOUT/IOCA6/OSC1	RA6	TTL/ST	CMOS/OD	General purpose I/O.
	ANA6	AN	_	ADC Channel A6 input.
	CLKOUT	_	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	IOCA6	TTL/ST	_	Interrupt-on-change input.
	OSC1	XTAL	_	External Crystal/Resonator (LP, XT, HS modes) driver input.
RA7/ANA7/CLKIN/IOCA7/OSC2	RA7	TTL/ST	CMOS/OD	General purpose I/O.
	ANA7	AN	—	ADC Channel A7 input.
	CLKIN	TTL/ST	_	External digital clock input.
	IOCA7	TTL/ST	_	Interrupt-on-change input.
	OSC2	_	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
$\frac{\text{RB0/ANB0/C2IN1+/ZCD1/\overline{SS2}^{(1)}}{(1)}}{(1)}$	RB0	TTL/ST	CMOS/OD	General purpose I/O.
CWG1 ¹ //INT ¹ //IOCB0	ANB0	AN	_	ADC Channel B0 input.
	C2IN1+	AN	_	Comparator positive input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/source).
	SS2 ⁽¹⁾	TTL/ST	_	MSSP2 SPI slave select input.
	CWG1 ⁽¹⁾	TTL/ST	_	Complementary Waveform Generator 1 input.
	INT ⁽¹⁾	TTL/ST	_	External interrupt request input.
	IOCB0	TTL/ST	_	Interrupt-on-change input.
RB1/ANB1/C1IN3-/C2IN3-/	RB1	TTL/ST	CMOS/OD	General purpose I/O.
SULT VSUKT VIUCBT	ANB1	AN	_	ADC Channel B1 input.
	C1IN3-	AN	_	Comparator negative input.
	C2IN3-	AN	_	Comparator negative input.
	SCL1 ⁽¹⁾	I ² C	OD	MSSP1 I ² C input/output.
	SCK1 ⁽¹⁾	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	IOCB1	TTL/ST	—	Interrupt-on-change input.
RB2/ANB2/SDA1 ⁽¹⁾ /SDI1 ⁽¹⁾ /IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA1 ⁽¹⁾	I ² C	OD	MSSP1 I ² C serial data input/output.
	SDI1 ⁽¹⁾	TTL/ST	_	MSSP1 SPI serial data input (default input location, SDI1 is a PPS remappable input and output).
	IOCB2	TTL/ST	—	Interrupt-on-change input.
RB3/ANB3/C1IN2-/C2IN2-/IOCB3	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	ANB3	AN	—	ADC Channel B3 input.
	C1IN2-	AN	_	Comparator negative input.
	C2IN2-	AN	_	Comparator negative input.
	IOCB3	TTL/ST	_	Interrupt-on-change input.

TABLE 1-3: PIC16(L)F15375/76 PINOUT DESCRIPTION (CONTINUED)

TTL = TTL compatible input HV = High Voltage

= Schmitt Trigger input with CMOS levels

I²C = Schmitt Trigger input with I²C

Note

= Crystal levels XTAL This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal. 1:

All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options 2: as described in Table 15-5, Table 15-6 and Table 15-6.

This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and 3: PPS output registers.

4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

IADLE 4	ABLE 4-11. SPECIAL FUNCTION REGISTER SUMMART BANKS 0-03 (CONTINUED)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR
Bank 19	lank 19										
	CPU CORE REGISTERS; see Table 4-3 for specifics										
98Ch	_				Unimple	mented					_
98Dh	_				Unimple	mented				_	—
98Eh	_				Unimple	mented				—	—
98Fh	CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	00	00
990h	CM1CON0	EN	OUT	—	POL	—	—	HYS	SYNC	00-000	00-000
991h	CM1CON1	—	—	—	—	—	—	INTP	INTN	00	00
992h	CM1NCH	—	—	—	—	—		NCH<2:0>		000	000
993h	CM1PCH	—	—	—	—	—		PCH<2:0>		000	000
994h	CM2CON0	EN	OUT	—	POL	—	—	HYS	SYNC	00-000	00-000
995h	CM2CON1	—	—	—	—	—	—	INTP	INTN	00	00
996h	CM2NCH	—	—	—	—	—		NCH<2:0>	000	000	
997h	CM2PCH	PCH — — — — PCH<2:0>					000	000			
998hUnimplemented							-	_			

TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

6.1 Microchip Unique identifier (MUI)

The PIC16(L)F15356/75/76/85/86 devices are individually encoded during final manufacturing with a Microchip Unique Identifier, or MUI. The MUI cannot be erased by a Bulk Erase command or any other useraccessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a required. It may also be used by the application manufacturer for a number of functions that require unverified unique identification, such as:

- · Tracking the device
- Unique serial number

The MUI consists of nine program words. When taken together, these fields form a unique identifier. The MUI is stored in nine read-only locations, located between 8100h to 8109h in the DIA space. Table 6-1 lists the addresses of the identifier words.

Note:	For applications that require verified unique
	identification, contact your Microchip Tech-
	nology sales office to create a Serialized
	Quick Turn Programming option.

6.2 External Unique Identifier (EUI)

The EUI data is stored at locations 810Ah to 8111h in the program memory region. This region is an optional space for placing application specific information. The data is coded per customer requirements during manufacturing. The EUI cannot be erased by a Bulk Erase command.

Note: Data is stored in this address range on receiving a request from the customer. The customer may contact the local sales representative or Field Applications Engineer, and provide them the unique identifier information that is required to be stored in this region.

6.3 Analog-to-Digital Conversion Data of the Temperature Sensor

The purpose of the temperature indicator module is to provide a temperature-dependent voltage that can be measured by an analog module. **Section 19.0 "Temperature Indicator Module**" explains the operation of the Temperature Indicator module and defines terms such as the low range and high range settings of the sensor.

The DIA table contains the internal ADC measurement values of the temperature sensor for low and high range at fixed points of reference. The values are measured during test and are unique to each device. The right-justified ADC readings are stored in the DIA memory region. The calibration data can be used to plot the approximate sensor output voltage, VTSENSE vs. Temperature curve.

- TSLR<3:1>: Address 8112h to 8114h store the measurements for the low range setting of the temperature sensor at VDD = 3V.
- TSHR<3:1>: Address 8115h to 8117h store the measurements for the high range setting of the temperature sensor at VDD = 3V.

The stored measurements are made by the device ADC using the internal VREF = 2.048V.

6.4 Fixed Voltage Reference Data

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator positive input
- Digital-to-Analog Converter

For more information on the FVR, refer to **Section 18.0 "Fixed Voltage Reference (FVR)"**.

The DIA stores measured FVR voltages for this device in mV for the different buffer settings of 1x, 2x or 4x at program memory locations 8118h to 811Dh.

- FVRA1X stores the value of ADC FVR1 Output voltage for 1x setting (in mV)
- FVRA2X stores the value of ADC FVR1 Output Voltage for 2x setting (in mV)
- FVRA4X stores the value of ADC FVR1 Output Voltage for 4x setting (in mV)
- FVRC1X stores the value of Comparator FVR2 output voltage for 1x setting (in mV)
- FVRC2X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC4X stores the value of Comparator FVR2 output voltage for 4x setting (in mV)

9.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

9.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 9-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz-crystal resonators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The RSTOSC bits of Configuration Word 1 determine the type of oscillator that will be used when the device reset, including when it is first powered up.

The internal clock modes, LFINTOSC, HFINTOSC (set at 1 MHz), or HFINTOSC (set at 32 MHz) can be set through the RSTOSC bits.

If an external clock source is selected, the FEXTOSC bits of Configuration Word 1 must be used to select the external clock mode.

The external oscillator module can be configured in one of the following clock modes, by setting the FEXTOSC<2:0> bits of Configuration Word 1:

- 1. ECL External Clock Low-Power mode ECL<= 500 kHz
- 2. ECM External Clock Medium Power mode ECM <= 8 MHz
- 3. ECH External Clock High-Power mode ECH <= 32 MHz
- 4. LP 32 kHz Low-Power Crystal mode.
- 5. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode (between 100 kHz and 4 MHz)
- HS High Gain Crystal or Ceramic Resonator mode (above 4 MHz)

The ECH, ECM, and ECL clock modes rely on an external logic level signal as the device clock source. The LP, XT, and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The INTOSC internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC. (see Internal Oscillator Block, Figure 9-1). A wide selection of device clock frequencies may be derived from these clock sources.

PIC16(L)F15356/75/76/85/86

	-R IU-13: PIK3:				I REGISTER		
R/W/HS-	-0/0 R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
RC2IF	F TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF
bit 7							bit (
Legend:							
R = Read	able bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all ot							other Resets
'1' = Bit is	set	'0' = Bit is clea	ared	HS = Hardwa	are clearable		
L:1 7					(1)		
DIT /	1 - The EUSA	ARIZ Receive I	nterrupt Flag	(Read-Only) b moty (contains	iti'''	to)	
	1 = The EUS 0 = The EUS	ART2 receive	buffer is empty	v (Contains	at least one by	le)	
bit 6	TX2IF: EUSA	RT2 Transmit	nterrupt Flag	, (Read-Only) b	it ⁽²⁾		
	1 = The EUS	ART2 transmit	buffer contain	is at least one	unoccupied spa	ice	
	0 = The EUS	SART2 transmi	t buffer is cu	rrently full. Th	ne application fi	rmware shoul	d not write to
	TXxREG				(1)		
bit 5	RC1IF: EUSA	ART1 Receive I	nterrupt Flag	(read-only) bit	(') 	L- \	
	1 = The EUS 0 = The FUS	ART1 receive	buffer is not ei buffer is empty	mpty (contains v	at least one by	(e)	
bit 4	TX1IF: EUSA	RT1 Transmit	nterrupt Flag	, (read-onlv) bit	(2)		
	1 = The EUS	SART1 transmi	t buffer contai	ns at least one	unoccupied spa	ace	
	0 = The EU	SART1 transm	it buffer is cu	irrently full. Th	ne application f	irmware shoul	d not write to
	TXxREG	again, until m	ore room becc	omes available	in the transmit	buffer.	
bit 3	BCL2IF: MSS	SP2 Bus Collisi	on Interrupt Fl	lag bit			
	1 = A bus coll $0 = No bus coll$	lision was dete	cted (must be ected	cleared in som	(ware)		
bit 2	SSP2IF: Svn	chronous Seria	l Port (MSSP2	2) Interrupt Fla	a bit		
~~ _	1 = The Tran	smission/Rece	ption/Bus Cor	dition is comp	lete (must be cl	eared in softwa	are)
	0 = Waiting f	or the Transmis	ssion/Reception	on/Bus Conditi	on in progress		,
bit 1	BCL1IF: MSS	SP1 Bus Collisi	on Interrupt Fl	lag bit			
	1 = A bus co	llision was dete	cted (must be	e cleared in sof	ftware)		
		ollision was de	tected				
bit 0	SSP1IF: Synd	chronous Seria	I Port (MSSP1	I) Interrupt Fla	g bit lata (muat ha al	oarad in aaffuur	
	1 = The tran 0 = Waiting f	or the Transmis	sion/Receptic	on/Bus Conditi	on in progress	eared in sollwa	are)
Note 1.		a road only hit			firmuoro muot	road from DCv	
Note 1:	times to remove al	l bytes from the	e receive buffe	er.	inniware must	read from RCX	REG enough
2:	The TXxIF flag is a	a read-only bit,	indicating if th	ere is room in	the transmit but	fer. To clear th	e TX1IF flag,
	the firmware must	write enough d	ata to TXxRE	G to complete	ly fill all available	e bytes in the b	ouffer. The
	TXxIF flag does no	ot indicate trans	smit completio	n (use TRMT	for this purpose	instead).	
Note:	Interrupt flag bits a	re set when an	interrupt				
	condition occurs, r	egardless of the	e state of				
	its corresponding	enable bit or th	e Global				
	Enable bit, GIE, c	should encu	register.				
	appropriate interri	upt flag bits a	are clear				

prior to enabling an interrupt.

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PIC16(L)F15356/75/76/85/86

REGISTER 1	1-2: CPUDOZ	E: DOZE AN	D IDLE REG	ISTER			
R/W-0/u	R/W/HC/HS-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
IDLEN	DOZEN ^(1,2)	ROI	DOE	_		DOZE<2:0>	
bit 7	•				•		bit 0
r							
Legend:							
R = Readable	bit	W = Writable	oit	U = Unimple	emented bit, r	ead as '0'	
u = Bit is unch	anged	x = Bit is unkn	own	-n/n = Value Resets	at POR and	BOR/Value at a	III other
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	IDLEN: Idle Enal 1 = A SLEEP ins 0 = A SLEEP ins	ble bit truction inhibits truction places	the CPU cloo	ck, but not the to full Sleep m	peripheral cl lode	ock(s)	
bit 6	DOZEN: Doze E 1 = The CPU ex 0 = The CPU ex	nable bit ^(1,2) ecutes instruct ecutes all instr	ion cycles acc uction cycles	cording to DO2 (fastest, highe	ZE setting st power ope	ration)	
bit 5	 ROI: Recover-on-Interrupt bit 1 = Entering the Interrupt Service Routine (ISR) makes DOZEN = 0 bit, bringing the CPU to full-speed operation. 0 = Interrupt entry does not change DOZEN 						
bit 4	DOE: Doze on E 1 = Executing R 0 = RETFIE doe	xit bit ETFIE makes I es not change [DOZEN = 1, b DOZEN	pringing the CF	PU to reduced	d speed operati	on.
bit 3	Unimplemented	Read as '0'					
bit 2-0	DOZE<2:0>: Rat 111 =1:256 110 =1:128 101 =1:64 100 =1:32 011 =1:16 010 =1:8 001 =1:4 000 =1:2	tio of CPU Insti	ruction Cycles	to Peripheral	Instruction C	ycles	

- **Note 1:** When ROI = 1 or DOE = 1, DOZEN is changed by hardware interrupt entry and/or exit.
 - 2: Entering ICD overrides DOZEN, returning the CPU to full execution speed; this bit is not affected.

12.1 Independent Clock Source

The WDT can derive its time base from either the 31 kHz LFINTOSC or 31.25 kHz MFINTOSC internal oscillators, depending on the value of either the WDTCCS<2:0> Configuration bits or the WDTCS<2:0> bits of WDTCON1. Time intervals in this chapter are based on a minimum nominal interval of 1 ms. See **Section 37.0 "Electrical Specifications"** for LFINTOSC and MFINTOSC tolerances.

12.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 12-1.

12.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always on.

WDT protection is active during Sleep.

12.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

12.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON0 register.

12.2.4 WDT IS OFF

When the WDTE bits of the Configuration Word are set to '00', the WDT is always OFF.

WDT protection is unchanged by Sleep. See Table 12-1 for more details.

WDTE<1:0>	SWDTEN	Device Mode	WDT Mode
11	Х	Х	Active
1.0	37	Awake	Active
Ĩ	A	Sleep	Disabled
01	1	х	Active
UI	0	х	Disabled
00	х	х	Disabled

TABLE 12-1: WDT OPERATING MODES

12.3 Time-Out Period

The WDTPS bits of the WDTCON0 register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

12.4 Watchdog Window

The Watchdog Timer has an optional Windowed mode that is controlled by the WDTCWS<2:0> Configuration bits and WINDOW<2:0> bits of the WDTCON1 register. In the Windowed mode, the CLRWDT instruction must occur within the allowed window of the WDT period. Any CLRWDT instruction that occurs outside of this window will trigger a window violation and will cause a WDT Reset, similar to a WDT time out. See Figure 12-2 for an example.

The window size is controlled by the WDTCWS<2:0> Configuration bits, or the WINDOW<2:0> bits of WDTCON1, if WDTCWS<2:0> = 111.

In the event of a <u>window</u> violation, a Reset will be generated and the WDTWV bit of the PCON register will be cleared. This bit is set by a POR or can be set in firmware.

12.5 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- Valid CLRWDT instruction is executed
- · Device enters Sleep
- · Device wakes up from Sleep
- WDT is disabled
- Oscillator Start-up Timer (OST) is running
- Any write to the WDTCON0 or WDTCON1 registers

12.5.1 CLRWDT CONSIDERATIONS (WINDOWED MODE)

When in Windowed mode, the WDT must be armed before a CLRWDT instruction will clear the timer. This is performed by reading the WDTCON0 register. Executing a CLRWDT instruction without performing such an arming action will trigger a window violation.

See Table 12-2 for more information.

12.6 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting. When the device exits Sleep, the WDT is cleared again.

The WDT remains clear until the OST, if enabled, completes. See Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)" for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. The RWDT bit in the PCON register can also be used. See Section 4.3.2.1 "STATUS Register" for more information.

20.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- · Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting

20.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin will be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 14.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined							
	as a digital input may cause the input							
	buffer to conduct excess current.							

20.1.2 CHANNEL SELECTION

There are several channel selections available:

- Seven Port A channels
- Seven Port B channels
- Seven Port C channels
- Seven Port D channels⁽¹⁾
- Seven Port E channels⁽¹⁾
- Seven Port F channels⁽²⁾
- Temperature Indicator
- DAC output
- Fixed Voltage Reference (FVR)
- AVss (Ground)

Note 1: Present on PIC16(L)F15375/76/85/86 only.
 2: Present on PIC16(L)F15385/86 only.

The CHS<5:0> bits of the ADCON0 register (Register 20-1) determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 20.2** "**ADC Operation**" for more information.

20.1.3 ADC VOLTAGE REFERENCE

The ADPREF<1:0> bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be:

- VREF+ pin
- Vdd
- FVR 2.048V
- FVR 4.096V (Not available on LF devices)

The ADPREF bit of the ADCON1 register provides control of the negative voltage reference. The negative voltage reference can be:

- VREF- pin
- Vss

See **Section 18.0** "Fixed Voltage Reference (FVR)" for more details on the Fixed Voltage Reference.

20.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS<2:0> bits of the ADCON1 register. There are seven possible clock options:

- · Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- ADCRC (dedicated RC oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11.5 TAD periods as shown in Figure 20-2.

For correct conversion, the appropriate TAD specification must be met. Refer to Table 37-13 for more information. Table 20-1 gives examples of appropriate ADC clock selections.

Note: Unless using the ADCRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

25.0 TIMER0 MODULE

The Timer0 module is an 8/16-bit timer/counter with the following features:

- 16-bit timer/counter
- 8-bit timer/counter with programmable period
- Synchronous or asynchronous operation
- Selectable clock sources
- Programmable prescaler (independent of Watchdog Timer)
- Programmable postscaler
- Operation during Sleep mode
- · Interrupt on match or overflow
- Output on I/O pin (via PPS) or to other peripherals

25.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the T016BIT bit of the T0CON register.

25.1.1 16-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

25.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

TMR0H is not the actual high byte of Timer0 in 16-bit mode. It is actually a buffered version of the real high byte of Timer0, which is neither directly readable nor writable (see Figure 25-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

25.1.2 8-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

The value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

- TMR0_out goes high for one prescaled clock period
- TMR0L is reset
- The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh.

Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- <u>Any device Reset Power-on Reset (POR),</u> <u>MCLR Reset, Watchdog Timer Reset (WDTR) or</u>
- Brown-out Reset (BOR)

25.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the T0CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by '1'.

25.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the T0CKPS bits of the T0CON1 register (Register 25-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

25.1.5 ASYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is set (T0ASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

25.1.6 SYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is clear (T0ASYNC = 0), the counter clock is synchronized to the system oscillator (Fosc/4). When operating in Synchronous mode, the counter clock frequency cannot exceed Fosc/4.

25.2 Clock Source Selection

The T0CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 25-2 displays the clock source selections.

25.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

25.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.

25.3 Programmable Prescaler

A software programmable prescaler is available for exclusive use with Timer0. There are 16 prescaler options for Timer0 ranging in powers of two from 1:1 to 1:32768. The prescaler values are selected using the T0CKPS<3:0> bits of the T0CON1 register.

The prescaler is not directly readable or writable. Clearing the prescaler register can be done by writing to the TMR0L register or the T0CON1 register.

25.4 Programmable Postscaler

A software programmable postscaler (output divider) is available for exclusive use with Timer0. There are 16 postscaler options for Timer0 ranging from 1:1 to 1:16. The postscaler values are selected using the TOOUTPS<3:0> bits of the TOCON0 register.

The postscaler is not directly readable or writable. Clearing the postscaler register can be done by writing to the TMR0L register or the T0CON0 register.

25.5 Operation during Sleep

When operating synchronously, Timer0 will halt. When operating asynchronously, Timer0 will continue to increment and wake the device from Sleep (if Timer0 interrupts are enabled) provided that the input clock source is active.

25.6 Timer0 Interrupts

The Timer0 interrupt flag bit (TMR0IF) is set when either of the following conditions occur:

- 8-bit TMR0L matches the TMR0H value
- · 16-bit TMR0 rolls over from 'FFFFh'

When the postscaler bits (T0OUTPS<3:0>) are set to 1:1 operation (no division), the T0IF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every T0OUTPS +1 matches or rollovers.

If Timer0 interrupts are enabled (TMR0IE bit of the PIE0 register = 1), the CPU will be interrupted and the device may wake from sleep (see Section 25.2 "Clock Source Selection" for more details).

25.7 Timer0 Output

The Timer0 output can be routed to any I/O pin via the RxyPPS output selection register (see Section 15.0 "Peripheral Pin Select (PPS) Module" for additional information). The Timer0 output can also be used by other peripherals, such as the Auto-conversion Trigger of the Analog-to-Digital Converter. Finally, the Timer0 output can be monitored through software via the Timer0 output bit (T0OUT) of the T0CON0 register (Register 25-1).

TMR0_out will be one postscaled clock period when a match occurs between TMR0L and TMR0H in 8-bit mode, or when TMR0 rolls over in 16-bit mode. The Timer0 output is a 50% duty cycle that toggles on each TMR0_out rising clock edge.

27.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except Fosc/4 and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using Fosc/4, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 28.0 "Capture/Compare/PWM Modules"**. The signals are not a part of the Timer2 module.

27.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 27-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

27.5.5 SOFTWARE START ONE-SHOT MODE

In One-Shot mode the timer resets and the ON bit is cleared when the timer value matches the PRx period value. The ON bit must be set by software to start another timer cycle. Setting MODE<4:0> = 01000 selects One-Shot mode which is illustrated in Figure 27-8. In the example, ON is controlled by BSF and BCF instructions. In the first case, a BSF instruction sets ON and the counter runs to completion and clears ON. In the second case, a BSF instruction starts the cycle, BCF/BSF instructions turn the counter off and on during the cycle, and then it runs to completion.

When One-Shot mode is used in conjunction with the CCP PWM operation the PWM pulse drive starts concurrent with setting the ON bit. Clearing the ON bit while the PWM drive is active will extend the PWM drive. The PWM drive will terminate when the timer value matches the CCPRx pulse width value. The PWM drive will remain off until software sets the ON bit to start another cycle. If software clears the ON bit after the CCPRx match but before the PRx match then the PWM drive will be extended by the length of time the ON bit remains cleared. Another timing cycle can only be initiated by setting the ON bit after it has been cleared by a PRx period count match.

FIGURE 27-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = 01000)



27.5.6 EDGE-TRIGGERED ONE-SHOT MODE

The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0> = 01011)

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 27-9 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the PRx period count match.

FIGURE 27-9: EDGE-TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)

MODE	0b01001
TMRx_clk	
PRx	5
Instruction ⁽¹⁾ -	(BSF)(BCF)(BCF)
ON	
TMRx_ers	
TMRx	$0 \qquad 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 0 \qquad 1 \\ 2 \qquad 2$
CCP_pset	
TMRx_postscaled	
PWM Duty Cycle	3
PWM Output	

32.0 MASTER SYNCHRONOUS SERIAL PORT (MSSPx) MODULES

32.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SPI interface supports the following modes and features:

- Master mode
- · Slave mode
- Clock Parity
- Slave Select Synchronization (Slave mode only)
- · Daisy-chain connection of slave devices

Figure 32-1 is a block diagram of the SPI interface module.





32.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 32-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDA is sampled low when SCL goes from low-to-high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 32-27: REPEATED START CONDITION WAVEFORM



36.2 General Format for Instructions

TABLE 36-3:	INSTRUCTION SET

Mnemonic,		Description	Cycles		14-Bit (Opcode)	Status	Notos
Opera	ands	2000.1.0.1		MSb			LSb	Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	_	Clear W	1	00	0001	0000	00xx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2
DECF	f. d	Decrement f	1	00	0011	dfff	ffff	z	2
INCF	f. d	Increment f	1	0.0	1010	dfff	ffff	z	2
IORWE	fd	Inclusive OR W with f	1	0.0	0100	dfff	ffff	7	2
MOVE	f d	Move f	1	0.0	1000	dfff	ffff	7	2
MOVWE	f., 🕰	Move W to f	1	0.0	0000	1fff	ffff	-	2
RIF	fd	Rotate Left f through Carry	1	0.0	1101	dfff	ffff	C	2
RRF	f d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	2
SUBWE	f d	Subtract W from f	1	00	0010	dfff	ffff		2
SUDWED	i, u f d	Subtract with Borrow W/ from f	1	11	1011	JEEE		C, DC, Z	2
SUBVIE	i, u f d	Subiraci with Borrow W Ironn i	1	11	1110	arre	LILL	C, DC, Z	2
SWAFF	i, u f d	Swap hipples in I	1	00	0110	arre	LILL	7	2
JURWF	1, U				0110	aiii	IIII	2	2
	£ _				1 0 1 1	1666			4.0
DECFSZ	r, a f. d	Increment f. Skip if 0	1(2)	00	1011	dfff	ffff		1, 2
INCESZ	., -								-, _
		BIT-ORIENTED FILE REGIST			5			r	
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2
BSF	t, b	Bit Set f	1	01	01bb	bfff	ffff		2
BIT-ORIENTED SKIP OPERATIONS									
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
LITERAL OPERATIONS									
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	000	0k	kkkk		
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVIW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C DC Z	
XORIW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	7	
				l <u>+ +</u>	TOTO		17171717	<u> </u>	<u>ــــــــــــــــــــــــــــــــــــ</u>

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

Standar	Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic	Тур.	Units	Conditions				
TH01	θJA	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package				
			80	°C/W	28-pin SO/C package				
			90	°C/W	28-pin SSOP package				
			48	°C/W	28-pin UQFN 4x4mm package				
			47.2	°C/W	40-pin PDIP package				
			41.0	°C/W	40-pin UQFN 5x5 package				
			46.0	°C/W	44-pin TQFP package				
			24.4	°C/W\	44-pin QFN 8X8mm package				
			27.6	∘C/W ∖	48-pin VQFN 6x6 package				
			—	∕~c/w	48-pin TQFP 7x7 package				
TH02	θJC	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package				
			24	°CAV \	28-pin SOIC package				
			24 -	°C/W	28-pin SSOP package				
			<u> </u>	°C/W	28-pin UQFN 4x4mm package				
			24.70	°C/₩	40-pin PDIP package				
			5,5	_ °℃⁄W	40-pin UQFN 5x5 package				
			14.5	>°C/W	44-pin TQFP package				
		\sim	20.0	°C/W	44-pin QFN 8X8mm package				
			6.7	°C/W	48-pin UQFN 6x6 package				
			\rightarrow	°C/W	48-pin TQFP 7x7 package				
TH03	TJMAX	Maximum Junction Temperature	[∼] 150	°C					
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O				
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD ⁽¹⁾				
TH06	Pi/o	I/O Power Dissipation	—	W	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$				
TH07	Pder	Derated Rower	—	W	Pder = PDmax (Τj - Τa)/θja ⁽²⁾				

TABLE 37-6: THERMAL CHARACTERISTICS

Note 1: IDD is current to run the chip alone without driving any load on the output pins.
2: TA = Ambient Temperature, TJ = Sunction Temperature

PIC16(L)F15356/75/76/85/86



TABLE 37-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)											
Param. No.	Sym.	Characteristic	Min.	Typt	Max.	Units	Conditions				
ECL Osc	illator			$\overline{\ }$	\searrow						
OS1	F _{ECL}	Clock Frequency		\sum	> 500	kHz					
OS2	T _{ECL_DC}	Clock Duty Cycle	40	<u> </u>	60	%					
ECM Oscillator											
OS3	F _{ECM}	Clock Frequency	\mathcal{X}	$\rangle -$	4	MHz					
OS4	T _{ECM_DC}	Clock Duty Cycle	40	—	60	%					
ECH Oscillator											
OS5	F _{ECH}	Clock Frequency	> -	—	32	MHz					
OS6	T _{ECH_DC}	Clock Duty Sycle	40	—	60	%					
LP Oscillator											
OS7	F _{LP}	Clock Frequency		_	100	kHz	Note 4				
XT Oscillator											
OS8	F _{XT}			_	4	MHz	Note 4				
HS Oscillator											
OS9	F _{HS})	Clock Frequency		—	20	MHz	Note 4				
System Oscillator											
0S20	Fose	System Clock Frequency	—	—	32	MHz	(Note 2, Note 3)				
ØS21	FCY	Instruction Frequency	_	Fosc/4	—	MHz					
0\$22	/т _{сү}	Instruction Period	125	1/F _{CY}	_	ns					

These parameters are characterized but not tested.

Pata in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: The system clock frequency (Fosc) is selected by the "main clock switch controls" as described in Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)".

- 3: The system clock frequency (Fosc) must meet the voltage requirements defined in the Section 37.2 "Standard Operating Conditions".
- 4: LP, XT and HS oscillator modes require an appropriate crystal or resonator to be connected to the device. For clocking the device with the external square wave, one of the EC mode selections must be used.

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensior	n Limits	MIN	NOM	MAX	
Contact Pitch	E		0.40 BSC		
Optional Center Pad Width	W2			3.80	
Optional Center Pad Length	T2			3.80	
Contact Pad Spacing	C1		5.00		
Contact Pad Spacing	C2		5.00		
Contact Pad Width (X40)	X1			0.20	
Contact Pad Length (X40)	Y1			0.75	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B

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