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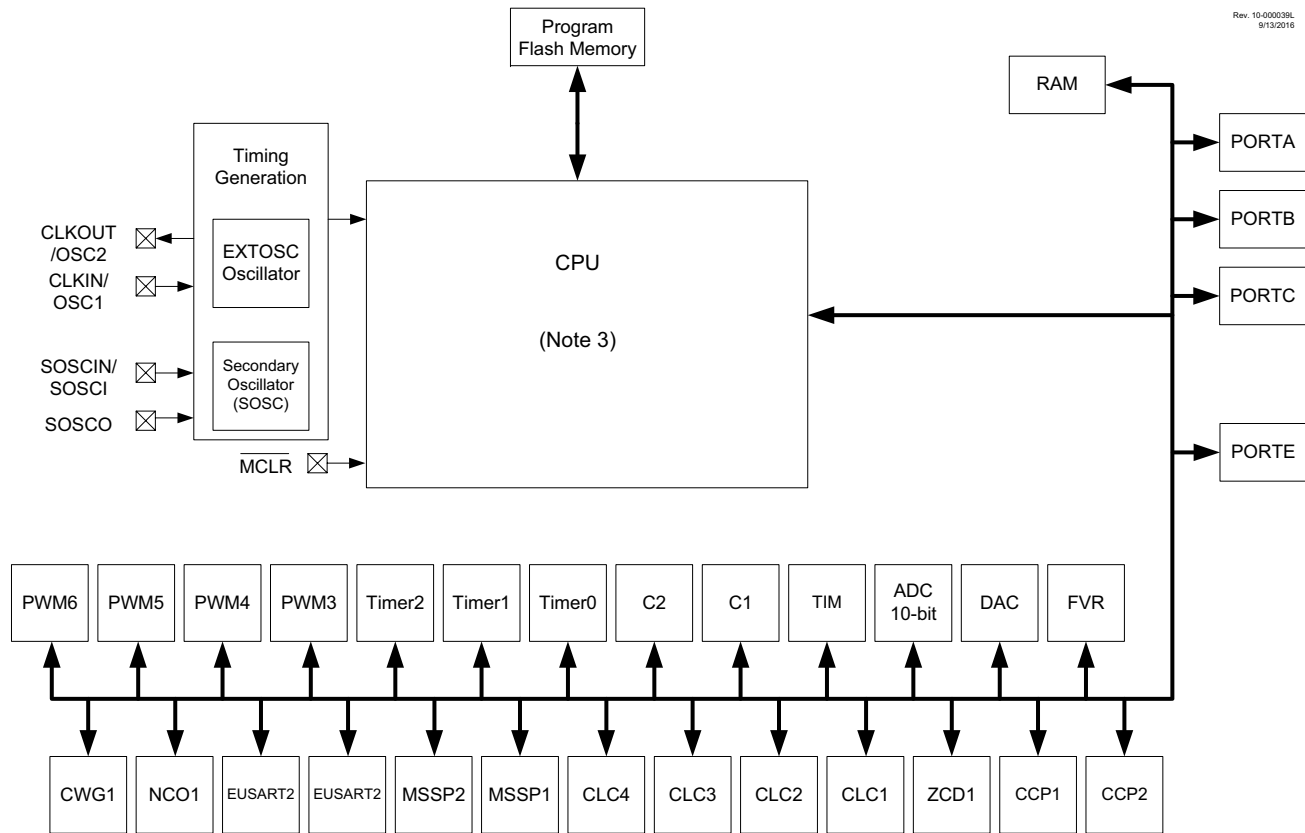
### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15376-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15376-i-pt</a>

**FIGURE 1-1: PIC16(L)F15356 BLOCK DIAGRAM**

**Note 1:** See applicable chapters for more information on peripherals.

**2:** See Table 1-1 for peripherals available on specific devices.

**3:** See Figure 3-1.

# PIC16(L)F15356/75/76/85/86

**TABLE 1-2: PIC16(L)F15356 PINOUT DESCRIPTION**

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0-/C2IN0-/CLCIN0 <sup>(1)</sup> /IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	CLCIN0 <sup>(1)</sup>	TTL/ST	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/C1IN1-/C2IN1-/CLCIN1 <sup>(1)</sup> /IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	CLCIN1 <sup>(1)</sup>	TTL/ST	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/C1IN0+/C2IN0+/DAC1OUT1/IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	C1IN0+	AN	—	Comparator 2 positive input.
	C2IN0+	AN	—	Comparator 2 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
RA3/ANA3/C1IN1+/VREF+/IOCA3/DAC1REF+	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN	—	ADC Channel A3 input.
	C1IN1+	AN	—	Comparator 1 positive input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
RA4/ANA4/T0CKI <sup>(1)</sup> /IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T0CKI <sup>(1)</sup>	TTL/ST	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
RA5/ANA5/SS1 <sup>(1)</sup> /IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	SS1 <sup>(1)</sup>	TTL/ST	—	MSSP1 SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.

**Legend:** AN = Analog input or output      CMOS = CMOS compatible input or output      OD = Open-Drain  
TTL = TTL compatible input      ST = Schmitt Trigger input with CMOS levels      I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage      XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

# PIC16(L)F15356/75/76/85/86

**TABLE 1-2: PIC16(L)F15356 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
OUT <sup>(2)</sup>	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	SDO2	—	CMOS/OD	MSSP2 SPI serial data output.
	SCK2	—	CMOS/OD	MSSP2 SPI serial clock output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1 <sup>(3)</sup>	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	TX2	—	CMOS/OD	EUSART2 Asynchronous mode transmitter data output.
	CK2 <sup>(3)</sup>	—	CMOS/OD	EUSART2 Synchronous mode clock output.
	DT <sup>(3)</sup>	—	CMOS/OD	EUSART Synchronous mode data output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP2 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
	NCO1OUT	—	CMOS/OD	Numerically Controller Oscillator output.
	CLKR	—	CMOS/OD	Clock Reference module output.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open-Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage    XTAL = Crystal levels

- Note** 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.
- 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
- 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
- 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLV register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

## 4.1.1 READING PROGRAM MEMORY AS DATA

There are three methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory. The third method is to use the NVMREG interface to access the program memory. For an example of NVMREG interface use, reference Section 13.3, NVMREG Access.

### 4.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 4-1.

#### EXAMPLE 4-1: RETLW INSTRUCTION

```
constants
    BRW                ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0        ;Index0 data
    RETLW DATA1        ;Index1 data
    RETLW DATA2
    RETLW DATA3

my_function
    ;... LOTS OF CODE...
    MOVLW DATA_INDEX
    call constants
    ;... THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement.

### 4.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of an FSRxH register and reading the matching INDFx register. The MOVLW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that read the program memory via the FSR require one extra instruction cycle to complete. Example 4-2 demonstrates reading the program memory via an FSR.

**TABLE 4-7: PIC16(L)F15356/75/76/85/86 MEMORY MAP, BANK 24-31**

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 4-3)	C80h	Core Registers (Table 4-3)	D00h	Core Registers (Table 4-3)	D80h	Core Registers (Table 4-3)	E00h	Core Registers (Table 4-3)	E80h	Core Registers (Table 4-3)	F00h	Core Registers (Table 4-3)	F80h	Core Registers (Table 4-3)
C0Bh C0Ch	Unimplemented Read as '0'	C8Bh C8Ch	Unimplemented Read as '0'	D0Bh D0Ch	Unimplemented Read as '0'	D8Bh	Unimplemented Read as '0'	E0Bh	Unimplemented Read as '0'	E8Bh	Unimplemented Read as '0'	F0Bh	Unimplemented Read as '0'	F8Bh	Unimplemented Read as '0'
C1Fh C20h		C9Fh CA0h													
C6Fh C70h	General Purpose Register 80 Bytes <sup>(1)</sup>	C9Fh CA0h	General Purpose Register 80 Bytes <sup>(1)</sup>	D6Fh D70h	Accesses 70h – 7Fh	DEFh DF0h	Accesses 70h – 7Fh	E6Fh E70h	Accesses 70h – 7Fh	EEFh EF0h	Accesses 70h – 7Fh	F6Fh F70h	Accesses 70h – 7Fh	FEFh FF0h	Accesses 70h – 7Fh
CFFh	Accesses 70h – 7Fh	CEFh CF0h	Accesses 70h – 7Fh	D7Fh		DEFh DF0h		E7Fh		EEFh		F7Fh		FEFh FF0h	
		CFFh				DEFh DF0h				EEFh				FEFh FF0h	

**Legend:**  = Unimplemented data memory locations, read as '0'.

**Note 1:** Present only in PIC16(L)F15356/76/86.

**TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 12											
CPU CORE REGISTERS; see Table 4-3 for specifics											
60Ch	CWG1CLKCON	—	—	—	—	—	—	—	CS	---- ---0	---- ---0
60Dh	CWG1DAT	—	—	—	—	DAT<3:0>				---- 0000	---- 0000
60Eh	CWG1DBR	—	—	DBR<5:0>						--00 0000	--00 0000
60Fh	CWG1DBF	—	—	DBF<5:0>						--00 0000	--00 0000
610h	CWG1CON0	EN	LD	—	—	—	MODE<2:0>			00-- -000	00-- -000
611h	CWG1CON1	—	—	IN	—	POLD	POLC	POLB	POLA	--x- 0000	--u- 0000
612h	CWG1AS0	SHUTDOWN	REN	LSBD<2:0>		LSAC<2:0>		—	—	0001 01--	0001 01--
613h	CWG1AS1	—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	---0 0000	---u 0000
614h	CWG1STR	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000
615h 61Fh	—	Unimplemented								—	—

**Legend:** x = unknown, u = unchanged, c = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

## 4.6.2 LINEAR DATA MEMORY

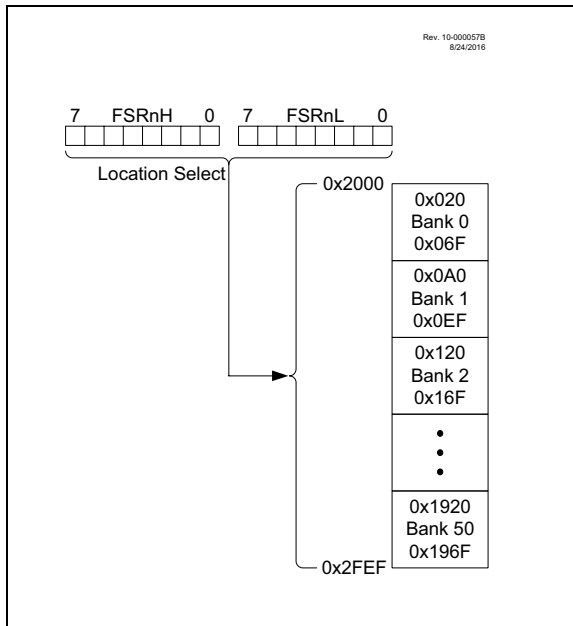
The linear data memory is the region from FSR address 0x2000 to FSR address 0x2FEF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks. Refer to Figure 4-12 for the Linear Data Memory Map.

**Note:** The address range 0x2000 to 0x2FF0 represents the complete addressable Linear Data Memory up to Bank 50. The actual implemented Linear Data Memory will differ from one device to the other in a family. Confirm the memory limits on every device.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

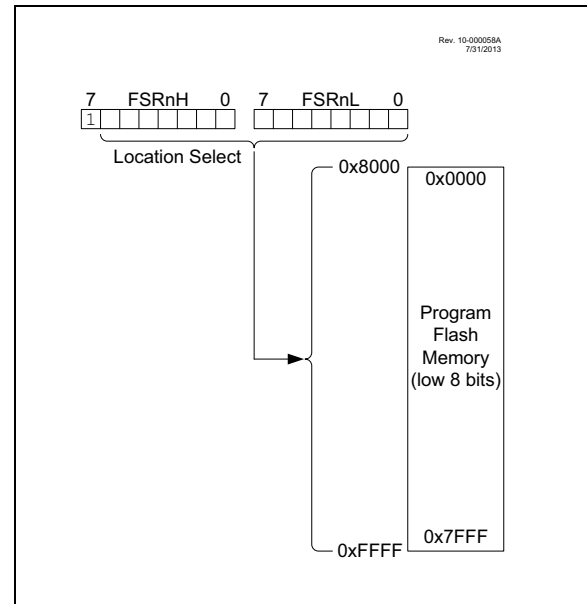
**FIGURE 4-12: LINEAR DATA MEMORY MAP**



## 4.6.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire Program Flash Memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower eight bits of each memory location is accessible via INDF. Writing to the Program Flash Memory cannot be accomplished via the FSR/INDF interface. All instructions that access Program Flash Memory via the FSR/INDF interface will require one additional instruction cycle to complete.

**FIGURE 4-13: PROGRAM FLASH MEMORY MAP**





# PIC16(L)F15356/75/76/85/86

## REGISTER 10-17: PIR7: PERIPHERAL INTERRUPT REQUEST REGISTER 7

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	R/W/HS-0/0
—	—	NVMIF	NCO1IF	—	—	—	CWG1IF
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

- bit 7-6      **Unimplemented:** Read as '0'
- bit 5      **NVMIF:** Nonvolatile Memory (NVM) Interrupt Flag bit  
1 = The requested NVM operation has completed  
0 = NVM interrupt not asserted
- bit 4      **NCO1IF:** Numerically Controlled Oscillator (NCO) Interrupt Flag bit  
1 = The NCO has rolled over  
0 = No NCO interrupt event has occurred
- bit 3-1      **Unimplemented:** Read as '0'
- bit 0      **CWG1IF:** CWG1 Interrupt Flag bit  
1 = CWG1 has gone into shutdown  
0 = CWG1 is operating normally, or interrupt cleared

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

## 12.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a `CLRWDT` instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that `CLRWDT` instructions are only accepted when they are performed within a specific window during the time-out period.

The WDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Configurable window size from 12.5 to 100 percent of the time-out period
- Multiple Reset conditions
- Operation during Sleep

## 14.9 Register Definitions: PORTD

### REGISTER 14-25: PORTD: PORTD REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
 '1' = Bit is set                          '0' = Bit is cleared

bit 7-0                  **RD<7:0>**: PORTD General Purpose I/O Pin bits<sup>(1)</sup>  
                             1 = Port pin is  $\geq V_{IH}$   
                             0 = Port pin is  $\leq V_{IL}$

**Note 1:** Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

### REGISTER 14-26: TRISD: PORTD TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
 '1' = Bit is set                          '0' = Bit is cleared

bit 7-0                  **TRISD<7:0>**: PORTD Tri-State Control bits  
                             1 = PORTD pin configured as an input (tri-stated)  
                             0 = PORTD pin configured as an output

### REGISTER 14-27: LATD: PORTD DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
 '1' = Bit is set                          '0' = Bit is cleared

bit 7-0                  **LATD<7:0>**: PORTD Output Latch Value bits<sup>(1)</sup>

**Note 1:** Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

## 14.12 PORTF Registers

**Note:** Present only on PIC16(L)F15385/86.

### 14.12.1 DATA REGISTER

PORTF is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISF (Register 14-42). Setting a TRISF bit (= 1) will make the corresponding PORTF pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISF bit (= 0) will make the corresponding PORTF pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Figure 14-1 shows how to initialize an I/O port.

Reading the PORTF register (Register 14-41) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATF).

The PORT data latch LATF (Register 14-43) holds the output port data, and contains the latest value of a LATF or PORTF write.

### 14.12.2 DIRECTION CONTROL

The TRISF register (Register 14-42) controls the PORTF pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISF register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

### 14.12.3 INPUT THRESHOLD CONTROL

The INLVLF register (Register 14-48) controls the input voltage threshold for each of the available PORTF input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTF register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 37-4 for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

### 14.12.4 OPEN-DRAIN CONTROL

The ODCONF register (Register 14-46) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONF bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONF bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

**Note:** It is not necessary to set open-drain control when using the pin for I<sup>2</sup>C; the I<sup>2</sup>C module controls the pin and makes the pin open-drain.

### 14.12.5 SLEW RATE CONTROL

The SLRCONF register (Register 14-47) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONF bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONF bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

### 14.12.6 ANALOG CONTROL

The ANSELF register (Register 14-44) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELF bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELF bits has no effect on digital output functions. A pin with TRIS clear and ANSELF set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

**Note:** The ANSELF bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

### 14.12.7 WEAK PULL-UP CONTROL

The WPUF register (Register 14-45) controls the individual weak pull-ups for each port pin.

### 14.12.8 PORTF FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

## 15.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I<sup>2</sup>C)

**Note:** The I<sup>2</sup>C SCLx and SDAx functions can be remapped through PPS. However, only the RB1, RB2, RC3 and RC4 pins have the I<sup>2</sup>C and SMBus specific input buffers implemented (I<sup>2</sup>C mode disables INLVL and sets thresholds that are specific for I<sup>2</sup>C). If the SCLx or SDAx functions are mapped to some other pin (other than RB1, RB2, RC3 or RC4), the general purpose TTL or ST input buffers (as configured based on INLVL register setting) will be used instead. In most applications, it is therefore recommended only to map the SCLx and SDAx pin functions to the RB1, RB2, RC3 or RC4 pins.

## 15.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 15-1.

### EXAMPLE 15-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    BCF    INTCON,GIE
; BANKSEL PPSLOCK    ; set bank
; required sequence, next 5 instructions
    MOVLW  0x55
    MOVWF  PPSLOCK
    MOVLW  0xAA
    MOVWF  PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    BSF    PPSLOCK,PPSLOCKED
; restore interrupts
    BSF    INTCON,GIE
```

## 15.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

## 15.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

## 15.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values (Permanent Lock Removed). All other Resets leave the selections unchanged. Default input selections are shown in Table 15-1 through Table 15-3.

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**REGISTER 16-2: PMD1: PMD CONTROL REGISTER 1**

R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
NCO1MD	—	—	—	—	TMR2MD	TMR1MD	TMR0MD
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	<b>NCO1MD:</b> Disable Numerically Control Oscillator bit 1 = NCO1 module disabled 0 = NCO1 module enabled
bit 6-3	<b>Unimplemented:</b> Read as '0'
bit 2	<b>TMR2MD:</b> Disable Timer TMR2 bit 1 = Timer2 module disabled 0 = Timer2 module enabled
bit 1	<b>TMR1MD:</b> Disable Timer TMR1 bit 1 = Timer1 module disabled 0 = Timer1 module enabled
bit 0	<b>TMR0MD:</b> Disable Timer TMR0 bit 1 = Timer0 module disabled 0 = Timer0 module enabled

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**TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		264
ADCON0	CHS<5:0>						GO/DONE	ADON	277
ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		279
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	287

**Legend:** — = unimplemented locations read as '0'. Shaded cells are not used with the Fixed Voltage Reference.

## 27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

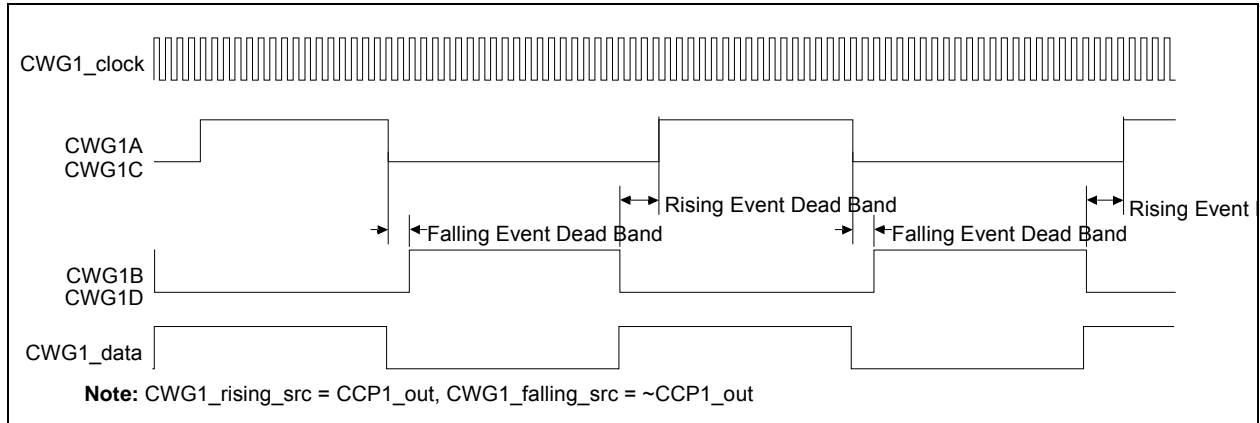
- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.



**FIGURE 30-9: CWG HALF-BRIDGE MODE OPERATION**



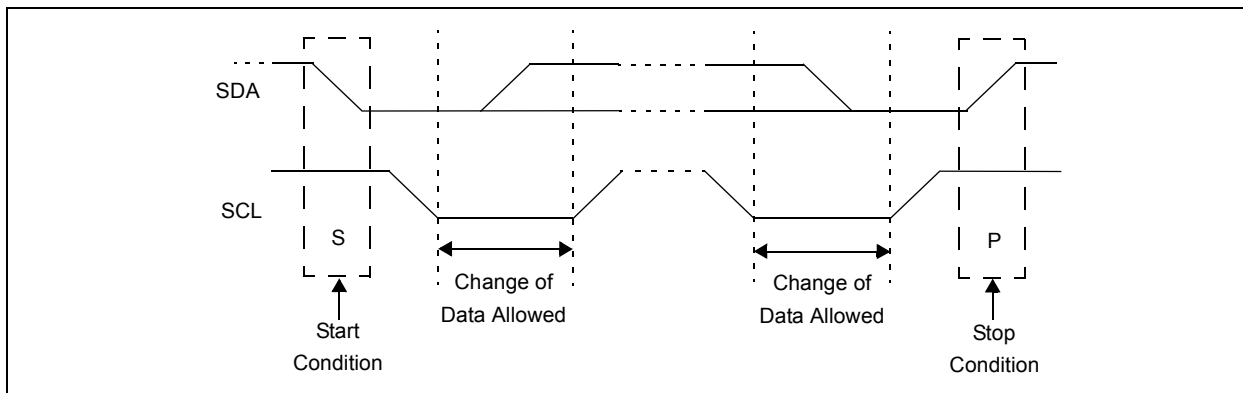
# PIC16(L)F15356/75/76/85/86

**TABLE 31-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx**

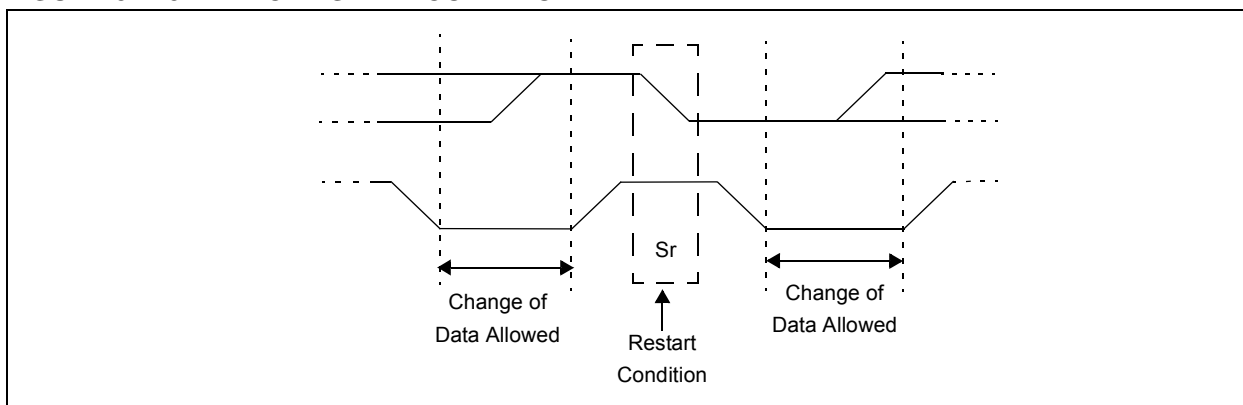
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	146
PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	160
PIE5	CLC4IE	CLC4IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	152
CLC1CON	LC1EN	—	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			410
CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	411
CLC1SEL0	—	—	LC1D1S<5:0>						412
CLC1SEL1	—	—	LC1D2S<5:0>						412
CLC1SEL2	—	—	LC1D3S<5:0>						412
CLC1SEL3	—	—	LC1D4S<5:0>						412
CLC1GLS0	—	—	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	413
CLC1GLS1	—	—	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	414
CLC1GLS2	—	—	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	415
CLC1GLS3	—	—	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	416
CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	LC2MODE<2:0>			410
CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	411
CLC2SEL0	—	—	LC2D1S<5:0>						412
CLC2SEL1	—	—	LC2D2S<5:0>						412
CLC2SEL2	—	—	LC2D3S<5:0>						412
CLC2SEL3	—	—	LC2D4S<5:0>						412
CLC2GLS0	—	—	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	413
CLC2GLS1	—	—	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	414
CLC2GLS2	—	—	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	415
CLC2GLS3	—	—	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	416
CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			410
CLC3POL	LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	411
CLC3SEL0	—	—	LC3D1S<5:0>						412
CLC3SEL1	—	—	LC3D2S<5:0>						412
CLC3SEL2	—	—	LC3D3S<5:0>						412
CLC3SEL3	—	—	LC3D4S<5:0>						412
CLC3GLS0	—	—	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	413
CLC3GLS1	—	—	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	414
CLC3GLS2	—	—	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	415
CLC3GLS3	—	—	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	416
CLC4CON	LC4EN	—	LC4OUT	LC4INTP	LC4INTN	LC4MODE<2:0>			410
CLC4POL	LC4POL	—	—	—	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	411
CLC4SEL0	—	—	LC4D1S<5:0>						412
CLC4SEL1	—	—	LC4D2S<5:0>						412
CLC4SEL2	—	—	LC4D3S<5:0>						412
CLC4SEL3	—	—	LC4D4S<5:0>						412
CLC4GLS0	—	—	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	413

**Legend:** — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

**FIGURE 32-12: I<sup>2</sup>C START AND STOP CONDITIONS**



**FIGURE 32-13: I<sup>2</sup>C RESTART CONDITION**



## 32.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I<sup>2</sup>C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ( $\overline{\text{ACK}}$ ) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

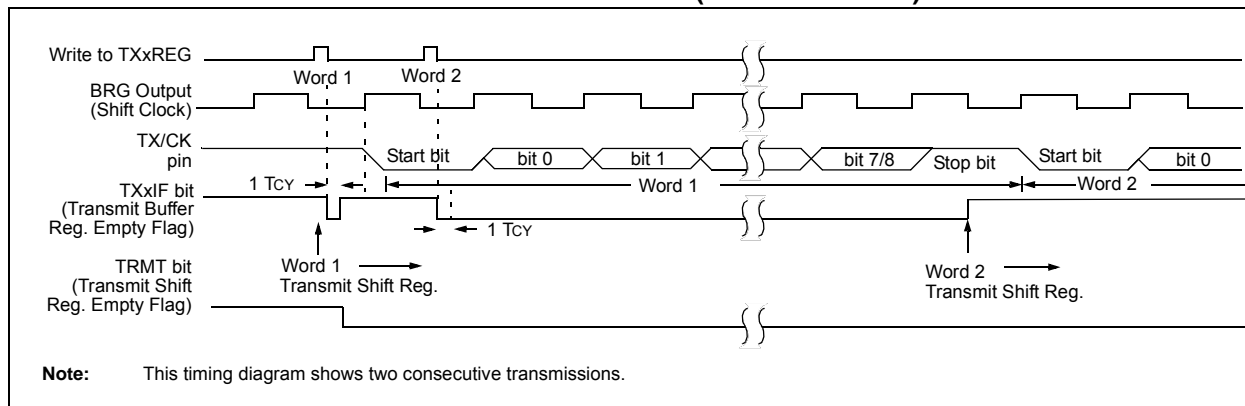
The result of an  $\overline{\text{ACK}}$  is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the  $\overline{\text{ACK}}$  value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

There are certain conditions where an  $\overline{\text{ACK}}$  will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

**FIGURE 33-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)**



## 33.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 33-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCxREG register.

### 33.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCxSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXxSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCxSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

**Note:** If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

### 33.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 33.1.2.4 "Receive Framing Error"** for more information on framing errors.

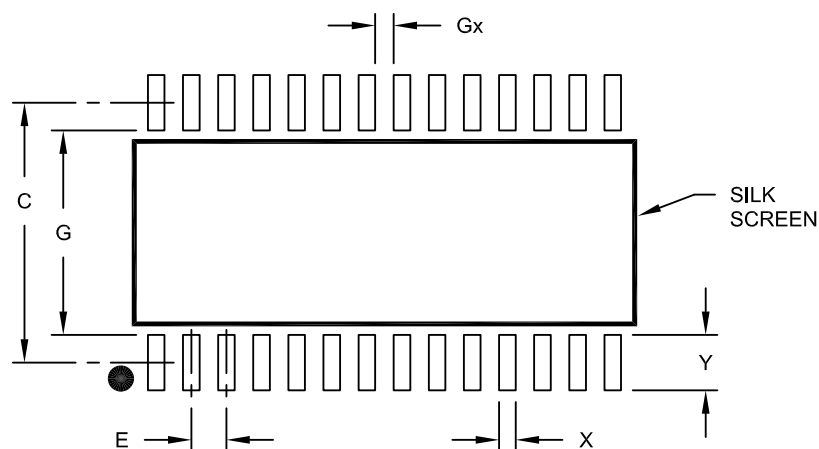
Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RXxIF interrupt flag bit of the PIR3 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCxREG register.

**Note:** If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 33.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

# PIC16(L)F15356/75/76/85/86

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A