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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	44
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 43x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15385-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RC1/ANC1/CCP2 <sup>(1)</sup> /IOCC1/SOSCI	RC1	TTL/ST	CMOS/OD	General purpose I/O.
	ANC1	AN	_	ADC Channel C1 input.
	CCP2 <sup>(1)</sup>	TTL/ST	CMOS/OD	CCP2 Capture Input.
	IOCC1	TTL/ST	_	Interrupt-on-change input.
	SOSCI	AN	_	32.768 kHz secondary oscillator crystal driver input.
RC2/ANC2/CCP1 <sup>(1)</sup> /IOCC2	RC2	TTL/ST	CMOS/OD	General purpose I/O.
	ANC2	AN	_	ADC Channel C2 input.
	CCP1 <sup>(1)</sup>	TTL/ST	CMOS/OD	CCP1 Capture Input.
	IOCC2	TTL/ST	_	Interrupt-on-change input.
RC3/ANC3/SCL1 <sup>(3,4)</sup> /SCK1 <sup>(1)</sup> /T2IN <sup>(1)</sup> /	RC3	TTL/ST	CMOS/OD	General purpose I/O.
10003	ANC3	AN	_	ADC Channel C3 input.
	SCL1 <sup>(3,4)</sup>	l <sup>2</sup> C	OD	MSSP1 I <sup>2</sup> C input/output.
	SCK1 <sup>(1)</sup>	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	T2IN <sup>(1)</sup>	TTL/ST	—	Timer2 external input.
	IOCC3	TTL/ST	_	Interrupt-on-change input.
RC4/ANC4/SDA1 <sup>(3,4)</sup> /SDI1 <sup>(1)</sup> /IOCC4	RC4	TTL/ST	CMOS/OD	General purpose I/O.
	ANC4	AN	_	ADC Channel C4 input.
	SDA1 <sup>(3,4)</sup>	I <sup>2</sup> C	OD	MSSP1 I <sup>2</sup> C serial data input/output.
	SDI1 <sup>(1)</sup>	TTL/ST	_	MSSP1 SPI serial data input.
	IOCC4	TTL/ST	_	Interrupt-on-change input.
RC5/ANC5/IOCC5	RC5	TTL/ST	CMOS/OD	General purpose I/O.
	ANC5	AN	_	ADC Channel C5 input.
	IOCC5	TTL/ST	_	Interrupt-on-change input.
RC6/ANC6/TX1/CK1 <sup>(1)</sup> /IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	_	ADC Channel C6 input.
	TX1	—	CMOS	EUSART1 asynchronous transmit.
	CK1 <sup>(1)</sup>	TTL/ST	CMOS/OD	EUSART 1 synchronous mode clock input/output.
	IOCC6	TTL/ST	_	Interrupt-on-change input.
RC7/ANC7/RX1/DT1 <sup>(3)</sup> /IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	_	ADC Channel C7 input.
	RX1	TTL/ST	_	EUSART1 Asynchronous mode receiver data input.
	DT1 <sup>(3)</sup>	TTL/ST	CMOS/OD	EUSART1 Synchronous mode data input/output.
	IOCC7	TTL/ST	_	Interrupt-on-change input.
Legend: AN = Analog input or outp	ut CMOS :	= CMOS co	mpatible input or o	utput OD = Open-Drain

### **TABLE 1-2:** PIC16(L)F15356 PINOUT DESCRIPTION (CONTINUED)

Note

Schmitt Trigger input of output
 Schmitt Trigger input with CMOS levels
 Crystal levels

 $\begin{aligned} HV &= \text{Airadeg input of output} & \text{Since on the comparison of the comparison o$ 1:

2: options as described in Table 15-3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and

3: PPS output registers.

These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS 4: assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

### TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

						<u> </u>	,				
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR
Bank 62 (C	continued)										
1F2Ah	RD2PPS <sup>(1)</sup>	—	_	_			RD2PPS<4:0	>		00 0000	uu uuuu
1F2Bh	RD3PPS <sup>(1)</sup>	—	—	—				00 0000	uu uuuu		
1F2Ch	RD4PPS <sup>(1)</sup>	—	—	—			RD4PPS<4:0	>		00 0000	uu uuuu
1F2Dh	RD5PPS <sup>(1)</sup>	—	—	—		RD5PPS<4:0>					uu uuuu
1F2Eh	RD6PPS <sup>(1)</sup>	—	_	_			RD6PPS<4:0	>		00 0000	uu uuuu
1F2Fh	RD7PPS <sup>(1)</sup>	—	—	—			RD7PPS<4:0	>		00 0000	uu uuuu
1F30h	RE0PPS	—	—	—			RD5PPS<4:0	>		00 0000	uu uuuu
1F31h	RE1PPS	—	—	—			RD6PPS<4:0	>		00 0000	uu uuuu
1F32h	RE2PPS	—	—	—			RD7PPS<4:0	>		00 0000	uu uuuu
1F33h 	_				Unimpler	mented				_	_

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Legend: x = unknown, u = unchanged, g = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'. Note 1: Present only on PIC16(L)F15375/76/85/86.

### 8.13 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON registers are updated to indicate the cause of the Reset. Table 8-3 and Table 8-4 show the Reset conditions of these registers.

STOVF	STKUNF	RWDT	RMCLR	١٣	POR	BOR	압	18	MEMV	Condition
0	0	1	1	1	0	x	1	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	u	Illegal, TO is set on POR
0	0	1	1	1	0	x	x	0	u	Illegal, PD is set on POR
0	0	u	1	1	u	0	1	1	u	Brown-out Reset
u	u	0	u	u	u	u	0	u	u	WWDT Reset
u	u	u	u	u	u	u	0	0	u	WWDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	u	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	1	MCLR Reset during normal operation
u	u	u	0	u	u	u	1	0	u	MCLR Reset during Sleep
u	u	u	u	0	u	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)
u	u	u	u	u	u	u	u	u	0	Memory violation Reset

### TABLE 8-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

### TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON0 Register	PCON1 Register
Power-on Reset	0000h	1 1000	0011 110x	1-
MCLR Reset during normal operation	0000h	u uuuu	uuuu Ouuu	1-
MCLR Reset during Sleep	0000h	1 Ouuu	uuuu Ouuu	u-
WWDT Timeout Reset	0000h	0 uuuu	uuu0 uuuu	u-
WWDT Wake-up from Sleep	PC + 1	0 Ouuu	uuuu uuuu	u-
WWDT Window Violation	0000h	u uuuu	uu0u uuuu	u-
Brown-out Reset	0000h	1 1000	0011 11u0	u-
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	1 Ouuu	uuuu uuuu	u-
RESET Instruction Executed	0000h	u uuuu	uuuu u0uu	u-
Stack Overflow Reset (STVREN = 1)	0000h	u uuuu	luuu uuuu	u-
Stack Underflow Reset (STVREN = 1)	0000h	u uuuu	uluu uuuu	u-
Memory Violation Reset (MEMV = 0)	0	-uuu uuuu	uuuu uuuu	0-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

# 8.15 Register Definitions: Power Control

### REGISTER 8-2: PCON0: POWER CONTROL REGISTER 0

R/W/HS-0/q	R/W/HS-0/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	WDTWV	RWDT	RMCLR	RI	POR	BOR
bit 7							bit 0

Legend:								
HC = Bit is clea	ared by hardwa	are	HS = Bit is set by hardware					
R = Readable	bit	W = Writable bit	U = Unimplemented bit, read as '0'					
u = Bit is unch	anged	x = Bit is unknown	-m/n = Value at POR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is cleared	q = Value depends on condition					
			,					
bit 7	STKOVF: Sta	ack Overflow Flag bit						
	1 = A Stack (	Overflow occurred	r cleared by firmware					
hit 6		overnow has not occurred o						
DIL O	1 = A  Stack l	Underflow occurred						
	0 = A Stack l	Underflow has not occurred	or cleared by firmware					
bit 5	WDTWV: WD	T Window Violation Flag bit	t					
1 = A WDT Window Violation Reset has not occurred or set to '1' by firmware								
0 = A WD1 Window Violation Reset has occurred (a CLRWDT instruction was executed either witho arming the window or outside the window (cleared by hardware)								
bit 4	RWDT: Watch	hdog Timer Reset Flag bit						
	1 = A Watchd	log Timer Reset has not occ	curred or set to '1' by firmware					
			ed (cleared by hardware)					
DIT 3	1 = A MCLR	LK Reset Flag bit Reset has not occurred or s	et to '1' by firmware					
	0 = A MCLR	Reset has occurred (cleared	d by hardware)					
bit 2	RI: RESET IN	struction Flag bit						
	1 = A RESET	instruction has not been exe	ecuted or set to '1' by firmware					
	0 = A RESET instruction has been executed (cleared by hardware)							
bit 1 POR: Power-on Reset Status bit								
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)								
bit 0	BOR: Brown-	out Reset Status bit						
	1 = No Brown	n-out Reset occurred						
	0 = A Brown-	out Reset occurred (must be	e set in software after a Power-on Reset or Brown-out Reset					
	occurs)							

### 9.2.1.4 4x PLL

The oscillator module contains a PLL that can be used with external clock sources and internal oscillator to provide a system clock source. The input frequency for the PLL must fall within specifications. See the PLL Clock Timing Specifications in Table 37-9.

The PLL may be enabled for use by one of two methods:

- 1. Program the RSTOSC bits in the Configuration Word 1 to enable the EXTOSC with 4x PLL.
- 2. Write the NOSC bits in the OSCCON1 register to enable the EXTOSC with 4x PLL.

### 9.2.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. Refer to **Section 9.3 "Clock Switching"** for more information.

### FIGURE 9-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
  - **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
  - **3:** For oscillator design assistance, reference the following Microchip Application Notes:
    - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC<sup>®</sup> and PIC<sup>®</sup> Devices" (DS00826)
    - AN849, "Basic PIC<sup>®</sup> Oscillator Design" (DS00849)
    - AN943, "Practical PIC<sup>®</sup> Oscillator Analysis and Design" (DS00943)
    - AN949, "Making Your Oscillator Work" (DS00949)
    - TB097, "Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS" (DS91097)
    - AN1288, "Design Practices for Low-Power External Oscillators" (DS01288)

# **10.0 INTERRUPTS**

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- · Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 10-1.

### FIGURE 10-1: INTERRUPT LOGIC



### 11.2.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source, with the exception of the clock switch interrupt, has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the execution of a SLEEP instruction
  - SLEEP instruction will execute as a NOP
  - WDT and WDT prescaler will not be cleared
  - TO bit of the STATUS register will not be set
  - PD bit of the STATUS register will not be cleared

- · If the interrupt occurs during or after the execution of a SLEEP instruction
  - SLEEP instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - TO bit of the STATUS register will be set
  - PD bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a **SLEEP** instruction executed, test the  $\overline{PD}$  bit. If the  $\overline{PD}$  bit is set, the SLEEP instruction was executed as a NOP.



### **FIGURE 11-2:** WAKE-UP FROM SLEEP THROUGH INTERRUPT

### 11.2.3 LOW-POWER SLEEP MODE

The PIC16F15356/75/76/85/86 device contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode.

The PIC16F15356/75/76/85/86 allows the user to optimize the operating current in Sleep, depending on the application requirements.

Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. Depending on the configuration of these bits, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

### 11.2.3.1 Sleep Current vs. Wake-up Time

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking-up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The Normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

### 14.7 Register Definitions: PORTC

### REGISTER 14-17: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7	•					•	bit 0
Legend:							
R = Readable b	it	W = Writable b	oit	U = Unimplem	nented bit, read a	is '0'	
u = Bit is uncha	nged	x = Bit is unkno	own	-n/n = Value a	t POR and BOR	Value at all othe	er Resets
'1' = Bit is set		'0' = Bit is clea	red				

bit 7-0 RC<7:0>: PORTC General Purpose I/O Pin bits<sup>(1)</sup> 1 = Port pin is  $\geq$  VIH 0 = Port pin is  $\leq$  VIL

### REGISTER 14-18: TRISC: PORTC TRI-STATE REGISTER

| R/W-1/1 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TRISC7  | TRISC6  | TRISC5  | TRISC4  | TRISC3  | TRISC2  | TRISC1  | TRISC0  |
| bit 7   |         |         |         |         |         |         | bit 0   |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

TRISC<7:0>: PORTC Tri-State Control bits

1 = PORTC pin configured as an input (tri-stated)

0 = PORTC pin configured as an output

### REGISTER 14-19: LATC: PORTC DATA LATCH REGISTER

| R/W-x/u |
|---------|---------|---------|---------|---------|---------|---------|---------|
| LATC7   | LATC6   | LATC5   | LATC4   | LATC3   | LATC2   | LATC1   | LATC0   |
| bit 7   |         |         |         |         |         |         | bit 0   |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 LATC<7:0>: PORTC Output Latch Value bits<sup>(1)</sup>

**Note 1:** Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register returns actual I/O pin values.

**Note 1:** Writes to PORTC are actually written to corresponding LATC register. The actual I/O pin values are read from the PORTC register.

### 14.10 PORTE Registers

### 14.10.1 DATA REGISTER

PORTE is a 4-bit wide port. The corresponding data direction register is TRISE (Register 14-33). Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., disable the output driver). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Figure 14-1 shows how to initialize PORTE.

Reading the PORTE register (Register 14-33) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATE).

### 14.10.2 DIRECTION CONTROL

The TRISE register (Register 14-34) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note:	The TRISE3 bit is a read-only bit and it
	always reads a '1'.

### 14.10.3 OPEN-DRAIN CONTROL

The ODCONE register (Register 14-38) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONE bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONE bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note:	It is not necessary to set open-drain control when using the pin for I <sup>2</sup> C; the I <sup>2</sup> C
	module controls the pin and makes the pin open-drain.

### 14.10.4 SLEW RATE CONTROL

The SLRCONE register (Register 14-39) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONE bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONE bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

### 14.10.5 INPUT THRESHOLD CONTROL

The INLVLE register (Register 14-40) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 37-4 for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

### 14.10.6 ANALOG CONTROL

The ANSELE register (Register 14-36) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELE bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELE bits has no effect on digital output functions. A pin with TRIS clear and ANSELE set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELE bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

### 14.10.7 WEAK PULL-UP CONTROL

The WPUE register (Register 14-37) controls the individual weak pull-ups for each port pin.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
PSYNC <sup>(1, 2)</sup>	CKPOL <sup>(3)</sup>	CKSYNC <sup>(4, 5)</sup>			MODE<4:0>(6, 7)	)		
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable bit		U = Unimpleme	ented bit, read as	s 'O'		
u = Bit is unch	anged	x = Bit is unknow	vn	-n/n = Value at	POR and BOR/\	/alue at all other	Resets	
'1' = Bit is set		'0' = Bit is cleare	ed					
bit 7	PSYNC: Timer	x Prescaler Synch	nronization Ena	able bit <sup>(1, 2)</sup>				
	1 = TMRx Pre	escaler Output is s	synchronized to	Fosc/4				
	0 = IMRx Pre	escaler Output is r	iot synchronize	ed to Fosc/4				
bit 6	CKPOL: Timer	x Clock Polarity S	election bit <sup>(3)</sup>					
	1 = Falling ed	ge of input clock of	clocks timer/pre	escaler				
5 H F				- 1-::(4, 5)				
DIES		erx Clock Synchro						
	0 = ON regist	er bit is not synchi	ronized to TMR2_0	2 clk input				
bit 4-0	MODE<4:0>: ]	Fimerx Control Mo	de Selection b	its(6, 7)				
	See Table 27-1							
Note 1: S	Sotting this bit one	uros that roading T	MDy will rotur	n a valid valuo				
Note 1. 3	N has this bit is $(1)$							
2: V	2: When this bit is 1, Timerz cannot operate in Sleep mode.							
3: (	<b>5:</b> UKPUL should not be changed while UN = $1$ .							
4: 5	Setting this bit ensures glitch-free operation when the ON is enabled or disabled.							
5: V	When this bit is set	then the timer op	eration will be	delayed by two TI	MRx input clocks	after the ON bit	is set.	
6: l	Jnless otherwise in of TMRx).	s otherwise indicated, all modes start upon ON = 1 and stop upon ON = 0 (stops occur without affecting the value Rx).						

### REGISTER 27-3: T2HLT: TIMERx HARDWARE LIMIT CONTROL REGISTER

7: When TMRx = PRx, the next clock clears TMRx, regardless of the operating mode.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	EN	—	OUT	FMT		MODE	<3:0>		366
CCP2CON	EN	—	OUT	FMT		MODE	<3:0>		366
INTCON	GIE	PEIE	_	—	—	—	-	INTEDG	146
PIE1	OSFIE	CSWIE	_	—	—	_	—	ADIE	148
PIR1	OSFIF	CSWIF		—	—	—	_	ADIF	156
PR2	Timer2 Module Period Register								
TMR2	Holding Register for the 8-bit TMR2 Register								
T2CON	ON		CKPS<2:0>			OUTP	S<3:0>		355
T2CLKCON	—	_	_	— CS<3:0>					
T2RST	_	_	_	— RSEL<3:0>					
T2HLT	PSYNC	CKPOL	CKSYNC			MODE<4:0>			356

### TABLE 27-2: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

\* Page provides register information.

### 30.1.4 STEERING MODES

In Steering modes, the data input can be steered to any or all of the four CWG output pins. In Synchronous Steering mode, changes to steering selection registers take effect on the next rising input.

In Non-Synchronous mode, steering takes effect on the next instruction cycle. Additional details are provided in **Section 30.9 "CWG Steering Mode"**.





### 30.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the CS bit of the CWG1CLKCON register.

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
	—	IN	_	POLD	POLC	POLB	POLA
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BO	R/Value at all c	other Resets
'1' = Bit is set		'0' = Bit is clea	ared	q = Value de	pends on condit	ion	
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5	IN: CWG Inpu	ut Value bit					
bit 4	Unimplemen	ted: Read as '	0'				
bit 3	3 <b>POLD:</b> CWG1D Output Polarity bit						
	1 = Signal output is inverted polarity						
	0 = Signal ou	itput is normal	polarity				
bit 2	POLC: CWG	1C Output Pola	arity bit				
	1 = Signal ou	Itput is inverted	l polarity				
	0 = Signal output is normal polarity						
bit 1	POLB: CWG	1B Output Pola	rity bit				
	1 = Signal ou	utput is inverted	l polarity				
	0 = Signal ou	utput is normal	polarity				
bit 0	POLA: CWG	1A Output Pola	rity bit				
	1 = Signal ou	utput is inverted	l polarity				

### **REGISTER 30-2:** CWG1CON1: CWG1 CONTROL REGISTER 1

0 = Signal output is normal polarity

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# 31.7 Register Definitions: CLC Control

### REGISTER 31-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
LCxEN	—	LCxOUT	LCxINTP	LCxINTN		LCxMODE<2:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	LCxEN: Configurable Logic Cell Enable bit
	<ul> <li>1 = Configurable logic cell is enabled and mixing input signals</li> <li>0 = Configurable logic cell is disabled and has logic zero output</li> </ul>
bit 6	Unimplemented: Read as '0'
bit 5	LCxOUT: Configurable Logic Cell Data Output bit
	Read-only: logic cell output data, after LCPOL; sampled from CLCxOUT
bit 4	LCxINTP: Configurable Logic Cell Positive Edge Going Interrupt Enable bit
	<ul><li>1 = CLCxIF will be set when a rising edge occurs on CLCxOUT</li><li>0 = CLCxIF will not be set</li></ul>
bit 3	LCxINTN: Configurable Logic Cell Negative Edge Going Interrupt Enable bit
	<ul><li>1 = CLCxIF will be set when a falling edge occurs on CLCxOUT</li><li>0 = CLCxIF will not be set</li></ul>
bit 2-0	LCxMODE<2:0>: Configurable Logic Cell Functional Mode bits
	111 = Cell is 1-input transparent latch with S and R
	110 = Cell is J-K flip-flop with R
	101 = Cell is 2-input D flip-flop with R
	100 = Cell is 1-input D flip-flop with S and R
	011 = Cell is S-R latch
	010 = Cell is 4-input AND
	001 = Cell is OR-XOR
	000 = Cell is AND-OR

# 32.5 I<sup>2</sup>C SLAVE MODE OPERATION

The MSSP Slave mode operates in one of four modes selected by the SSPM bits of SSPxCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes with SSPxIF additionally getting set upon detection of a Start, Restart, or Stop condition.

### 32.5.1 SLAVE MODE ADDRESSES

The SSPxADD register (Register 32-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPxBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 32-5) affects the address matching process. See **Section 32.5.9** "**SSP Mask Register**" for more information.

32.5.1.1 I<sup>2</sup>C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

32.5.1.2 I<sup>2</sup>C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSb's of the 10-bit address and stored in bits 2 and 1 of the SSPxADD register.

After the acknowledge of the high byte the UA bit is set and SCL is held low until the user updates SSPxADD with the low address. The low address byte is clocked in and all eight bits are compared to the low address value in SSPxADD. Even if there is not an address match; SSPxIF and UA are set, and SCL is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

### 32.5.2 SLAVE RECEPTION

When the  $R/\overline{W}$  bit of a matching received address byte is clear, the  $R/\overline{W}$  bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 32-4.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register.

32.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an  $I^2C$  slave in 7-bit Addressing mode. Figure 32-14 and Figure 32-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish  $I^2C$  communication.

- 1. Start bit detected.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Matching address with  $R/\overline{W}$  bit clear is received.
- 4. The slave pulls SDA low sending an ACK to the master, and sets SSPxIF bit.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDA low sending an ACK to the master, and sets SSPxIF bit.
- 10. Software clears SSPxIF.
- 11. Software reads the received byte from SSPxBUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the master.
- 13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.



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### 32.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the  $I^2C$  bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the  $I^2C$  protocol, defined as address  $0 \ge 0.00$ . When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 32-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the eighth falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.





32.5.9 SSP MASK REGISTER

An SSP Mask (SSPxMSK) register (Register 32-5) is available in I<sup>2</sup>C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care". This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

# TABLE 37-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard	Operating	Conditions (unless otherwise stated)					$\sim$
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
RST01*	TMCLR	MCLR Pulse Width Low to ensure Reset	2	_	—	μS	
RST02*	Tioz	I/O high-impedance from Reset detection	_	_	2	μs	
RST03	TWDT	Watchdog Timer Time-out Period	—	16	—	ms	16 ms Wominal-Reset Time
RST04*	TPWRT	Power-up Timer Period	_	65	_	ms	
RST05	Tost	Oscillator Start-up Timer Period <sup>(1,2)</sup>	_	1024	—	/TOSC	$\left \right\rangle$
RST06	VBOR	Brown-out Reset Voltage <sup>(4)</sup>	2.55	2.70	2.85	<u>7</u> 7	BORV = 0
			2.30	2.45	2.60		BORV = ∕I (F devices)
			1.80	1.90	2.05	∖v∨	BORV = 1 (LF devices)
RST07	VBORHYS	Brown-out Reset Hysteresis	_	40 🧹	$\overline{)}$	m∖V ′	
RST08	TBORDC	Brown-out Reset Response Time	_	3	$\langle - \rangle$	μs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	1.8	/ 1.9	2.2	V V	LF Devices Only

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## TABLE 37-12: ANALOG-TO-DIGITAL CONVERTER (ADC) ACCURACY SPECIFICATIONS<sup>(1,2)</sup>:

Standard Operating Conditions (unless otherwise stated)       VDD = 3.0V, TA = 25°C							
Param. No.	Sym.	Characteristic	Min.	Typt	Max.	Units	Conditions
AD01	NR	Resolution	$\sim$	I	10	bit	
AD02	EIL	Integral Error	$\geq$ –	±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD03	Edl	Differential Epror		±0.1	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD04	EOFF	Offset Error		0.5	2.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD05	Egn	Gain Error 🗸 🖊 📈		±0.2	±1.0	LSb	ADCREF+ = 3.0V, ADCREF-= 0V
AD06	VADREF	ADC Reference Voltage (ADREF+ - ADREF-)	1.8	—	Vdd	V	
AD07	VAIN	Full-Scale Range	ADREF-	_	ADREF+	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source		10		kΩ	
AD09	RVREF	ADC Voltage Reference Ladder		50	_	kΩ	Note 3

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.

2: The ABC conversion result never decreases with an increase in the input and has no missing codes.

3: This is the impedance seen by the VREF pads when the external reference pads are selected.

<sup>Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.
2: To ensure these voltage tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible.</sup> 0.1 μF and 0.01 μF values in parallel are recommended.

## 40.1 Package Marking Information (Continued)



Legend:	: XXX	Customer-specific information						
	Y	Year code (last digit of calendar year)						
	ΥY	Year code (last 2 digits of calendar year)						
	WW	Week code (week of January 1 is week '01')						
	NNN	N Alphanumeric traceability code						
		Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)						
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3))						
		can be found on the outer packaging for this package.						
Note:	In the event the full Microchip part number cannot be marked on one line, it will							
	be carried over to the next line, thus limiting the number of available							
	character	s for customer-specific information.						

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