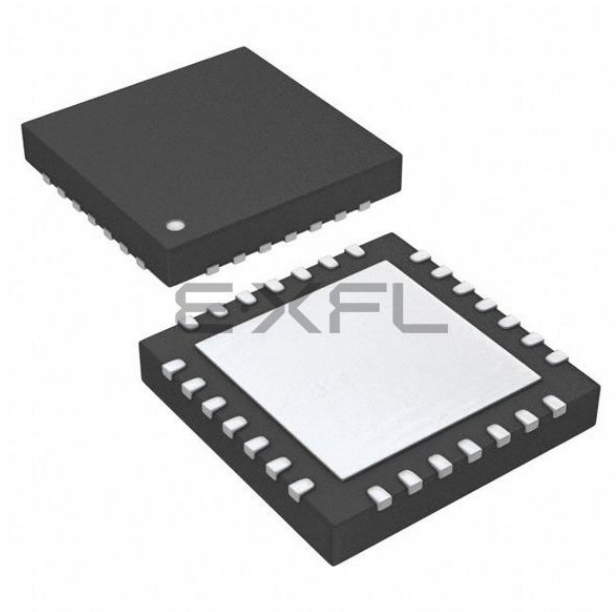

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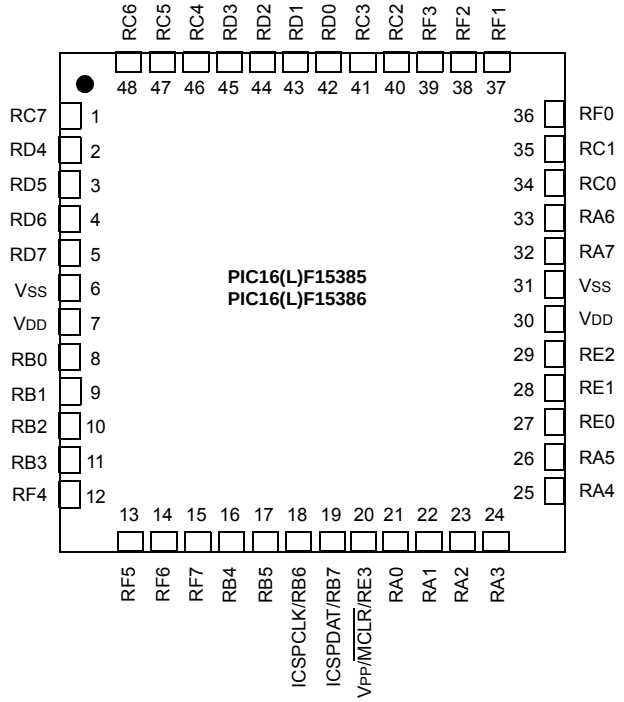
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 44 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 224 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 43x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UFQFN Exposed Pad |
| Supplier Device Package | 28-UQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15385-i-mv |

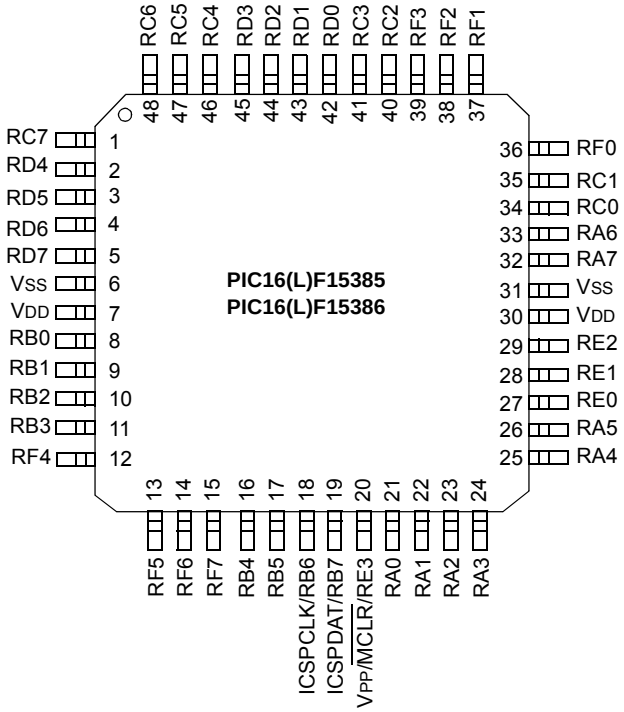
**48-PIN UQFN (6x6)**




**Note 1:** See Table 5 for location of all peripheral functions.

**2:** The bottom pad of the QFN/UQFN package should be connected to Vss as the circuit board level.

**48-PIN TQFP (7x7)**




**Note:** See Table 5 for location of all peripheral functions.

**TABLE 1-3: PIC16(L)F15375/76 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB4/ANB4/ADACT(1)/IOCB4 | RB4 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB4 | AN | — | ADC Channel B4 input. |
| | ADACT(1) | TTL/ST | — | ADC Auto-Conversion Trigger input. |
| | IOCB4 | TTL/ST | — | Interrupt-on-change input. |
| RB5/ANB5/IOCB5 | RB5 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB5 | AN | — | ADC Channel B5 input. |
| | IOCB5 | TTL/ST | — | Interrupt-on-change input. |
| RB6/ANB6/CLCIN2(1)/TX2/CK2(1)/ IOCB6/ICSPCLK | RB6 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB6 | AN | — | ADC Channel B6 input. |
| | CLCIN2(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | TX2 | TTL/ST | — | EUSART2 Asynchronous mode receiver data input. |
| | CK2(1) | TTL/ST | CMOS/OD | EUSART2 Synchronous mode clock input/output. |
| | IOCB6 | TTL/ST | — | Interrupt-on-change input. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming™ and debugging clock input. |
| RB7/ANB7/DAC1OUT2/CLCIN3(1)/ RX2/DT2(1)/IOCB7/ICSPDAT | RB7 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANB7 | AN | — | ADC Channel B7 input. |
| | DAC1OUT2 | — | AN | Digital-to-Analog Converter output. |
| | CLCIN3(1) | TTL/ST | — | Configurable Logic Cell source input. |
| | RX2 | TTL/ST | — | EUSART2 Asynchronous mode receiver data input. |
| | DT2 | TTL/ST | CMOS/OD | EUSART2 Synchronous mode data input/output. |
| | IOCB7 | TTL/ST | — | Interrupt-on-change input. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming™ and debugging data input/output. |
| RC0/ANC0/T1CKI(1)/IOCC0/SOSCO | RC0 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC0 | AN | — | ADC Channel C0 input. |
| | T1CKI(1) | TTL/ST | — | Timer1 external digital clock input. |
| | IOCC0 | TTL/ST | — | Interrupt-on-change input. |
| | SOSCO | — | AN | 32.768 kHz secondary oscillator crystal driver output. |
| RC1/ANC1/CCP2(1)/IOCC1/SOSCI | RC1 | TTL/ST | CMOS/OD | General purpose I/O. |
| | ANC1 | AN | — | ADC Channel C1 input. |
| | CCP2(1) | TTL/ST | CMOS/OD | Capture/compare/PWM2 (default input location for capture function). |
| | IOCC1 | TTL/ST | — | Interrupt-on-change input. |
| | SOSCI | AN | — | 32.768 kHz secondary oscillator crystal driver input. |

**Legend:** AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$
HV = High Voltage; XTAL = Crystal levels

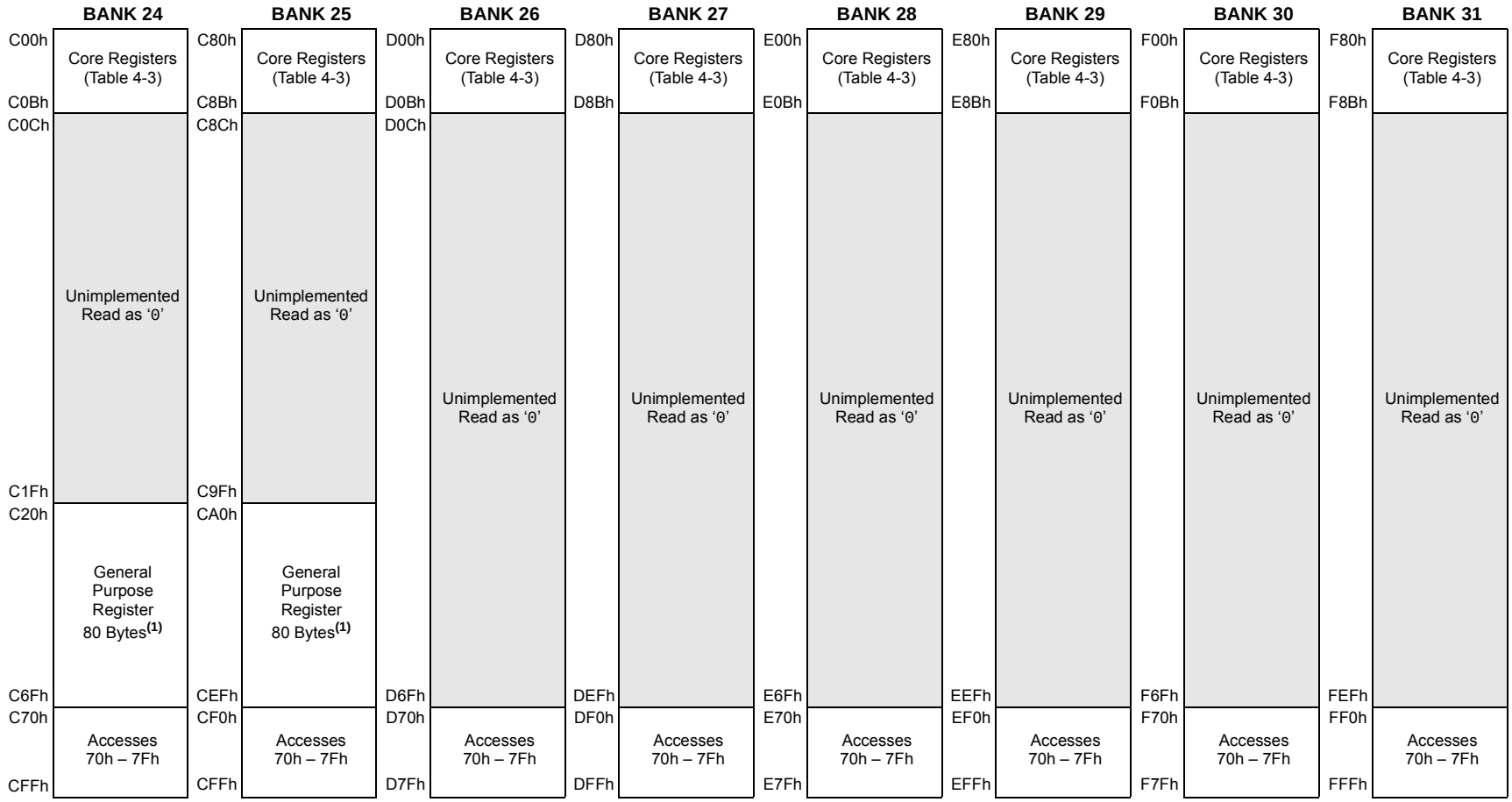
**Note 1:** This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-4 for details on which PORT pins may be used for this signal.

**2:** All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-5, Table 15-6 and Table 15-6.

**3:** This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

**4:** These pins are configured for $I^2C$ logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the $I^2C$ specific or SMBus input buffer thresholds.

**TABLE 4-7: PIC16(L)F15356/75/76/85/86 MEMORY MAP, BANK 24-31**




**Legend:** = Unimplemented data memory locations, read as '0'.

**Note 1:** Present only in PIC16(L)F15356/76/86.

**TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on: MCLR |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 2** | | | | | | | | | | | |
| CPU CORE REGISTERS; see Table 4-3 for specifics | | | | | | | | | | | |
| 10Ch — 118h | — | Unimplemented | | | | | | | | — | — |
| 119h | RC1REG | EUSART Receive Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| 11Ah | TX1REG | EUSART Transmit Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| 11Bh | SP1BRGL | SP1BRG<7:0> | | | | | | | | 0000 0000 | 0000 0000 |
| 11Ch | SP1BRGH | SP1BRG<15:8> | | | | | | | | 0000 0000 | 0000 0000 |
| 11Dh | RC1STA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 0000 | 0000 0000 |
| 11Eh | TX1STA | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D | 0000 0010 | 0000 0010 |
| 11Fh | BAUD1CON | ABDOVF | RCIDL | — | SCKP | BRG16 | — | WUE | ABDEN | 01-0 0-00 | 01-0 0-00 |

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

**TABLE 4-11: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on: MCLR |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 8-10** | | | | | | | | | | | |
| CPU CORE REGISTERS; see Table 4-3 for specifics | | | | | | | | | | | |
| x0Ch/ x8Ch — x1Fh/ x9Fh | — | Unimplemented | | | | | | | | | |

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

### 8.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

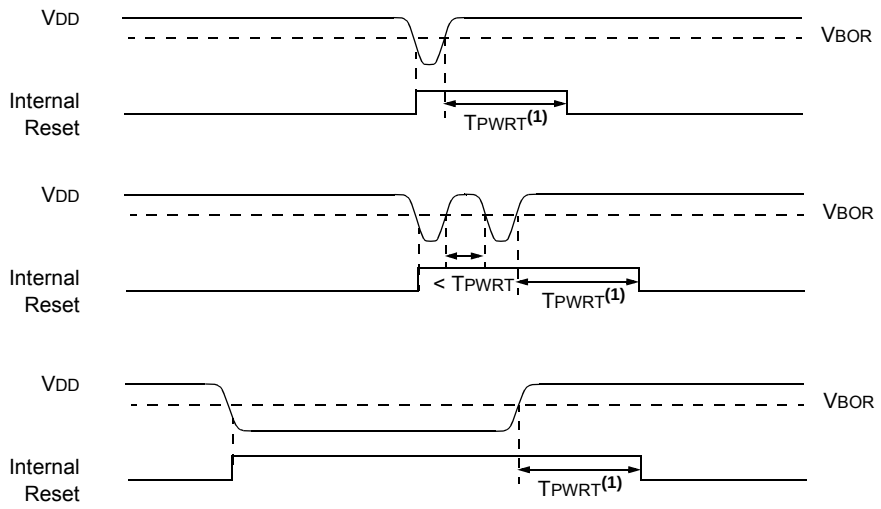
BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

### 8.2.4 BOR IS ALWAYS OFF

When the BOREN bits of the Configuration Words are programmed to '00', the BOR is off at all times. The device start-up is not delayed by the BOR ready condition or the VDD level.

**FIGURE 8-2: BROWN-OUT SITUATIONS**




**Note 1:** TPWRT delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

**TABLE 15-6: PPS OUTPUT SIGNAL ROUTING OPTIONS (PIC16(L)F15375/76)**

| Output Signal Name | RxyPPS Register Value | Remappable to Pins of PORTx | | | | |
|---|---|---|---|---|---|---|
| | | PIC16(L)F15375/76 | | | | |
| | | PORTA | PORTB | PORTC | PORTD | PORTE |
| CLKR | 0x1B | | • | • | | |
| NCO1OUT | 0x1A | • | | | • | |
| TMR0 | 0x19 | | • | • | | |
| SDO2/SDA2 | 0x18 | | • | | • | |
| SCK2/SCL2 | 0x17 | | • | | • | |
| SDO1/SDA1 | 0x16 | | • | • | | |
| SCK1/SCL1 | 0x15 | | • | • | | |
| C2OUT | 0x14 | • | | | | • |
| C1OUT | 0x13 | • | | | • | |
| DT2 | 0x12 | | • | | • | |
| TX2/CK2 | 0x11 | | • | | • | |
| DT1 | 0x10 | | • | • | | |
| TX1/CK1 | 0x0F | | • | • | | |
| PWM6OUT | 0x0E | • | | | • | |
| PWM5OUT | 0x0D | • | | • | | |
| PWM4OUT | 0x0C | | • | | • | |
| PWM3OUT | 0x0B | | • | | • | |
| CCP2 | 0x0A | | • | • | | |
| CCP1 | 0x09 | | • | • | | |
| CWG1D | 0x08 | | • | | • | |
| CWG1C | 0x07 | | • | | • | |
| CWG1B | 0x06 | | • | | • | |
| CWG1A | 0x05 | | • | • | | |
| CLC4OUT | 0x04 | | • | | • | |
| CLC3OUT | 0x03 | | • | | • | |
| CLC2OUT | 0x02 | • | | • | | |
| CLC1OUT | 0x01 | • | | • | | |

**REGISTER 16-6: PMD5 – PMD CONTROL REGISTER 5**

| U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | CLC4MD | CLC3MD | CLC2MD | CLC1MD | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | q = Value depends on condition |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **CLC4MD:** Disable CLC4 bit
1 = CLC4 module disabled
0 = CLC4 module enabled

bit 3 **CLC3MD:** Disable CLC3 bit
1 = CLC3 module disabled
0 = CLC3 module enabled

bit 2 **CLC2MD:** Disable CLC2 bit
1 = CLC2 module disabled
0 = CLC2 module enabled

bit 1 **CLC1MD:** Disable CLC bit
1 = CLC1 module disabled
0 = CLC1 module enabled

bit 0 **Unimplemented**: Read as ‘0’

## 21.6 Register Definitions: DAC Control

**REGISTER 21-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0**

| R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| DAC1EN | — | DAC1OE1 | DAC1OE2 | DAC1PSS<1:0> | | — | DAC1NSS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **DAC1EN:** DAC1 Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **DAC1OE1:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT1 pin
0 = DAC voltage level is disconnected from the DAC1OUT1 pin

bit 4 **DAC1OE2:** DAC1 Voltage Output 1 Enable bit
1 = DAC voltage level is an output on the DAC1OUT2 pin
0 = DAC voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 **DAC1PSS<1:0>:** DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR output
01 = $V_{REF+}$ pin
00 = $V_{DD}$

bit 1 **Unimplemented:** Read as '0'

bit 0 **DAC1NSS:** Read as '0'

**REGISTER 21-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DAC1R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **DAC1R<4:0>:** DAC1 Voltage Output Select bits
$V_{OUT} = (V_{SRC+} - V_{SRC-})*(DAC1R<4:0>/32) + V_{SRC}$

## 23.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Programmable input selection
- Selectable voltage reference
- Programmable output polarity
- Rising/falling output edge interrupts
- CWG1 Auto-shutdown source

### 23.1 Comparator Overview

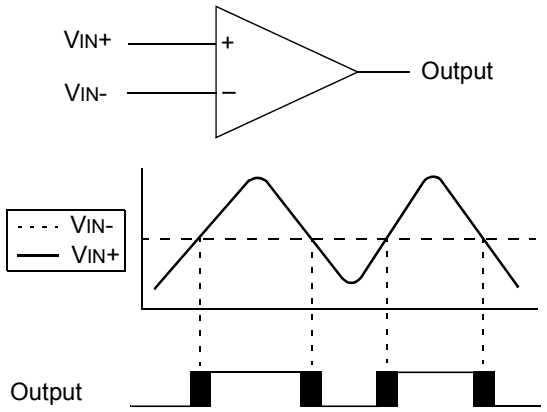
A single comparator is shown in Figure 23-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available are shown in Table 23-1.

**TABLE 23-1: AVAILABLE COMPARATORS**

| Device | C1 | C2 |
|---|---|---|
| PIC16(L)F15356/75/76/85/86 | • | • |

**FIGURE 23-1: SINGLE COMPARATOR**




**Note:** The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

**EXAMPLE 24-1:**

$V_{RMS}$ = 120

$V_{PEAK} = V_{RMS} * \sqrt{2} = 169.7$

f = 60 Hz

C = 0.1 uF

$Z = V_{PEAK}/3x10^{-4} = 169.7/(3x10^{-4}) = 565.7$ kOhms

$Xc = 1/(2\Pi fC) = 1/(2\Pi * 60 * 1 * 10^{-7}) = 26.53$ kOhms

$R = \sqrt{(Z^2 - Xc^2)} = 565.1$ kOhms (computed)

R = 560 kOhms (used)

$Z_R = \sqrt{(R^2 + Xc^2)} = 560.6$ kOhms (using actual resistor)

$I_{PEAK} = V_{PEAK}/ Z_R = 302.7 * 10^{-6}$

$V_C = Xc * I_{PEAK} = 8.0$ V

$\Phi = Tan^{-1}(Xc/R) = 0.047$ radians

$T_\Phi = \Phi/(2\Pi f) = 125.6$ us

### 24.5.2 CORRECTION BY OFFSET CURRENT

When the waveform is varying relative to $V_{SS}$, then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to $V_{DD}$, then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 24-3.

**EQUATION 24-3: ZCD EVENT OFFSET**

When External Voltage Source is relative to Vss:

$$T_{OFFSET} = \frac{\text{asin}\left(\frac{Vcpinv}{V_{PEAK}}\right)}{2\pi \bullet Freq}$$

When External Voltage Source is relative to $V_{DD}$:

$$T_{OFFSET} = \frac{\text{asin}\left(\frac{V_{DD} - Vcpinv}{V_{PEAK}}\right)}{2\pi \bullet Freq}$$

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to $V_{SS}$. A pull-down resistor is used when the voltage is varying relative to $V_{DD}$. The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the $V_{CPINV}$ switching voltage. The pull-up or pull-down value can be determined with the equation shown in Equation 24-4.

**EQUATION 24-4: ZCD PULL-UP/DOWN**

When External Signal is relative to Vss:

$$R_{PULLUP} = \frac{R_{SERIES}(V_{PULLUP} - Vcpinv)}{Vcpinv}$$

When External Signal is relative to $V_{DD}$:

$$\left(R_{PULLDOWN} = \frac{R_{SERIES} \times (Vcpinv)}{(V_{DD} - Vcpinv)}\right)$$

## 24.6 Handling $V_{PEAK}$ variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of ± 600 μA and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed ± 600 μA and the minimum is at least ± 100 μA, compute the series resistance as shown in Equation 24-5. The compensating pull-up for this series resistance can be determined with Equation 24-4 because the pull-up value is not dependent from the peak voltage.

**EQUATION 24-5: SERIES R FOR V RANGE**

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

## 28.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxMODE<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR6 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 28-1 shows a simplified diagram of the capture operation.

### 28.1.1 CAPTURE SOURCES

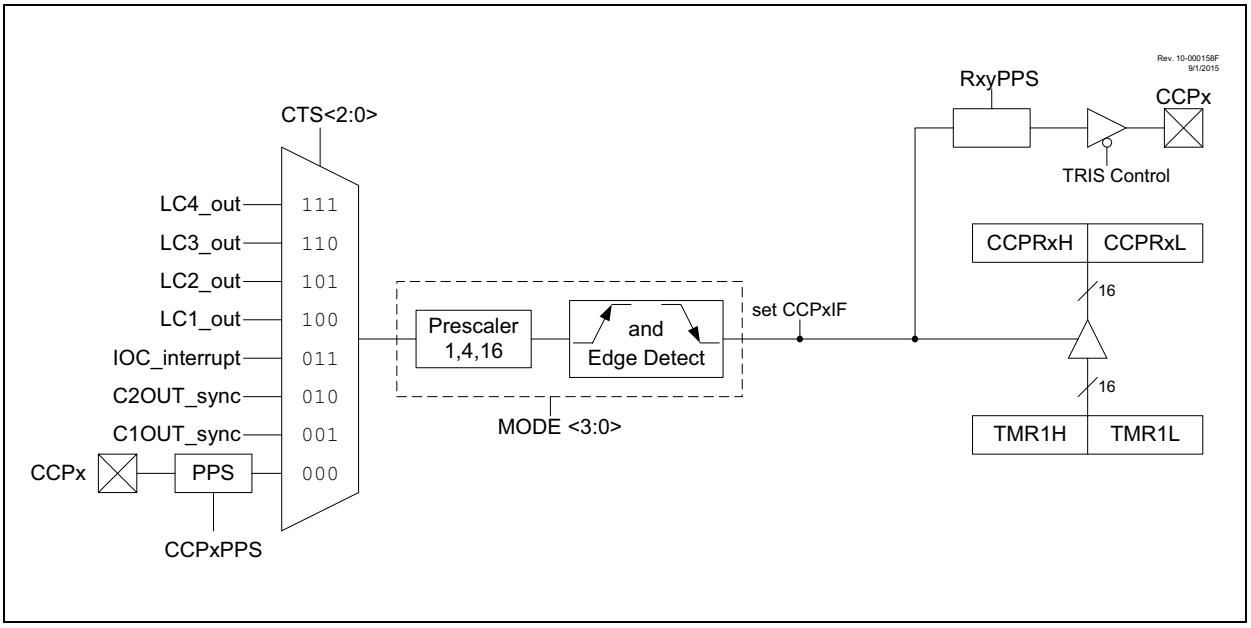
In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

| **Note:** | If the CCPx pin is configured as an output, a write to the port can cause a capture condition. |
|---|---|

The capture source is selected by configuring the CCPxCTS<2:0> bits of the CCPxCAP register. The following sources can be selected:

- CCPxPPS input
- C1OUT_sync
- C2OUT_sync
- IOC_interrupt
- LC1_out
- LC2_out
- LC3_out
- LC4_out

**FIGURE 28-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



**REGISTER 28-1: CCPxCON: CCPx CONTROL REGISTER (CONTINUED)**

bit 3-0 **MODE<3:0>:** CCPx Mode Select bits(1)

1111 - 1100 = PWM mode (Timer2 as the timer source)
1110 = Reserved
1101 = Reserved
1100 = Reserved

1011 = Compare mode: output will pulse 0-1-0; Clears TMR1
1010 = Compare mode: output will pulse 0-1-0
1001 = Compare mode: clear output on compare match
1000 = Compare mode: set output on compare match

0111 = Capture mode: every 16th rising edge of CCPx input
0110 = Capture mode: every 4th rising edge of CCPx input
0101 = Capture mode: every rising edge of CCPx input
0100 = Capture mode: every falling edge of CCPx input

0011 = Capture mode: every edge of CCPx input
0010 = Compare mode: toggle output on match
0001 = Compare mode: toggle output on match; clear TMR1
0000 = Capture/Compare/PWM off (resets CCPx module)

**Note 1:** All modes will set the CCPxIF bit, and will trigger an ADC conversion if CCPx is selected as the ADC trigger source.

**FIGURE 32-12: I²C START AND STOP CONDITIONS**

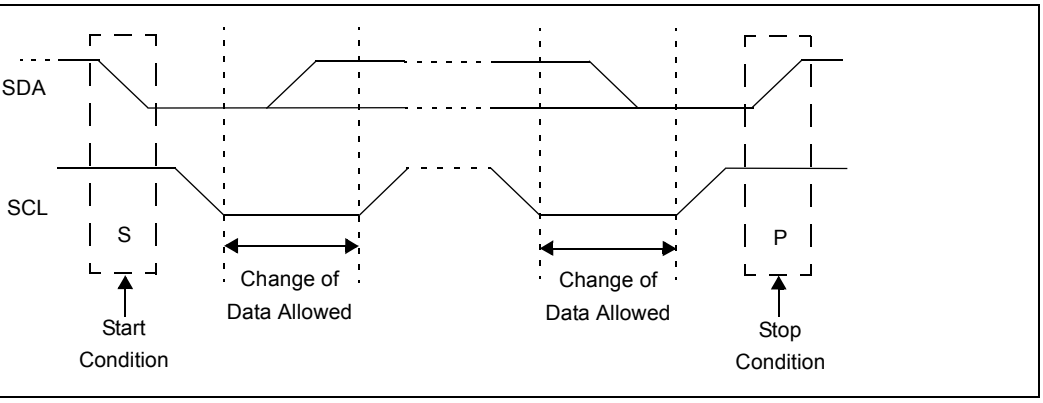
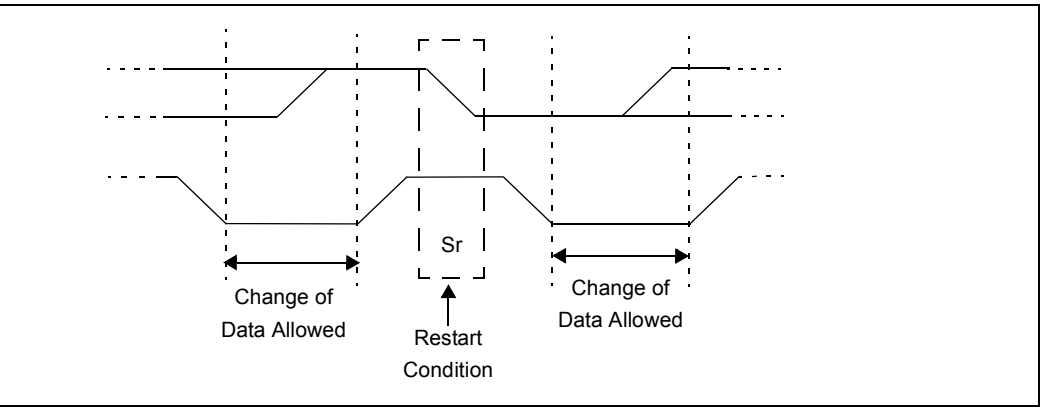



**FIGURE 32-13: I²C RESTART CONDITION**




32.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I²C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ($\overline{ACK}$) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an $\overline{ACK}$ is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the $\overline{ACK}$ value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

There are certain conditions where an $\overline{ACK}$ will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

### 33.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCxSTA register and the received data as indicated by RCxREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

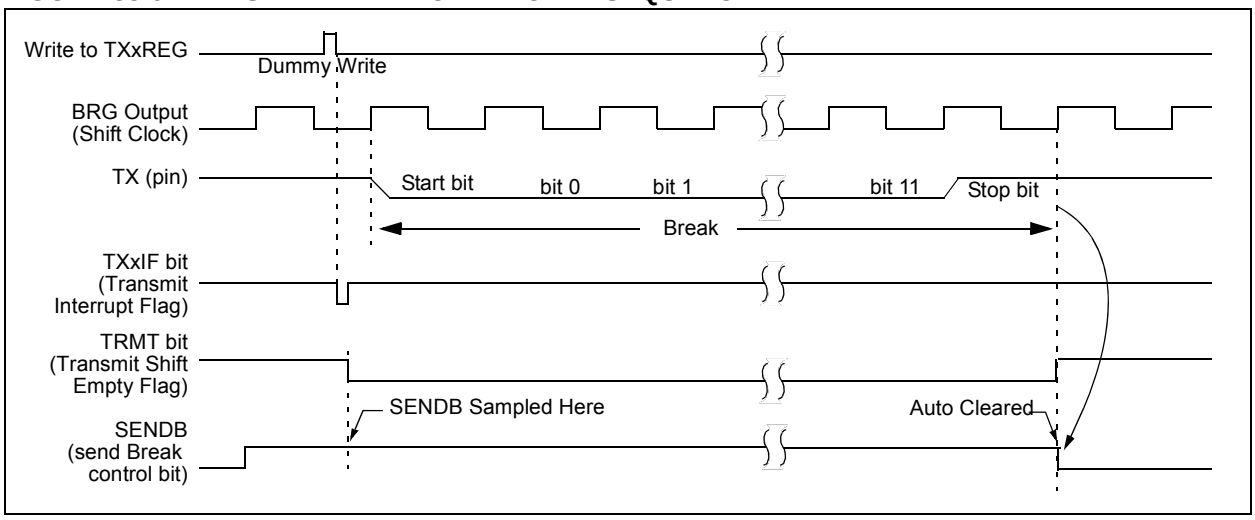
A Break character has been received when:

- RXxIF bit is set
- FERR bit is set
- RCxREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 33.3.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RXxIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDxCON register before placing the EUSART in Sleep mode.

**FIGURE 33-9: SEND BREAK CHARACTER SEQUENCE**



#### 33.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 33.4.1.5 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCxREG register. If the RXxIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

#### 33.4.2.4 Synchronous Slave Reception Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for both the CK and DT pins (if applicable).
3. If interrupts are desired, set the RXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Set the CREN bit to enable reception.
6. The RXxIF bit will be set when reception is complete. An interrupt will be generated if the RXxIE bit was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCxSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCxREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

## 33.6 Register Definitions: EUSART Control

**REGISTER 33-1: TXxSTA: TRANSMIT STATUS AND CONTROL REGISTER**

| R/W-/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R-1/1 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| CSRC | TX9 | TXEN(1) | SYNC | SENDB | BRGH | TRMT | TX9D |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Unused in this mode – value ignored
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send SYNCH BREAK on next transmission – Start bit, followed by 12 '0' bits, followed by Stop bit; cleared by hardware upon completion
0 = SYNCH BREAK transmission disabled or completed
Synchronous mode:
Unused in this mode – value ignored

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode – value ignored

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

**Note 1:** SREN/CREN overrides TXEN in Sync mode.

**REGISTER 33-7: SPxBRGH(1, 2): BAUD RATE GENERATOR HIGH REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPxBRG<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7 **SPxBRG<15:8>:** Upper eight bits of the Baud Rate Generator

**Note 1:** SPxBRGH value is ignored for all modes unless BAUDxCON<BRG16> is active.

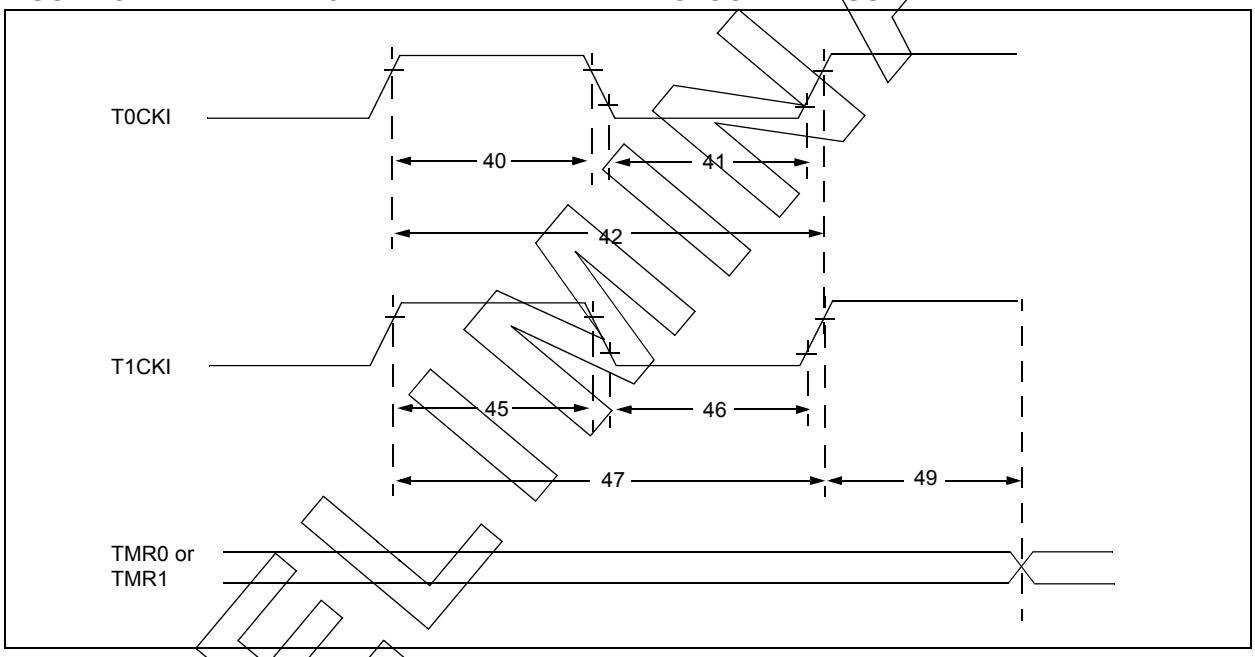
**2:** Writing to SPxBRGH resets the BRG counter.

**TABLE 37-17: ZERO CROSS DETECT (ZCD) SPECIFICATIONS**

| **Standard Operating Conditions (unless otherwise stated)**<br>$V_{DD}$ = 3.0V, $T_A$ = 25°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristics** | **Min.** | **Typ†** | **Max.** | **Units** | **Comments** |
| ZC01 | $V_{PINZC}$ | Voltage on Zero Cross Pin | — | 0.75 | — | V | |
| ZC02 | $I_{ZCD\_MAX}$ | Maximum source or sink current | — | — | 600 | µA | |
| ZC03 | $T_{RESPH}$ | Response Time, Rising Edge | — | 1 | — | µs | |
| | $T_{RESPL}$ | Response Time, Falling Edge | — | 1 | — | µs | |

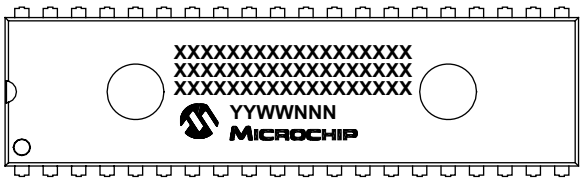
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 37-12: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**

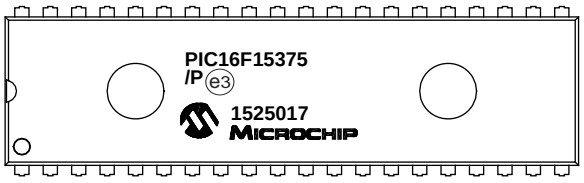


## 40.1 Package Marking Information (Continued)

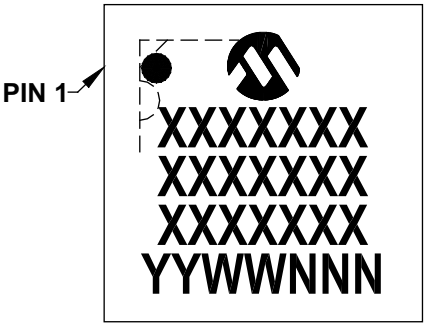
40-Lead PDIP (600 mil)



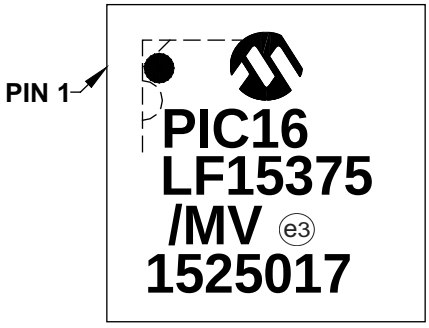

Example




40-Lead UQFN (5x5x0.5 mm)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.