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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cb

Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7312 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. Table 3 shows the SDRAM Interface pin assignments.

Table 3. SDRAM Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
SDCLK		O	SDRAM clock output
SDCKE		O	SDRAM clock enable output
nSDCS[1:0]		O	SDRAM chip select out
WRITE/nSDRAS	(Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS	(Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE	(Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12]	(Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]		O	SDRAM internal bank select
PD[7:6]/SDQM[1:0]	(Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]		O	SDRAM byte lane mask
D[31:0]		I/O	Data I/O

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table 19 on page 11 for more information.

Digital Audio Capability

The EP7312 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7312

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7312 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly. Table 4 shows the UART pin assignments.

Table 4. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Digital Audio Interface (DAI)

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal CS43L41/42/43 low-power audio DACs and the Crystal CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions. Table 5 shows the DAI Interface pin assignments.

Table 5. DAI Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Note: See Table 18 on page 11 for information on pin multiplexes.

DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

Table 14. DC-to-DC Converter Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

Table 15. General Purpose Input/Output Pin Assignments

Pin Mnemonic		I/O	Pin Description
PA[7:0]		I	GPIO port A
PB[7:0]		I	GPIO port B
PD[0]/LEDFLSH	(Note)	I/O	GPIO port D
PD[5:1]		I/O	GPIO port D
PD[7:6]/SDQM[1:0]	(Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0]	(Note)	I	GPIO port E
PE[2]/CLKSEL	(Note)	I	GPIO port E

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

Table 16. Hardware Debug Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Table 17. LED Flasher Pin Assignments

Pin Mnemonic		I/O	Pin Description
PD[0]/LEDFLSH	(Note)	O	LED flasher driver

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	

SDRAM Load Mode Register Cycle

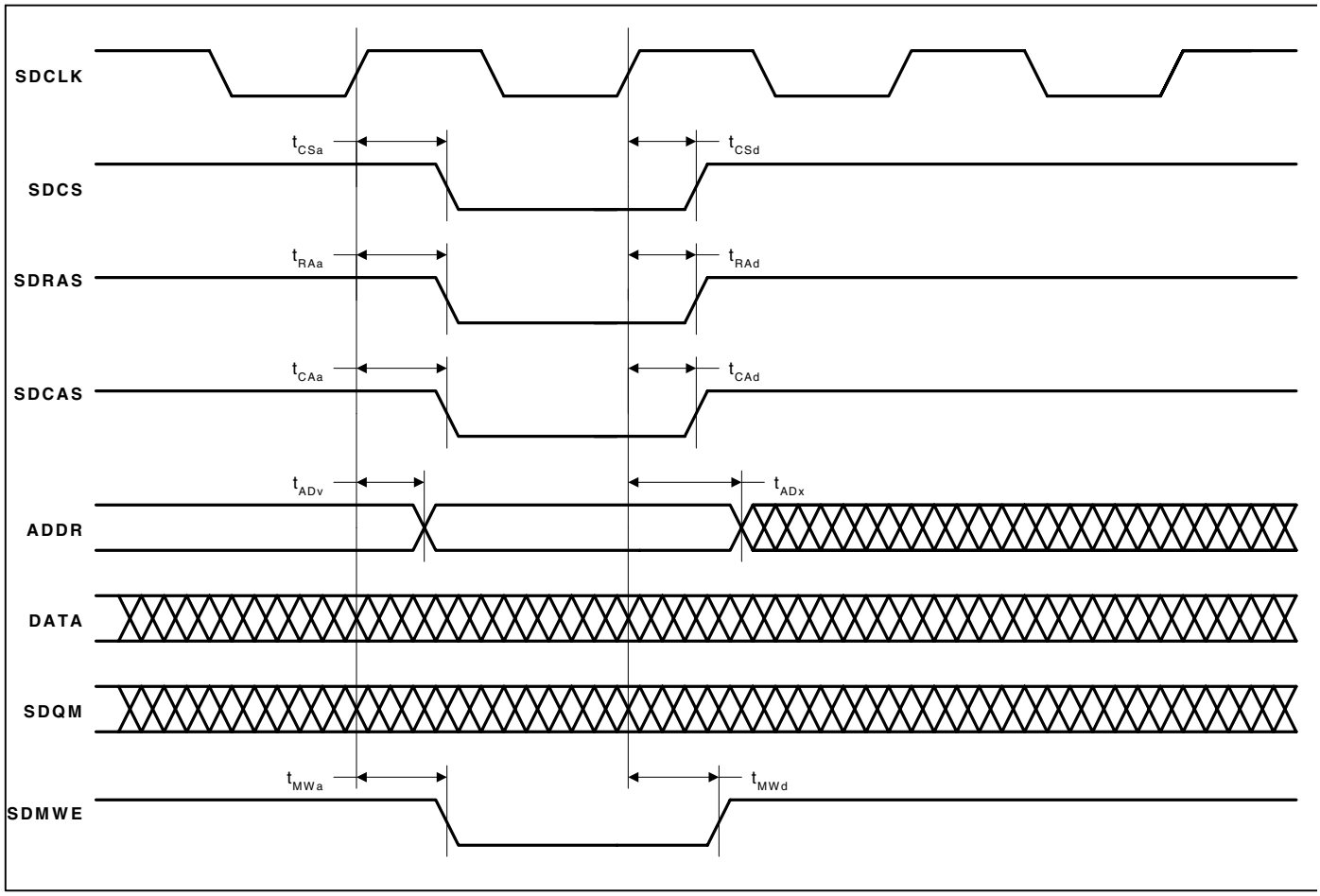


Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory Single Write Cycle

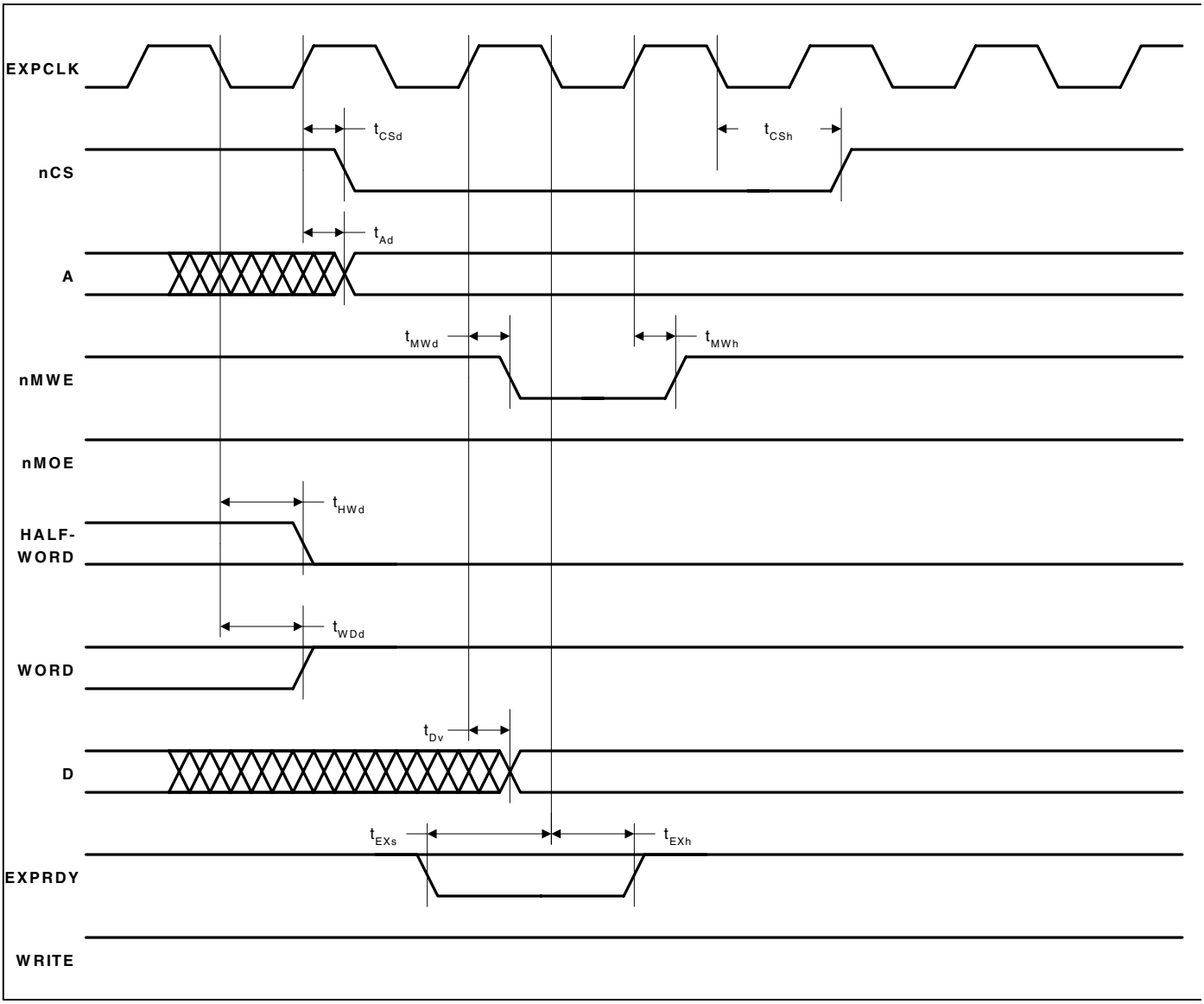


Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

LCD Interface

Parameter	Symbol	Min	Max	Unit
CL[2] falling to CL[1] rising delay time	t_{CL1d}	– 10	25	ns
CL[1] falling to CL[2] rising delay time	t_{CL2d}	80	3,475	ns
CL[1] falling to FRM transition time	t_{FRMd}	300	10,425	ns
CL[1] falling to M transition time	t_{Md}	– 10	20	ns
CL[2] rising to DD (display data) transition time	t_{DDd}	– 10	20	ns

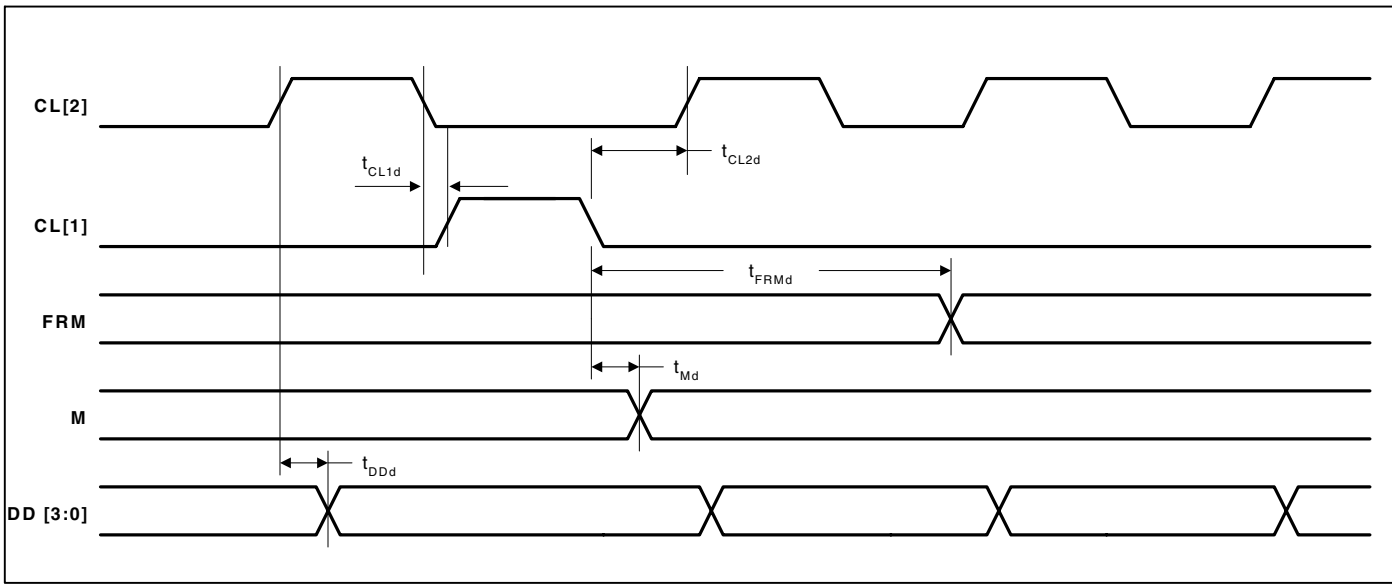


Figure 13. LCD Controller Timing Measurement

JTAG Interface

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	2	-	ns
TCK clock high time	t_{clk_high}	1	-	ns
TCK clock low time	t_{clk_low}	1	-	ns
JTAG port setup time	t_{JPs}	-	0	ns
JTAG port hold time	t_{JPh}	-	3	ns
JTAG port clock to output	t_{JPco}	-	10	ns
JTAG port high impedance to valid output	t_{JPzx}	-	12	ns
JTAG port valid output to high impedance	t_{JPxz}	-	19	ns

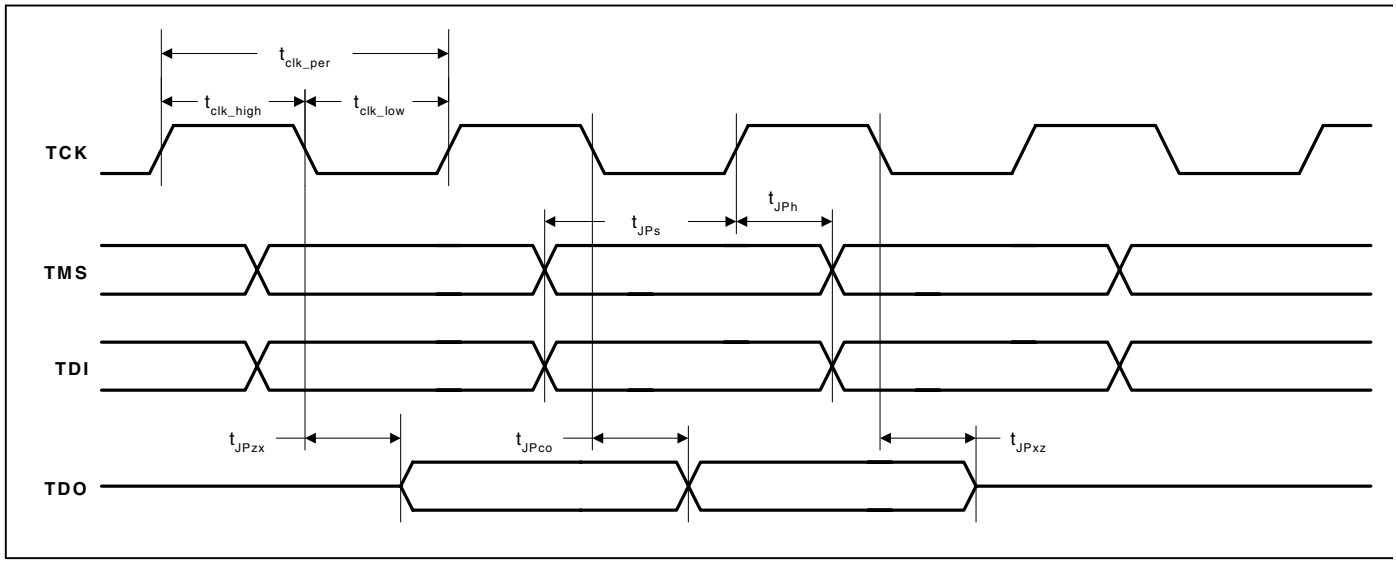


Figure 14. JTAG Timing Measurement

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
38	DSR			I	UART 1 data set ready input
39	nTEST[1]	With p/u*		I	Test mode select input
40	nTEST[0]	With p/u*		I	Test mode select input
41	EINT[3]			I	External interrupt
42	nEINT[2]			I	External interrupt input
43	nEINT[1]			I	External interrupt input
44	nEXTFIQ			I	External fast interrupt input
45	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
46	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
47	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / Boot mode select
48	VSSRTC			RTC Gnd	Real time clock ground
49	RTCOUT			O	Real time clock oscillator output
50	RTCIN			I	Real time clock oscillator input
51	VDDRTC			RTC power	Real time clock power, 2.5 V
52	N/C				
53	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
54	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
55	PD[5]	1	Low	I/O	GPIO port D
56	PD[4]	1	Low	I/O	GPIO port D
57	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
58	TMS	with p/u*		I	JTAG mode select
59	PD[3]	1	Low	I/O	GPIO port D
60	PD[2]	1	Low	I/O	GPIO port D
61	PD[1]	1	Low	I/O	GPIO port D
62	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
63	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
64	VSSIO			Pad Gnd	I/O ground
65	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 serial clock
66	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
67	SSIRXDA			I	DAI/CODEC/SSI2 serial data input
68	SSIRXFR		Input‡	I/O	DAI/CODEC/SSI2 frame sync
69	ADCIN			I	SSI1 ADC serial input
70	nADCCS	1	High	O	SSI1 ADC chip select
71	VSSCORE			Core ground	Core ground
72	VDDCORE			Core Pwr	Core power, 2.5 V
73	VSSIO			Pad Gnd	I/O ground
74	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
75	DRIVE[1]	2	High / Low	I/O	PWM drive output
76	DRIVE[0]	2	High / Low	I/O	PWM drive output
77	ADCCLK	1	Low	O	SSI1 ADC serial clock
78	ADCOUT	1	Low	O	SSI1 ADC serial data output

204-Ball TFBGA Package Characteristics

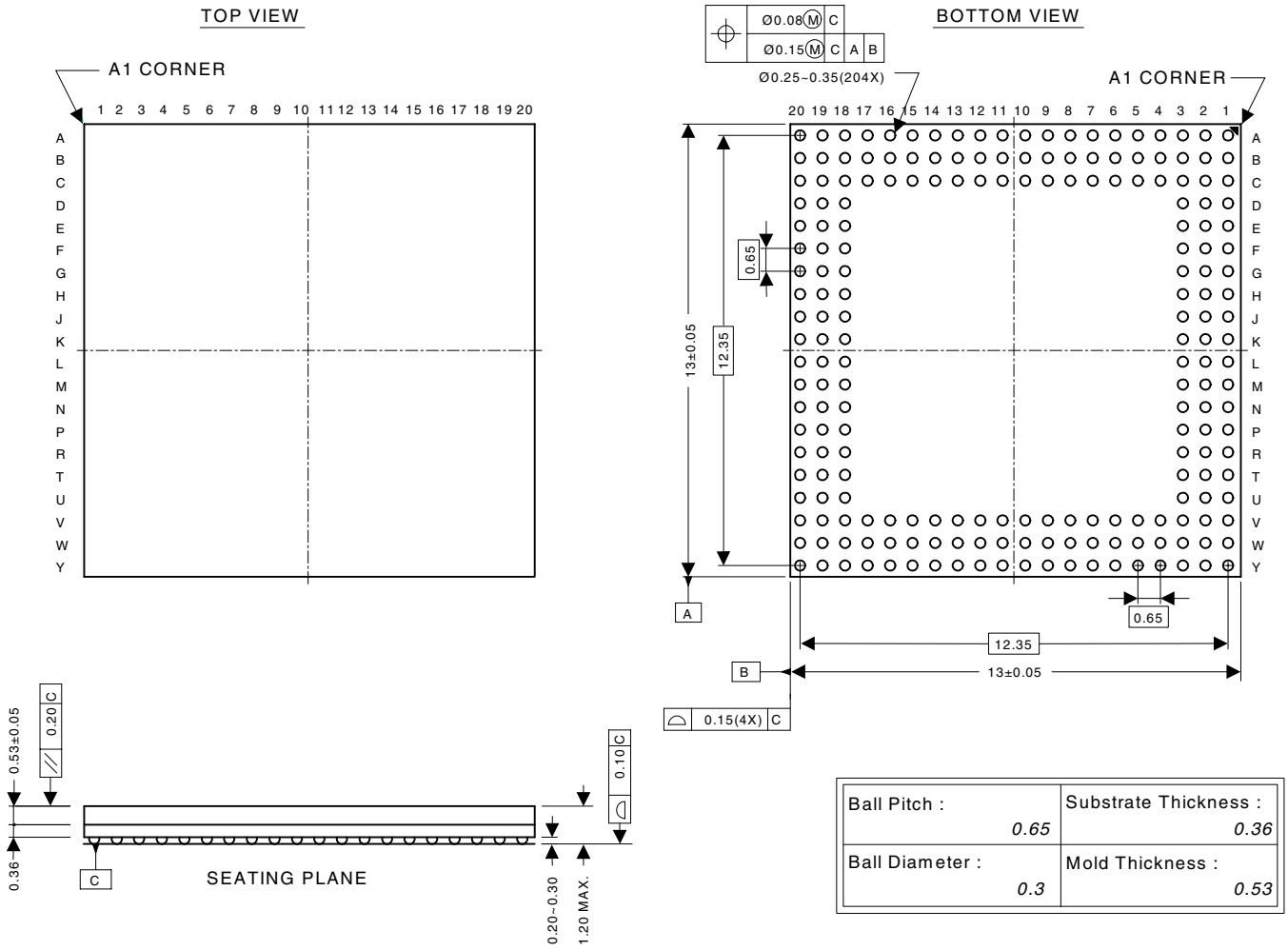


Figure 17. 204-Ball TFBGA Package

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B8	DD[1]	1	Low	O	LCD serial display data
B9	M	1	Low	O	LCD AC bias drive
B10	CL[2]	1	Low	0	LCD pixel clock out
B11	D[0]	1	Low	I/O	Data I/O
B12	A[1]	2	Low	O	System byte address
B13	D[3]	2	Low	I/O	Data I/O
B14	A[4]	1	Low	O	System byte address
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	SDCLK	2	Low	O	SDRAM clock out
C7	SDQM[3]	2	Low	O	SDRAM byte lane mask
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
Y20	VDDIO			Pad power	Digital I/O power, 3.3V

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

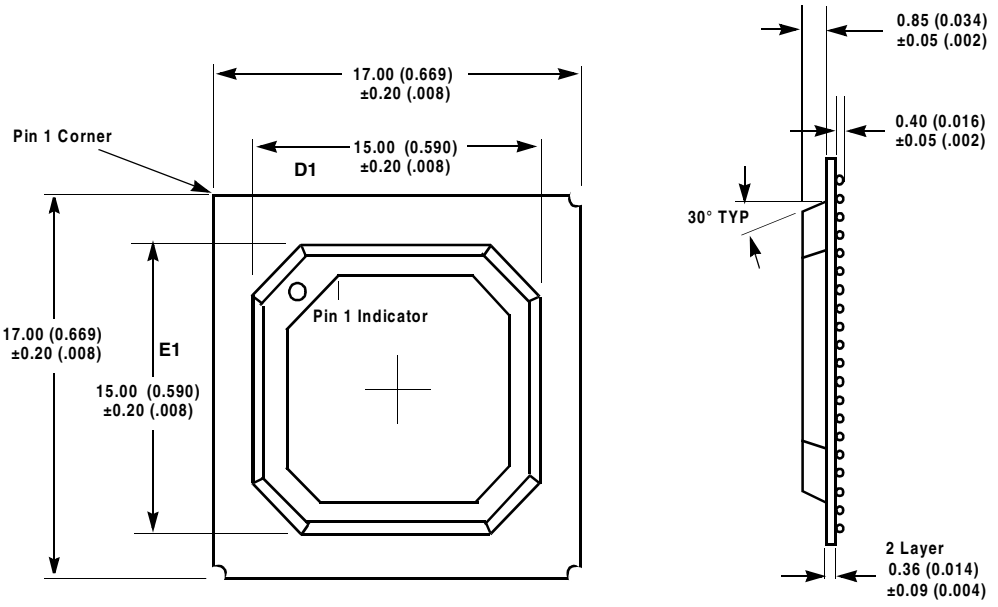
† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

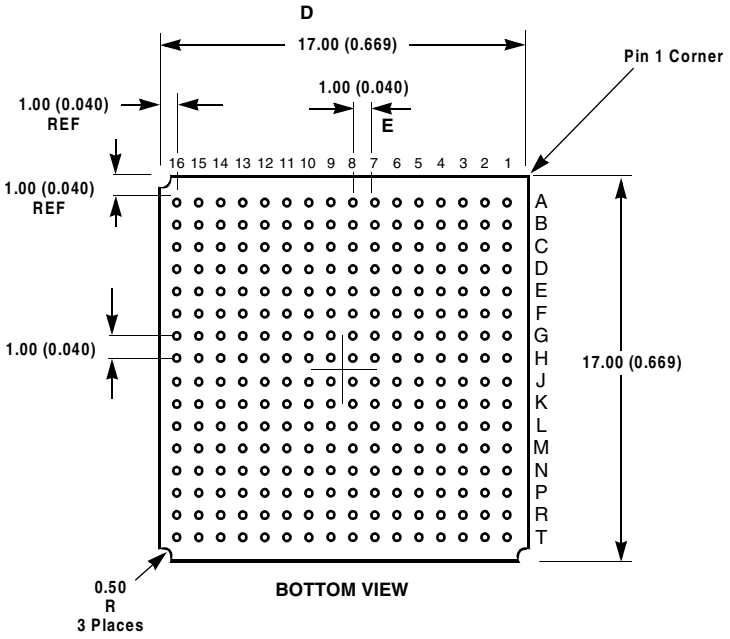
256-Ball PBGA Package Characteristics

Figure 18. 256-Ball PBGA Package

Note: 1) For pin locations see Table 22.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7312 design, contact Cirrus Logic for the latest package information.



TOP VIEW **SIDE VIEW**



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
F10	D[6]	1	Low	I/O	Data I/O
F11	VSSRTC			RTC ground	Real time clock ground
F12	BATOK			I	Battery OK input
F13	nBATCHG			I	Battery changed sense input
F14	VSSIO			Pad ground	I/O ground
F15	D[11]	1	Low	I/O	Data I/O
F16	VDDIO			Pad power	Digital I/O power, 3.3V
G1	PB[1]	1	Input‡	I	GPIO port B
G2	VDDIO			Pad power	Digital I/O power, 3.3V
G3	TDO	1	Input‡	O	JTAG data out
G4	PB[4]	1	Input‡	I	GPIO port B
G5	PB[6]	1	Input‡	I	GPIO port B
G6	VSSCore			Core ground	Core ground
G7	VSSRTC			RTC ground	Real time clock ground
G8	DD[0]	1	Low	O	LCD serial display data
G9	D[3]	1	Low	I/O	Data I/O
G10	VSSRTC			RTC ground	Real time clock ground
G11	A[7]	1	Low	O	System byte address
G12	A[8]	1	Low	O	System byte address
G13	A[9]	1	Low	O	System byte address
G14	VSSIO			Pad ground	I/O ground
G15	D[12]	1	Low	I/O	Data I/O
G16	D[13]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H2	PA[5]	1	Input‡	I/O	GPIO port A
H3	VSSIO			Pad ground	I/O ground
H4	PA[4]	1	Input‡	I/O	GPIO port A
H5	PA[6]	1	Input‡	I/O	GPIO port A
H6	PB[0]	1	Input‡	I/O	GPIO port B
H7	PB[2]	1	Input‡	I/O	GPIO port B
H8	VSSRTC			RTC ground	Real time clock ground
H9	VSSRTC			RTC ground	Real time clock ground
H10	A[10]	1	Low	O	System byte address
H11	A[11]	1	Low	O	System byte address
H12	A[12]	1	Low	O	System byte address
H13	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
H14	VSSIO			Pad ground	I/O ground
H15	D[14]	1	Low	I/O	Data I/O
H16	D[15]	1	Low	I/O	Data I/O
J1	PA[3]	1	Input‡	I/O	GPIO port A
J2	PA[1]	1	Input‡	I/O	GPIO port A
J3	VSSIO			Pad ground	I/O ground
J4	PA[2]	1	Input‡	I/O	GPIO port A

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
206	B4	D5	nCS[2]	O	366
207	A3	B3	nCS[3]	O	368
208	C4	A2	nCS[4]	O	370

1) See EP7312 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.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