Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	90MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	204-TFBGA
Supplier Device Package	204-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cr-90

Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

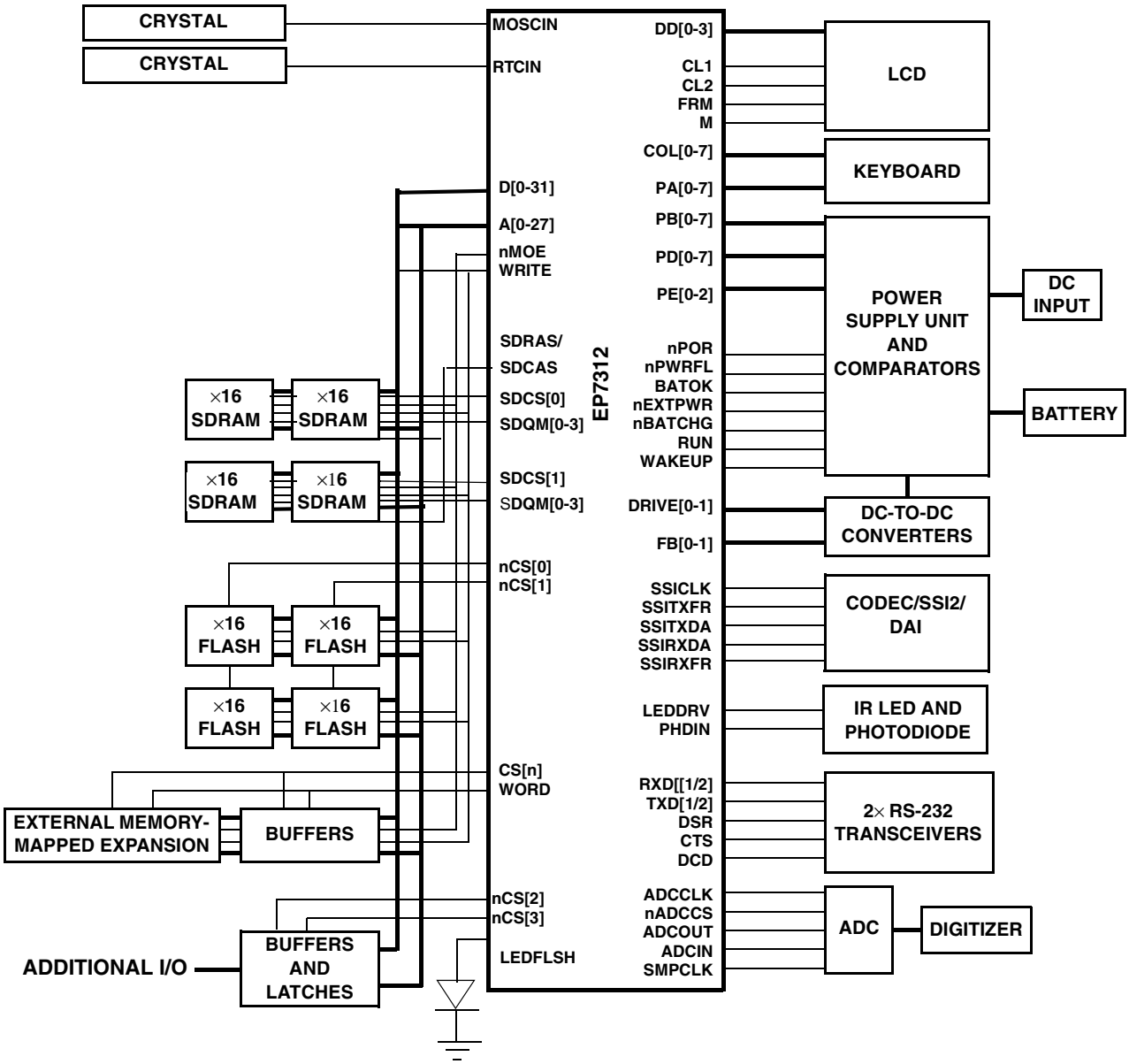


Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @2.5 V[1] I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{IDLE} at 90 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	7 11	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

SDRAM Burst Read Cycle

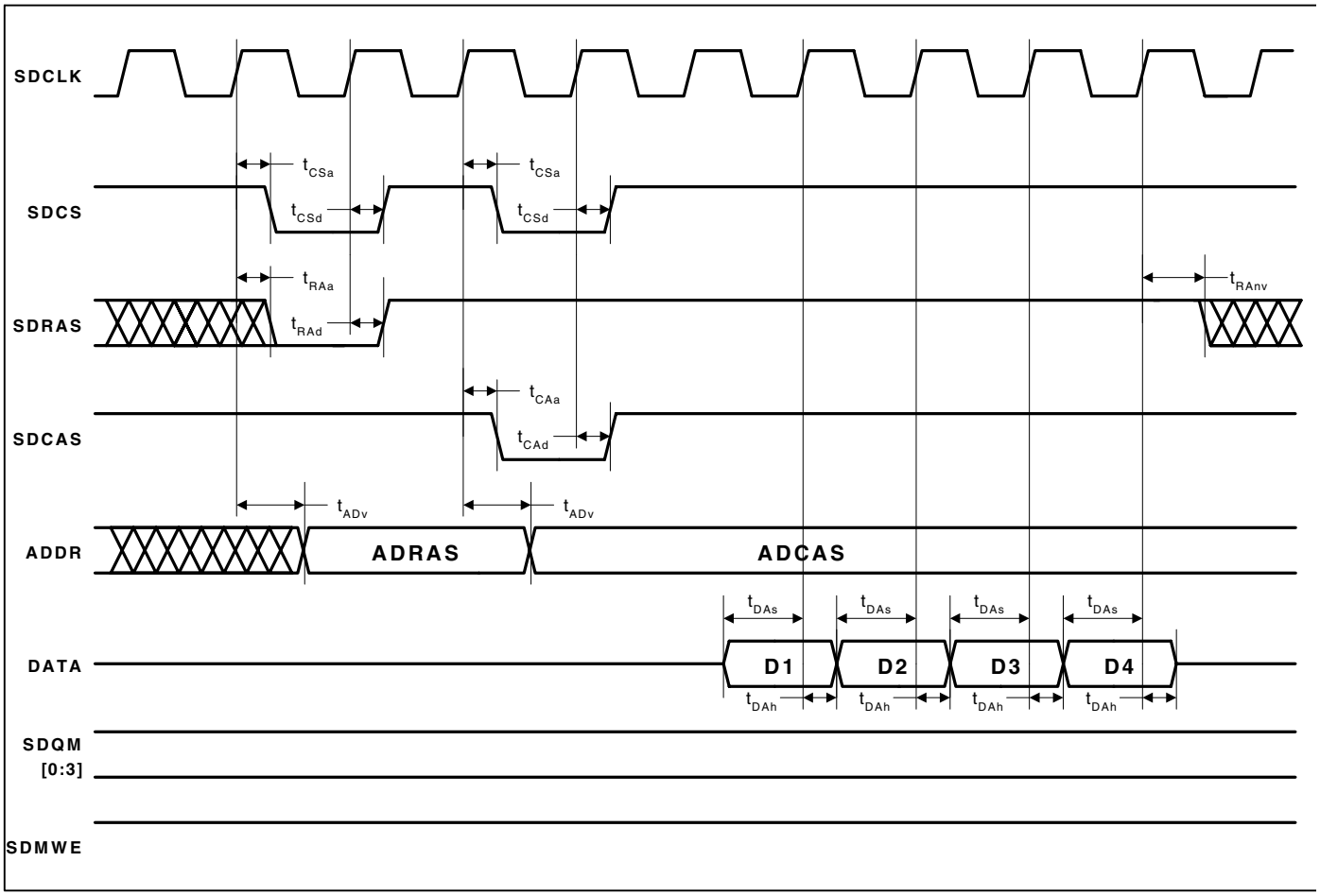


Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal.

Static Memory Single Write Cycle

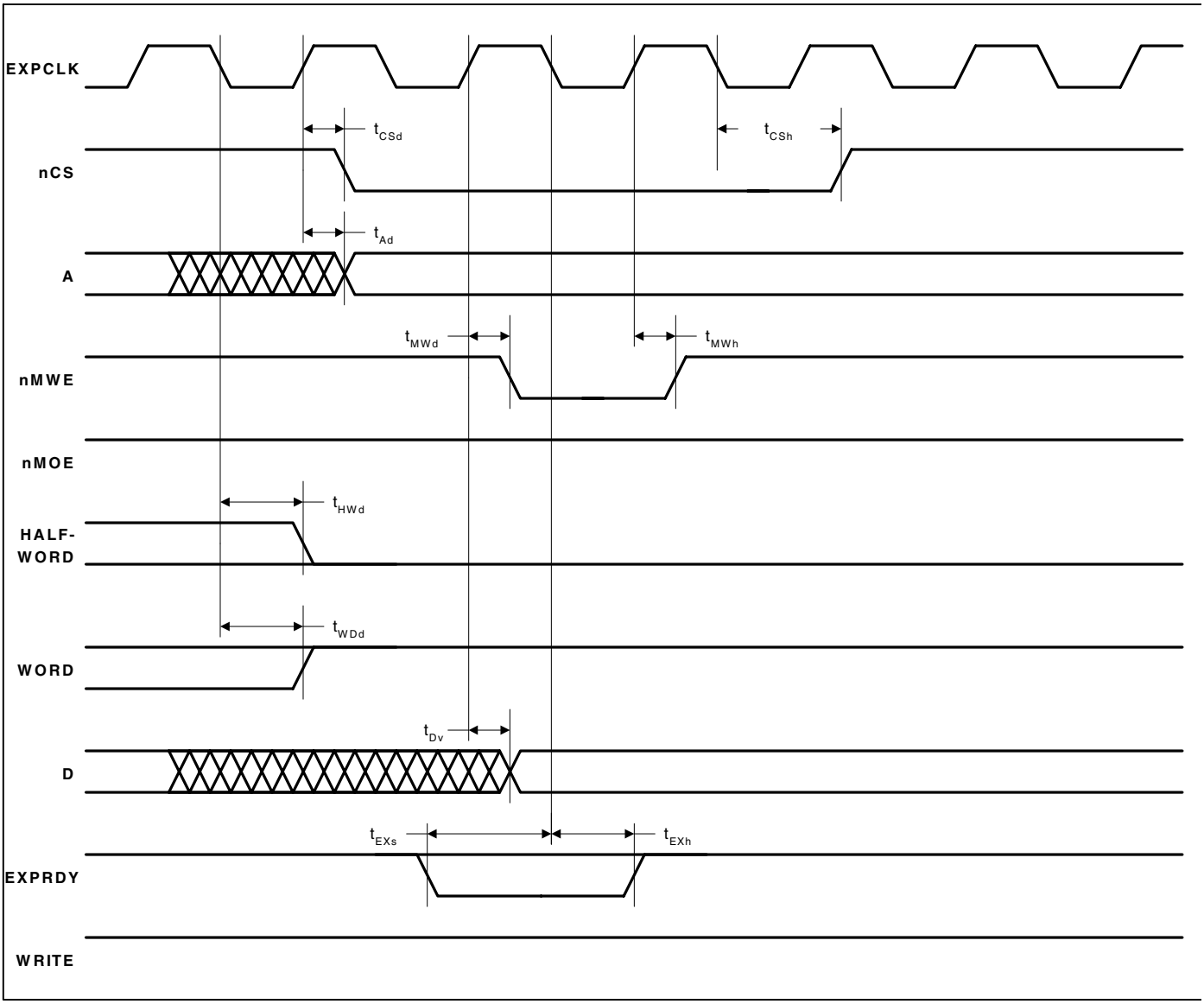


Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

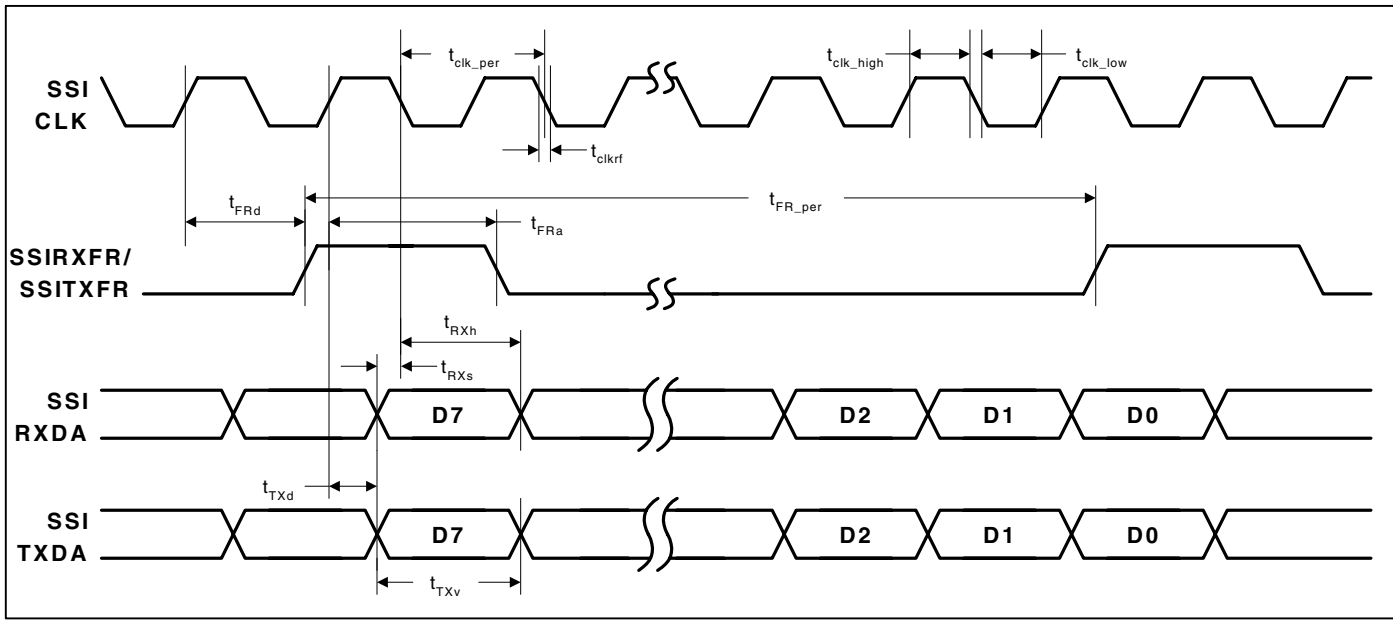


Figure 12. SSI2 Interface Timing Measurement

208-Pin LQFP Pin Diagram

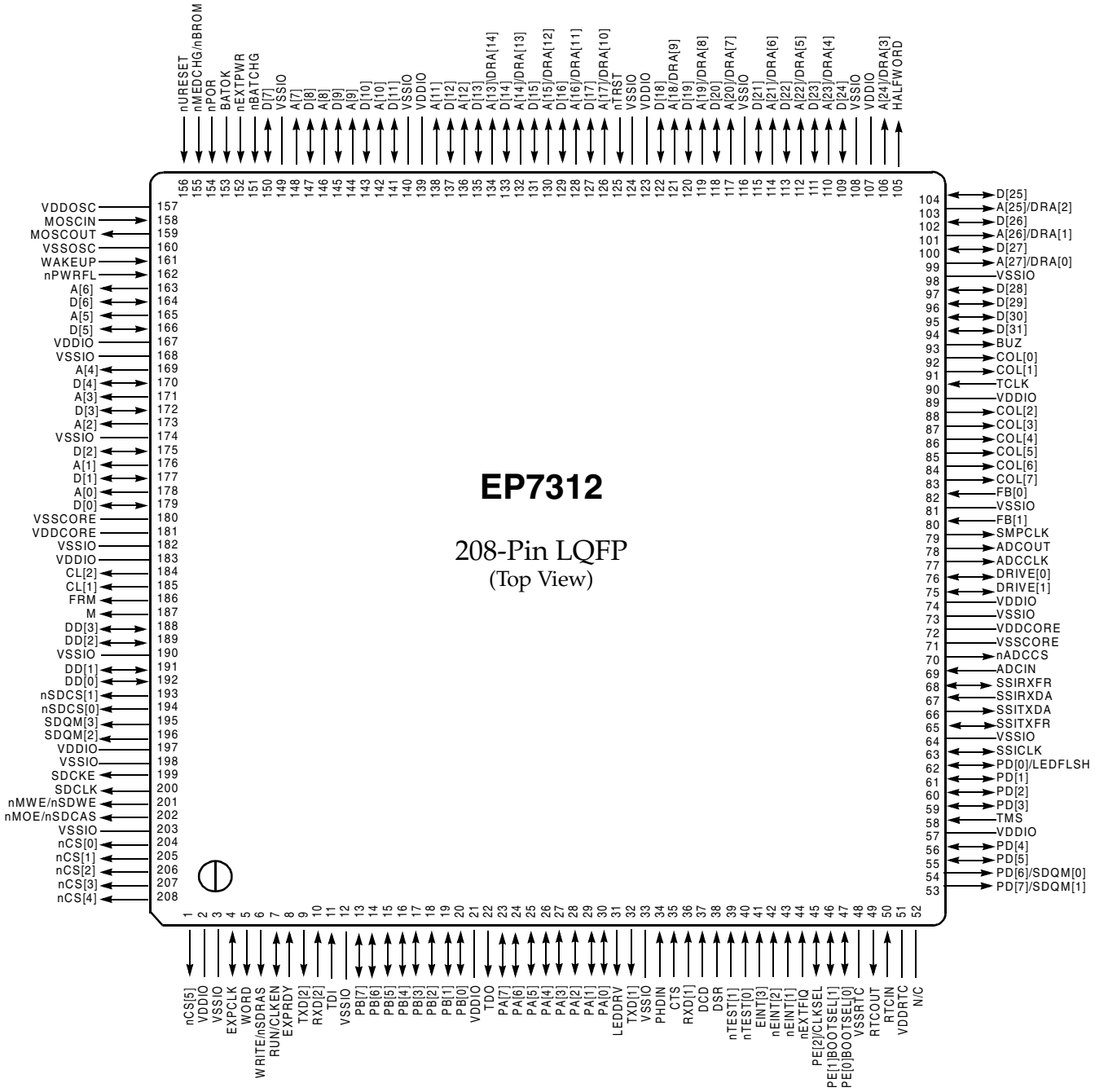


Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Note: 1. N/C should not be grounded but left as no connects.

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
206	nCS[2]	1	High	O	Chip select 2
207	nCS[3]	1	High	O	Chip select 3
208	nCS[4]	1	High	O	Chip select 4

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A
J2	PA[5]	1	Input‡	I/O	GPIO port A
J3	PA[6]	1	Input‡	I/O	GPIO port A
J18	A[11]	1	Low	O	System byte address
J19	D[13]	1	Low	I/O	Data I/O
J20	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
K1	PA[1]	1	Input‡	I/O	GPIO port A
K2	PA[2]	1	Input‡	I/O	GPIO port A
K3	VDDIO			Pad power	Digital I/O power, 3.3V
K18	D[14]	1	Low	I/O	Data I/O
K19	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
K20	D[15]	1	Low	I/O	Data I/O
L1	TXD[1]	1	High	O	UART 1 transmit data out
L2	LEDDRV	1	Low	O	IR LED drive
L3	PA[3]	1	Input‡	I/O	GPIO port A
L18	VDDIO			Pad power	Digital I/O power, 3.3V
L19	D[16]	1	Low	I/O	Data I/O
L20	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
M1	RXD[1]			I	UART 1 receive data input
M2	CTS			I	UART 1 clear to send input
M3	PA[0]	1	Input‡	I/O	GPIO port A
M18	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
M19	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
M20	nTRST			I	JTAG async reset input
N1	DSR			I	UART 1 data set ready input
N2	nTEST[1]	With p/u*		I	Test mode select input
N3	PHDIN			I	Photodiode input

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
Y20	VDDIO			Pad power	Digital I/O power, 3.3V

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

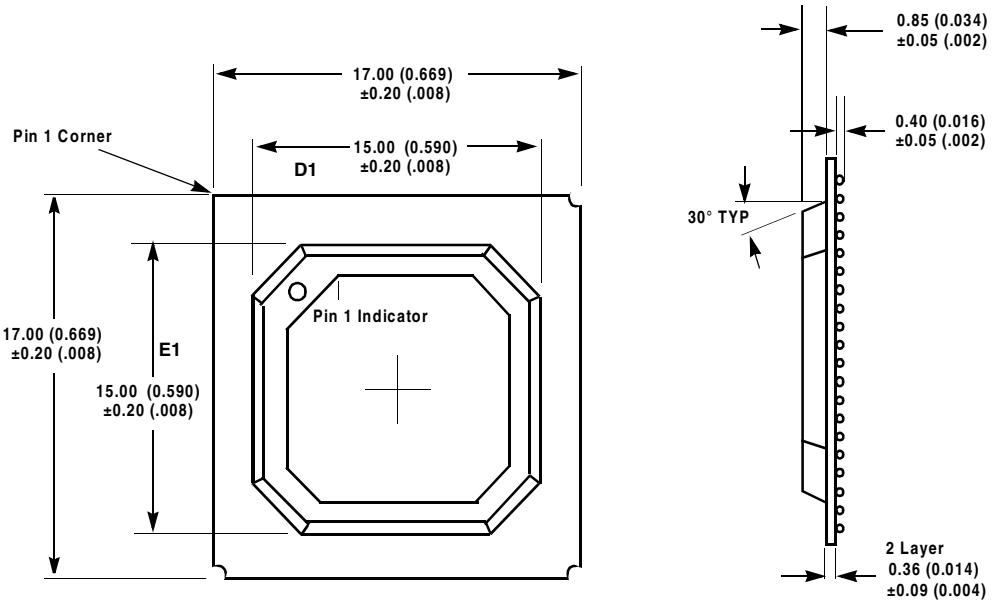
† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

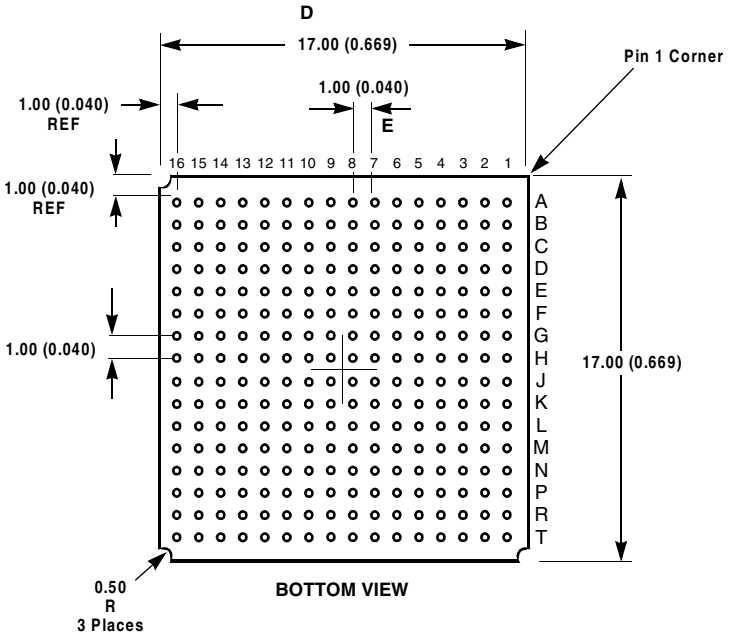
256-Ball PBGA Package Characteristics

Figure 18. 256-Ball PBGA Package

Note: 1) For pin locations see Table 22.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7312 design, contact Cirrus Logic for the latest package information.



TOP VIEW **SIDE VIEW**



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

256-Ball PBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	SDCLK	SDQM[3]	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE/ nSDCAS	VDDIO	nSDCS[1]	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE/ nSDRAS	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE/ nSDWE	nSDCS[0]	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	SDQM[2]	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	SDCKE	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSCore	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]/ DRA[14]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]/ DRA[10]	A[16]/ DRA[11]	A[15]/ DRA[12]	A[14]/ DRA[13]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]/ DRA[5]	A[21]/ DRA[6]	VSSIO	A[18]/ DRA[9]	A[19]/ DRA[8]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]/ DRA[4]	VDDIO	A[20]/ DRA[7]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]/ DRA[0]	A[25]/ DRA[2]	VDDIO	A[24]\ DRA[3]	R
T	VDDRTC	PD[7]/ SDQM[1]	PD[6]/ SDQM[0]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]/ DRA[1]	D[25]	VSSIO	T

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table 22. 256-Ball PBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	nCS[4]	1	High	O	Chip select 4
A3	nCS[1]	1	High	O	Chip select 1
A4	SDCLK	2	Low	O	SDRAM clock out
A5	SDQM[3]	2	Low	O	SDRAM byte lane mask
A6	DD[1]	1	Low	O	LCD serial display data
A7	M	1	Low	O	LCD AC bias drive
A8	VDDIO			Pad power	Digital I/O power, 3.3 V
A9	D[0]	1	Low	I/O	Data I/O
A10	D[2]	1	Low	I/O	Data I/O
A11	A[3]	2	Low	O	System byte address
A12	VDDIO			Pad power	Digital I/O power, 3.3V
A13	A[6]	1	Low	O	System byte address
A14	MOSCOUT			O	Main oscillator out
A15	VDDOSC			Oscillator power	Oscillator power in, 2.5 V
A16	VSSIO			Pad ground	I/O ground
B1	nCS[5]	1	Low	O	Chip select 5
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[3]	1	High	O	Chip select 3
B4	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO			Pad power	Digital I/O power, 3.3 V
B6	nSDCS[1]	1	High	O	SDRAM chip select 1
B7	DD[2]	1	Low	O	LCD serial display data
B8	CL[1]	1	Low	O	LCD line clock
B9	VDDCORE			Core power	Digital core power, 2.5V
B10	D[1]	1	Low	I/O	Data I/O
B11	A[2]	2	Low	O	System byte address
B12	A[4]	1	Low	O	System byte address
B13	A[5]	1	Low	O	System byte address
B14	WAKEUP	Schmitt		I	System wake up input
B15	VDDIO			Pad power	Digital I/O power, 3.3 V
B16	nURESET	Schmitt		I	User reset input
C1	VDDIO			Pad power	Digital I/O power, 3.3V
C2	EXPCLK	1		I	Expansion clock input
C3	VSSIO			Pad ground	I/O ground
C4	VDDIO			Pad power	Digital I/O power, 3.3 V
C5	VSSIO			Pad ground	I/O ground
C6	VSSIO			Pad ground	I/O ground
C7	VSSIO			Pad ground	I/O ground
C8	VDDIO			Pad power	Digital I/O power, 3.3 V
C9	VSSIO			Pad ground	I/O ground
C10	VSSIO			Pad ground	I/O ground
C11	VSSIO			Pad ground	I/O ground
C12	VDDIO			Pad power	Digital I/O power, 3.3 V

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
F10	D[6]	1	Low	I/O	Data I/O
F11	VSSRTC			RTC ground	Real time clock ground
F12	BATOK			I	Battery OK input
F13	nBATCHG			I	Battery changed sense input
F14	VSSIO			Pad ground	I/O ground
F15	D[11]	1	Low	I/O	Data I/O
F16	VDDIO			Pad power	Digital I/O power, 3.3V
G1	PB[1]	1	Input‡	I	GPIO port B
G2	VDDIO			Pad power	Digital I/O power, 3.3V
G3	TDO	1	Input‡	O	JTAG data out
G4	PB[4]	1	Input‡	I	GPIO port B
G5	PB[6]	1	Input‡	I	GPIO port B
G6	VSSCore			Core ground	Core ground
G7	VSSRTC			RTC ground	Real time clock ground
G8	DD[0]	1	Low	O	LCD serial display data
G9	D[3]	1	Low	I/O	Data I/O
G10	VSSRTC			RTC ground	Real time clock ground
G11	A[7]	1	Low	O	System byte address
G12	A[8]	1	Low	O	System byte address
G13	A[9]	1	Low	O	System byte address
G14	VSSIO			Pad ground	I/O ground
G15	D[12]	1	Low	I/O	Data I/O
G16	D[13]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H2	PA[5]	1	Input‡	I/O	GPIO port A
H3	VSSIO			Pad ground	I/O ground
H4	PA[4]	1	Input‡	I/O	GPIO port A
H5	PA[6]	1	Input‡	I/O	GPIO port A
H6	PB[0]	1	Input‡	I/O	GPIO port B
H7	PB[2]	1	Input‡	I/O	GPIO port B
H8	VSSRTC			RTC ground	Real time clock ground
H9	VSSRTC			RTC ground	Real time clock ground
H10	A[10]	1	Low	O	System byte address
H11	A[11]	1	Low	O	System byte address
H12	A[12]	1	Low	O	System byte address
H13	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
H14	VSSIO			Pad ground	I/O ground
H15	D[14]	1	Low	I/O	Data I/O
H16	D[15]	1	Low	I/O	Data I/O
J1	PA[3]	1	Input‡	I/O	GPIO port A
J2	PA[1]	1	Input‡	I/O	GPIO port A
J3	VSSIO			Pad ground	I/O ground
J4	PA[2]	1	Input‡	I/O	GPIO port A

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
M4	PE[0]/BOOTSEL[0]	1	Input‡	I	GPIO port E / Boot mode select
M5	TMS	with p/u*		I	JTAG mode select
M6	VDDIO			Pad power	Digital I/O power, 3.3V
M7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	2	High / Low	I/O	PWM drive output
M9	FB[0]			I	PWM feedback input
M10	COL[0]	1	High	O	Keyboard scanner column drive
M11	D[27]	1	Low	I/O	Data I/O
M12	VSSIO			Pad ground	I/O ground
M13	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
M14	VDDIO			Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
M16	D[21]	1	Low	I/O	Data I/O
N1	nEXTFIQ			I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
N3	VSSIO			Pad ground	I/O ground
N4	VDDIO			Pad power	Digital I/O power, 3.3V
N5	PD[5]	1	Low	I/O	GPIO port D
N6	PD[2]	1	Low	I/O	GPIO port D
N7	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	1	Low	O	SSI1 ADC serial clock
N9	SMPCLK	1	Low	O	SSI1 ADC sample clock
N10	COL[2]	1	High	O	Keyboard scanner column drive
N11	D[29]	1	Low	I/O	Data I/O
N12	D[26]	1	Low	I/O	Data I/O
N13	HALFWORD	1	Low	O	Halfword access select output
N14	VSSIO			Pad ground	I/O ground
N15	D[22]	1	Low	I/O	Data I/O
N16	D[23]	1	Low	I/O	Data I/O
P1	VSSRTC			RTC ground	Real time clock ground
P2	RTCOUT			O	Real time clock oscillator output
P3	VSSIO			Pad ground	I/O ground
P4	VSSIO			Pad ground	I/O ground
P5	VDDIO			Pad power	Digital I/O power, 3.3V
P6	VSSIO			Pad ground	I/O ground
P7	VSSIO			Pad ground	I/O ground
P8	VDDIO			Pad power	Digital I/O power, 3.3V
P9	VSSIO			Pad ground	I/O ground
P10	VDDIO			Pad power	Digital I/O power, 3.3V
P11	VSSIO			Pad ground	I/O ground
P12	VSSIO			Pad ground	I/O ground
P13	VDDIO			Pad power	Digital I/O power
P14	VSSIO			Pad ground	I/O ground
P15	D[24]	1	Low	I/O	Data I/O
P16	VDDIO			Pad power	Digital I/O power, 3.3V
R1	RTCIN			I/O	Real time clock oscillator input
R2	VDDIO			Pad power	Digital I/O power, 3.3V

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
206	B4	D5	nCS[2]	O	366
207	A3	B3	nCS[3]	O	368
208	C4	A2	nCS[4]	O	370

1) See EP7312 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.


CIRRUS LOGIC®