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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	204-TFBGA
Supplier Device Package	204-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cr

FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Table of Contents

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:

http://www.cirrus.com/corporate/contacts/sales.cfm

Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Pin Multiplexing

Table 18 shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the *EP7312 User's Manual* for more information).

Table 18. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 19 shows the pins that have been multiplexed in the EP7312.

Table 19. Pin Multiplexing

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @2.5 V[1] I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{IDLE} at 90 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	7 11	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

SDRAM Refresh Cycle

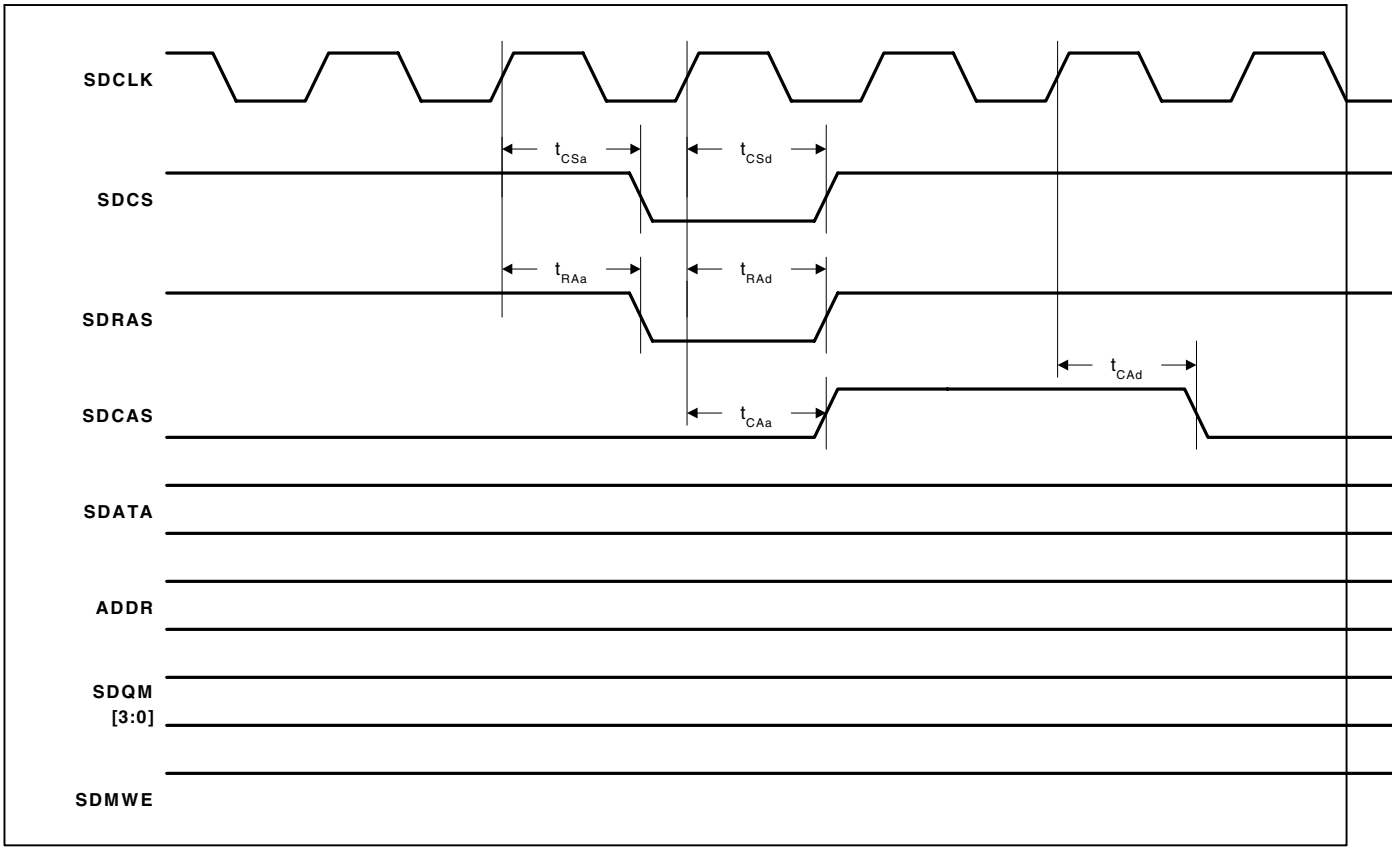

Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Read Cycle

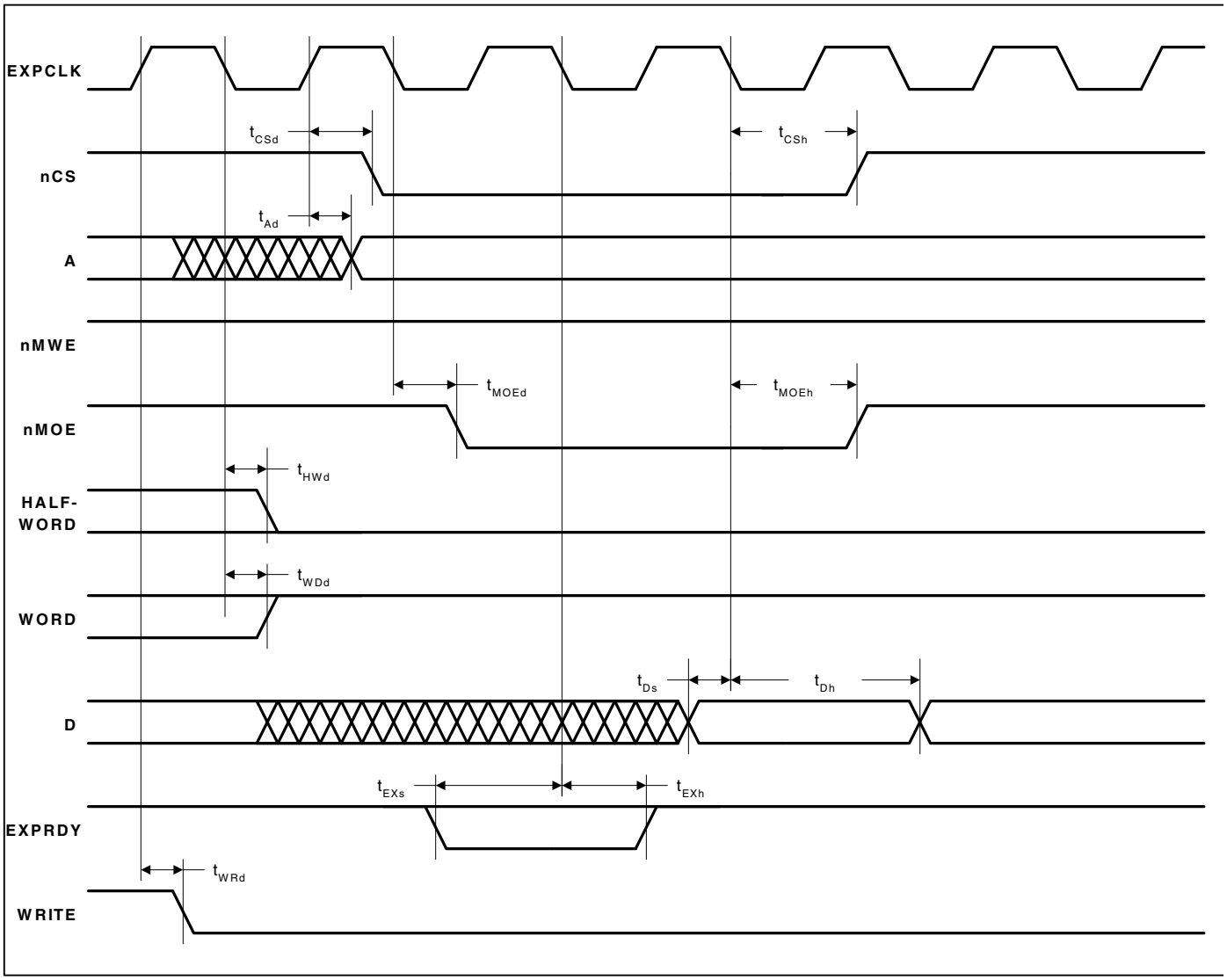

Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Read Cycle

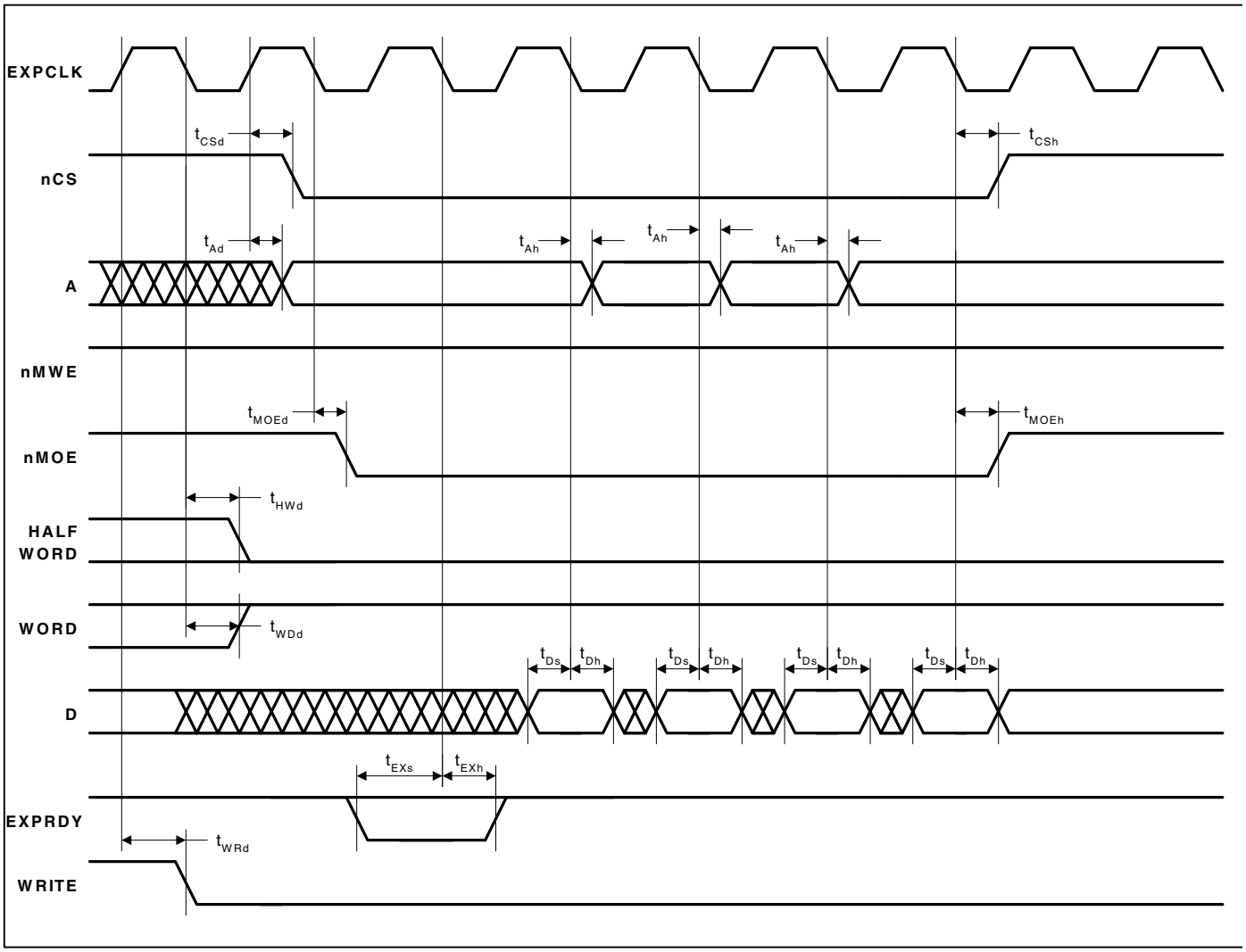

Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

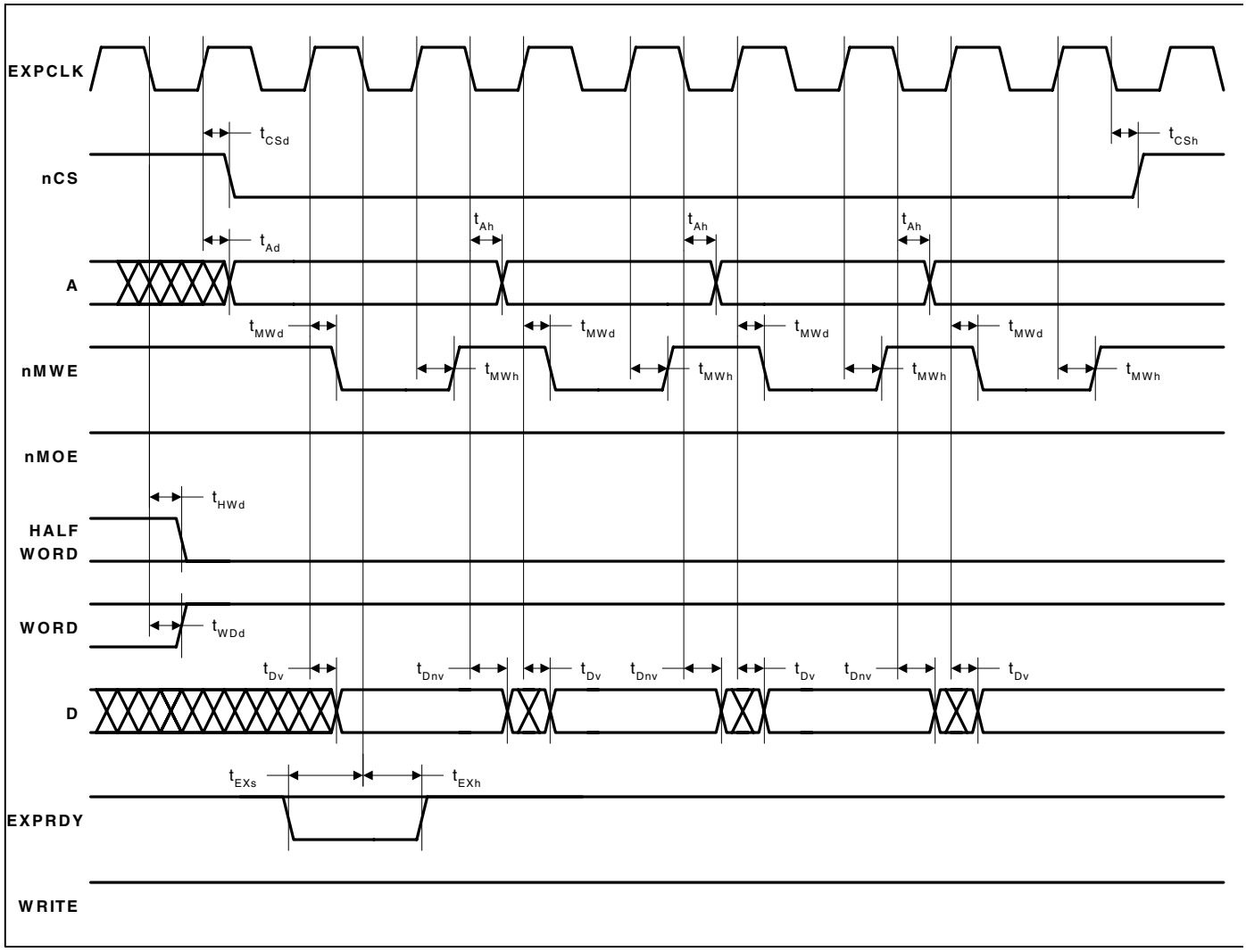

Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

LCD Interface

Parameter	Symbol	Min	Max	Unit
CL[2] falling to CL[1] rising delay time	t_{CL1d}	– 10	25	ns
CL[1] falling to CL[2] rising delay time	t_{CL2d}	80	3,475	ns
CL[1] falling to FRM transition time	t_{FRMd}	300	10,425	ns
CL[1] falling to M transition time	t_{Md}	– 10	20	ns
CL[2] rising to DD (display data) transition time	t_{DDd}	– 10	20	ns

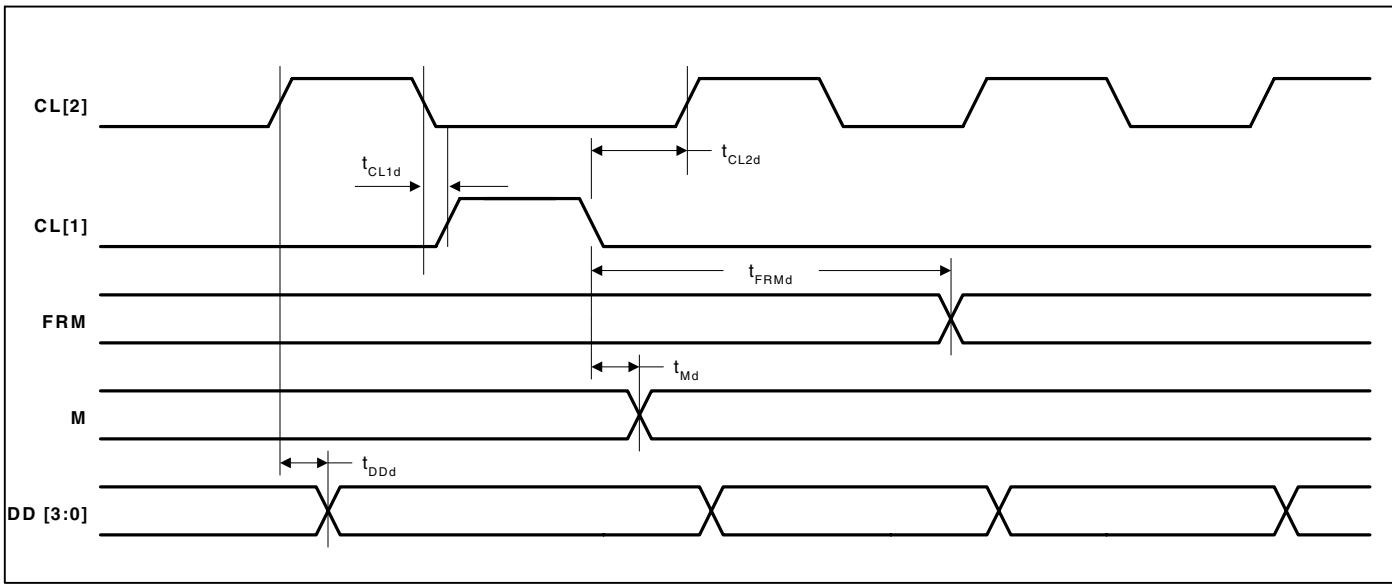

Figure 13. LCD Controller Timing Measurement

JTAG Interface

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	2	-	ns
TCK clock high time	t_{clk_high}	1	-	ns
TCK clock low time	t_{clk_low}	1	-	ns
JTAG port setup time	t_{JPs}	-	0	ns
JTAG port hold time	t_{JPh}	-	3	ns
JTAG port clock to output	t_{JPco}	-	10	ns
JTAG port high impedance to valid output	t_{JPzx}	-	12	ns
JTAG port valid output to high impedance	t_{JPxz}	-	19	ns

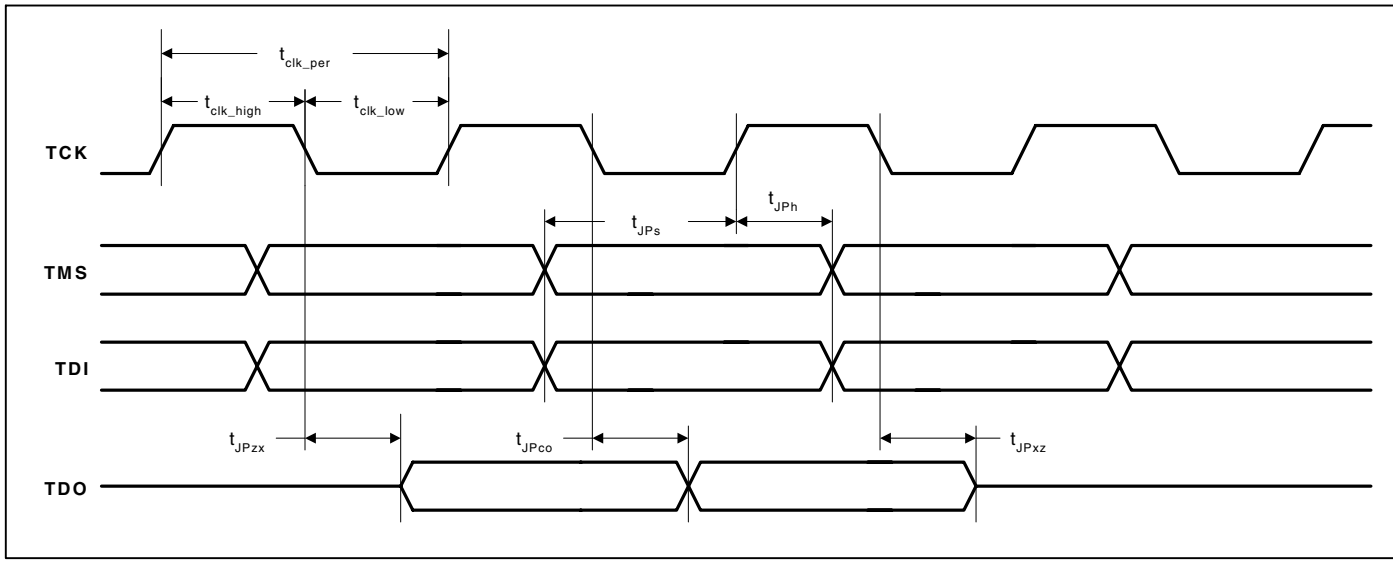

Figure 14. JTAG Timing Measurement

Packages

208-Pin LQFP Package Characteristics

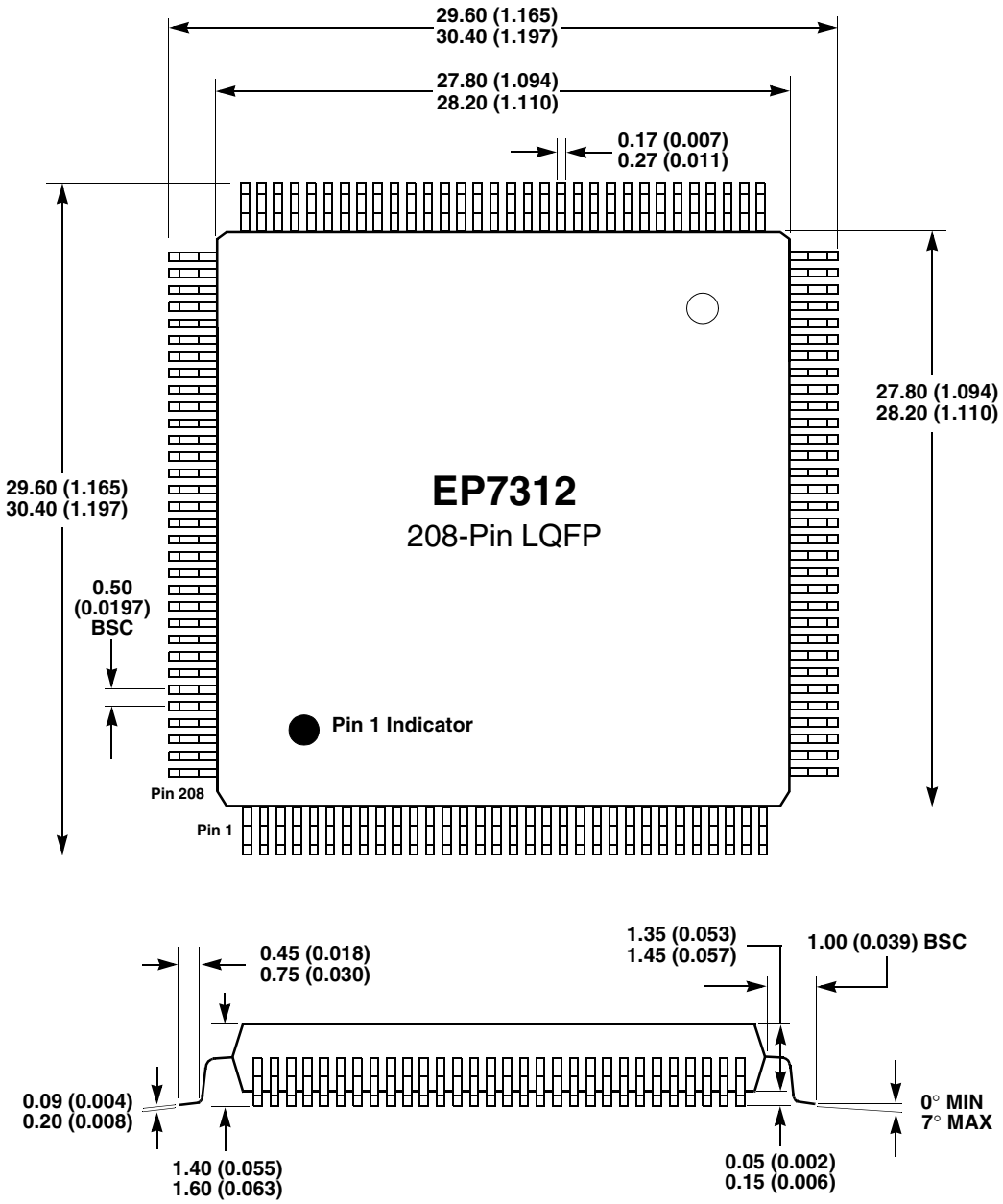

Figure 15. 208-Pin LQFP Package Outline Drawing

Note: 1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 16. For pin descriptions see the EP7312 User's Manual.

208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
206	nCS[2]	1	High	O	Chip select 2
207	nCS[3]	1	High	O	Chip select 3
208	nCS[4]	1	High	O	Chip select 4

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
F10	D[6]	1	Low	I/O	Data I/O
F11	VSSRTC			RTC ground	Real time clock ground
F12	BATOK			I	Battery OK input
F13	nBATCHG			I	Battery changed sense input
F14	VSSIO			Pad ground	I/O ground
F15	D[11]	1	Low	I/O	Data I/O
F16	VDDIO			Pad power	Digital I/O power, 3.3V
G1	PB[1]	1	Input‡	I	GPIO port B
G2	VDDIO			Pad power	Digital I/O power, 3.3V
G3	TDO	1	Input‡	O	JTAG data out
G4	PB[4]	1	Input‡	I	GPIO port B
G5	PB[6]	1	Input‡	I	GPIO port B
G6	VSSCore			Core ground	Core ground
G7	VSSRTC			RTC ground	Real time clock ground
G8	DD[0]	1	Low	O	LCD serial display data
G9	D[3]	1	Low	I/O	Data I/O
G10	VSSRTC			RTC ground	Real time clock ground
G11	A[7]	1	Low	O	System byte address
G12	A[8]	1	Low	O	System byte address
G13	A[9]	1	Low	O	System byte address
G14	VSSIO			Pad ground	I/O ground
G15	D[12]	1	Low	I/O	Data I/O
G16	D[13]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H2	PA[5]	1	Input‡	I/O	GPIO port A
H3	VSSIO			Pad ground	I/O ground
H4	PA[4]	1	Input‡	I/O	GPIO port A
H5	PA[6]	1	Input‡	I/O	GPIO port A
H6	PB[0]	1	Input‡	I/O	GPIO port B
H7	PB[2]	1	Input‡	I/O	GPIO port B
H8	VSSRTC			RTC ground	Real time clock ground
H9	VSSRTC			RTC ground	Real time clock ground
H10	A[10]	1	Low	O	System byte address
H11	A[11]	1	Low	O	System byte address
H12	A[12]	1	Low	O	System byte address
H13	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
H14	VSSIO			Pad ground	I/O ground
H15	D[14]	1	Low	I/O	Data I/O
H16	D[15]	1	Low	I/O	Data I/O
J1	PA[3]	1	Input‡	I/O	GPIO port A
J2	PA[1]	1	Input‡	I/O	GPIO port A
J3	VSSIO			Pad ground	I/O ground
J4	PA[2]	1	Input‡	I/O	GPIO port A

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
M4	PE[0]/BOOTSEL[0]	1	Input‡	I	GPIO port E / Boot mode select
M5	TMS	with p/u*		I	JTAG mode select
M6	VDDIO			Pad power	Digital I/O power, 3.3V
M7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	2	High / Low	I/O	PWM drive output
M9	FB[0]			I	PWM feedback input
M10	COL[0]	1	High	O	Keyboard scanner column drive
M11	D[27]	1	Low	I/O	Data I/O
M12	VSSIO			Pad ground	I/O ground
M13	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
M14	VDDIO			Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
M16	D[21]	1	Low	I/O	Data I/O
N1	nEXTFIQ			I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
N3	VSSIO			Pad ground	I/O ground
N4	VDDIO			Pad power	Digital I/O power, 3.3V
N5	PD[5]	1	Low	I/O	GPIO port D
N6	PD[2]	1	Low	I/O	GPIO port D
N7	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	1	Low	O	SSI1 ADC serial clock
N9	SMPCLK	1	Low	O	SSI1 ADC sample clock
N10	COL[2]	1	High	O	Keyboard scanner column drive
N11	D[29]	1	Low	I/O	Data I/O
N12	D[26]	1	Low	I/O	Data I/O
N13	HALFWORD	1	Low	O	Halfword access select output
N14	VSSIO			Pad ground	I/O ground
N15	D[22]	1	Low	I/O	Data I/O
N16	D[23]	1	Low	I/O	Data I/O
P1	VSSRTC			RTC ground	Real time clock ground
P2	RTCOUT			O	Real time clock oscillator output
P3	VSSIO			Pad ground	I/O ground
P4	VSSIO			Pad ground	I/O ground
P5	VDDIO			Pad power	Digital I/O power, 3.3V
P6	VSSIO			Pad ground	I/O ground
P7	VSSIO			Pad ground	I/O ground
P8	VDDIO			Pad power	Digital I/O power, 3.3V
P9	VSSIO			Pad ground	I/O ground
P10	VDDIO			Pad power	Digital I/O power, 3.3V
P11	VSSIO			Pad ground	I/O ground
P12	VSSIO			Pad ground	I/O ground
P13	VDDIO			Pad power	Digital I/O power
P14	VSSIO			Pad ground	I/O ground
P15	D[24]	1	Low	I/O	Data I/O
P16	VDDIO			Pad power	Digital I/O power, 3.3V
R1	RTCIN			I/O	Real time clock oscillator input
R2	VDDIO			Pad power	Digital I/O power, 3.3V

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
110	U20	M13	A[23]/DRA[4]	O	194
111	T19	N16	D[23]	I/O	196
112	T20	L12	A[22]/DRA[5]	O	199
113	R19	N15	D[22]	I/O	201
114	R20	L13	A[21]/DRA[6]	O	204
115	T18	M16	D[21]	I/O	206
117	P19	M15	A[20]/DRA[7]	O	209
118	P20	K11	D[20]	I/O	211
119	R18	L16	A[19]/DRA[8]	O	214
120	N19	K12	D[19]	I/O	216
121	N20	L15	A[18]/DRA[9]	O	219
122	P18	K13	D[18]	I/O	221
126	M19	J10	A[17]/DRA[10]	O	224
127	N18	J16	D[17]	I/O	226
128	L20	J11	A[16]/DRA[11]	O	229
129	L19	J15	D[16]	I/O	231
130	M18	J12	A[15]/DRA[12]	O	234
131	K20	H16	D[15]	I/O	236
132	K19	J13	A[14]/DRA[13]	O	239
133	K18	H15	D[14]	I/O	241
134	J20	H13	A[13]/DRA[14]	O	244
135	J19	G16	D[13]	I/O	246
136	H20	H12	A[12]	O	249
137	H19	G15	D[12]	I/O	251
138	J18	H11	A[11]	O	254
141	G20	F15	D[11]	I/O	256
142	H18	H10	A[10]	O	259
143	F20	E16	D[10]	I/O	261
144	G19	G13	A[9]	O	264
145	E20	E15	D[9]	I/O	266
146	F19	G12	A[8]	O	269
147	G18	D16	D[8]	I/O	271
148	D20	G11	A[7]	O	274
150	F18	D15	D[7]	I/O	276
151	D19	F13	nBATCHG	I	279
152	E19	C16	nEXTPWR	I	280
153	C19	F12	BATOK	I	281
154	C20	C15	nPOR	I	282

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
155	E18	E13	nMEDCHG/nBROM	I	283
156	B20	B16	nURESET	I	284
161	B16	B14	WAKEUP	I	285
162	A16	D11	nPWRFL	I	286
163	C15	A13	A[6]	O	287
164	B15	F10	D[6]	I/O	289
165	A15	B13	A[5]	O	292
166	C14	E10	D[5]	I/O	294
169	B14	B12	A[4]	O	297
170	A14	D10	D[4]	I/O	299
171	C13	A11	A[3]	O	302
172	B13	G9	D[3]	I/O	304
173	A13	B11	A[2]	O	307
175	C12	A10	D[2]	I/O	309
176	B12	F9	A[1]	O	312
177	A12	B10	D[1]	I/O	314
178	C11	E9	A[0]	O	317
179	B11	A9	D[0]	I/O	319
184	B10	D8	CL2	O	322
185	A10	B8	CL1	O	324
186	A9	E8	FRM	O	326
187	B9	A7	M	O	328
188	C9	F8	DD[3]	O	330
189	A8	B7	DD[2]	O	333
191	B8	A6	DD[1]	O	336
192	C8	G8	DD[0]	O	339
193	A7	B6	nSDCS[1]	O	342
194	B7	D7	nSDCS[0]	O	344
195	C7	A5	SDQM[3]	I/O	346
196	A6	E7	SDQM[2]	I/O	349
199	B6	F7	SDCKE	I/O	352
200	C6	A4	SDCLK	I/O	355
201	A5	D6	nMWE/nSDWE	O	358
202	B5	B4	nMOE/nSDCAS	O	360
204	C5	E6	nCS[0]	O	362
205	A4	A3	nCS[1]	O	364