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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	90MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cv-90

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7312 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. Table 3 shows the SDRAM Interface pin assignments.

Table 3. SDRAM Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
SDCLK		O	SDRAM clock output
SDCKE		O	SDRAM clock enable output
nSDCS[1:0]		O	SDRAM chip select out
WRITE/nSDRAS	(Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS	(Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE	(Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12]	(Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]		O	SDRAM internal bank select
PD[7:6]/SDQM[1:0]	(Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]		O	SDRAM byte lane mask
D[31:0]		I/O	Data I/O

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table 19 on page 11 for more information.

Digital Audio Capability

The EP7312 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7312

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7312 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly. Table 4 shows the UART pin assignments.

Table 4. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Digital Audio Interface (DAI)

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal CS43L41/42/43 low-power audio DACs and the Crystal CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions. Table 5 shows the DAI Interface pin assignments.

Table 5. DAI Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Note: See Table 18 on page 11 for information on pin multiplexes.

DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

Table 14. DC-to-DC Converter Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

Table 15. General Purpose Input/Output Pin Assignments

Pin Mnemonic		I/O	Pin Description
PA[7:0]		I	GPIO port A
PB[7:0]		I	GPIO port B
PD[0]/LEDFLSH	(Note)	I/O	GPIO port D
PD[5:1]		I/O	GPIO port D
PD[7:6]/SDQM[1:0]	(Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0]	(Note)	I	GPIO port E
PE[2]/CLKSEL	(Note)	I	GPIO port E

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

Table 16. Hardware Debug Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Table 17. LED Flasher Pin Assignments

Pin Mnemonic		I/O	Pin Description
PD[0]/LEDFLSH	(Note)	O	LED flasher driver

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

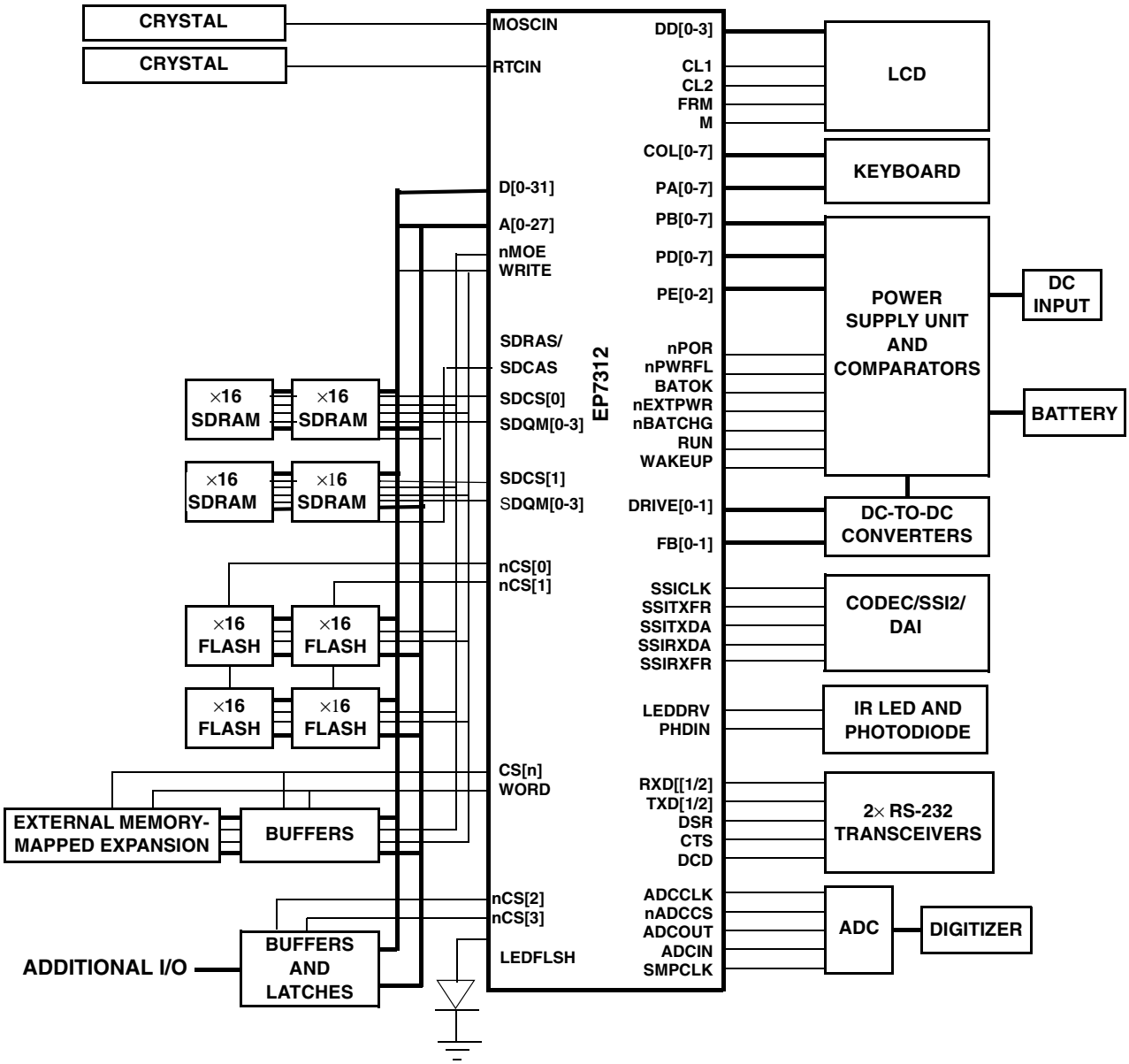

Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

SDRAM Burst Write Cycle

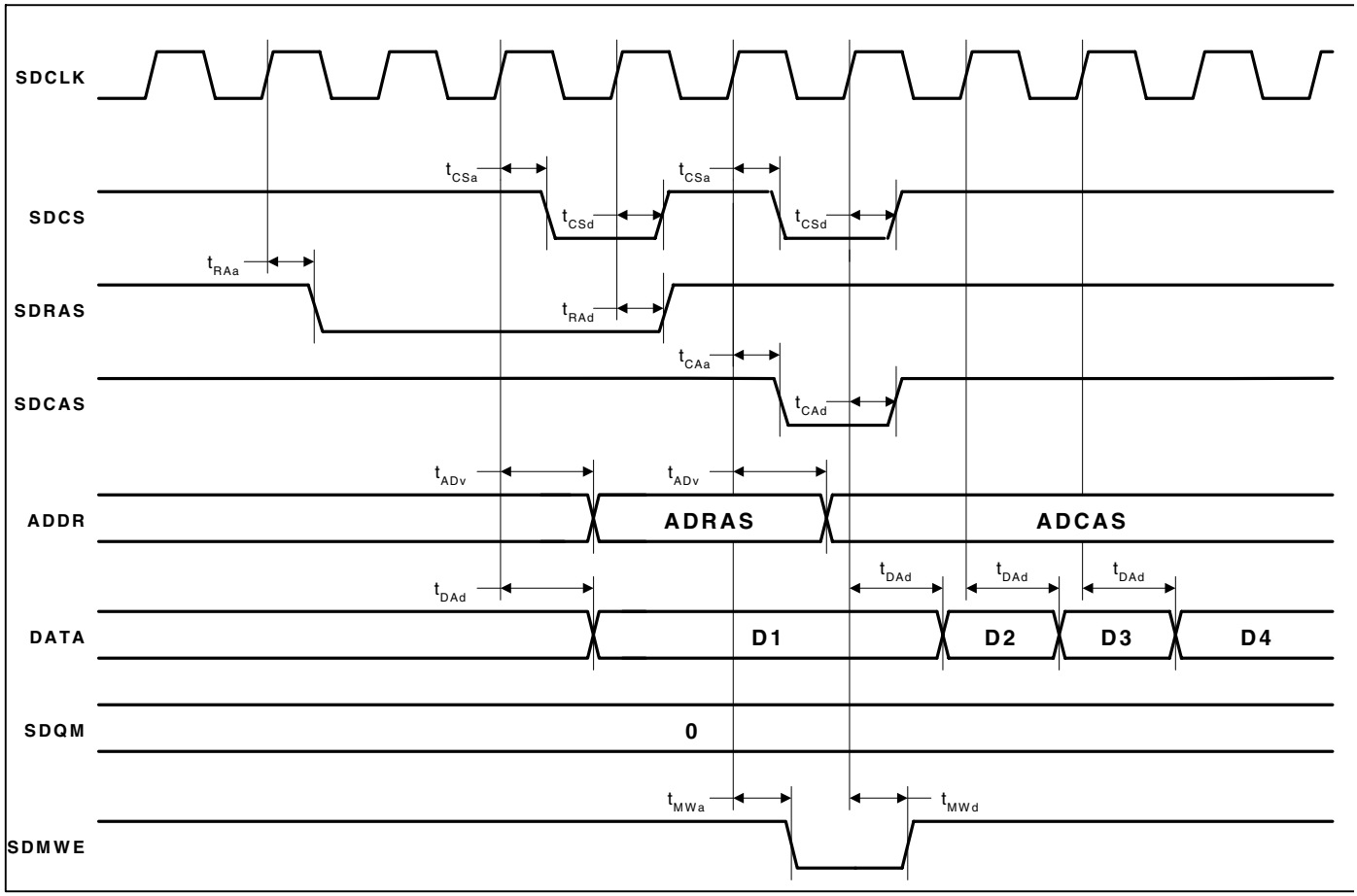

Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Write Cycle

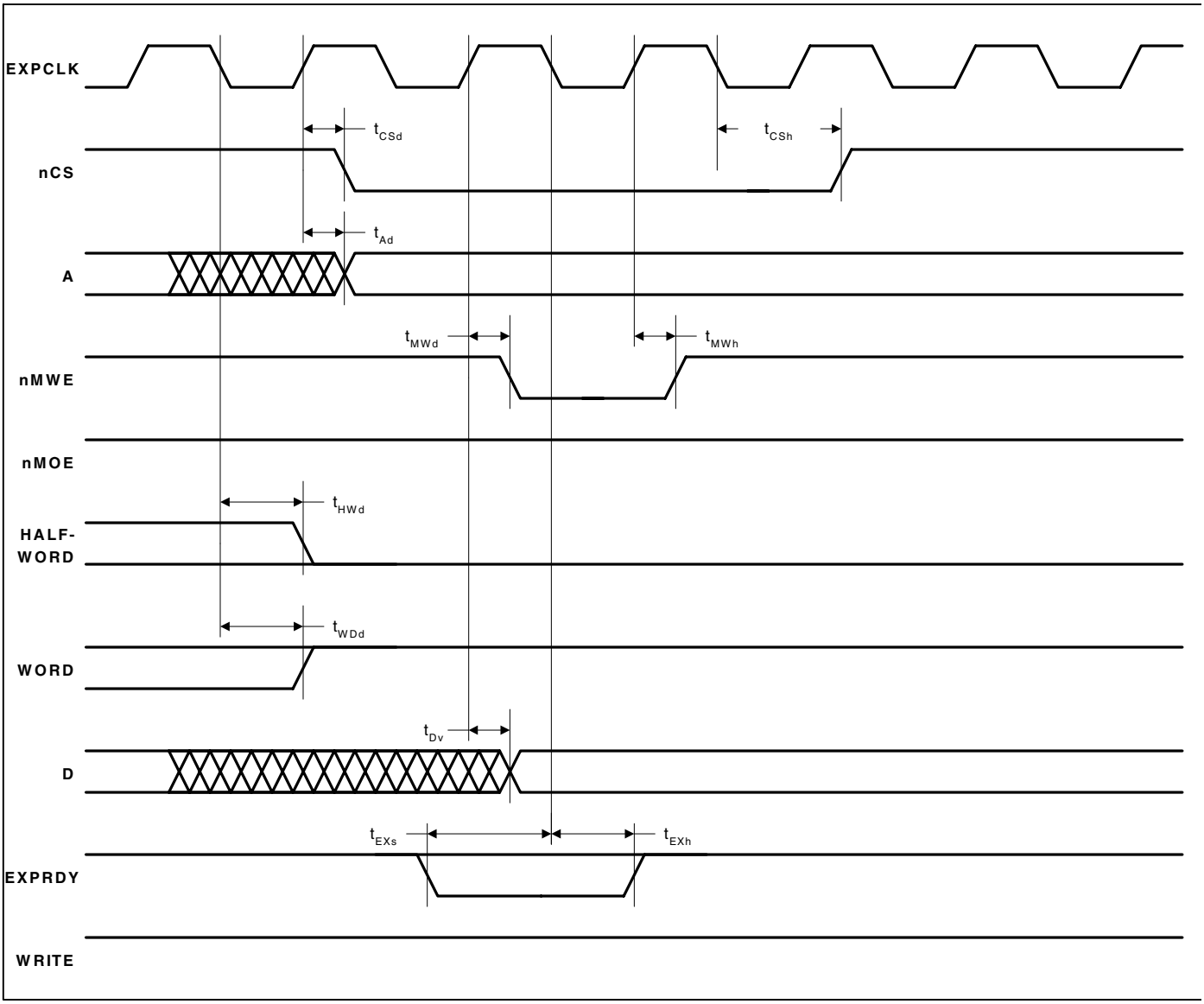

Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

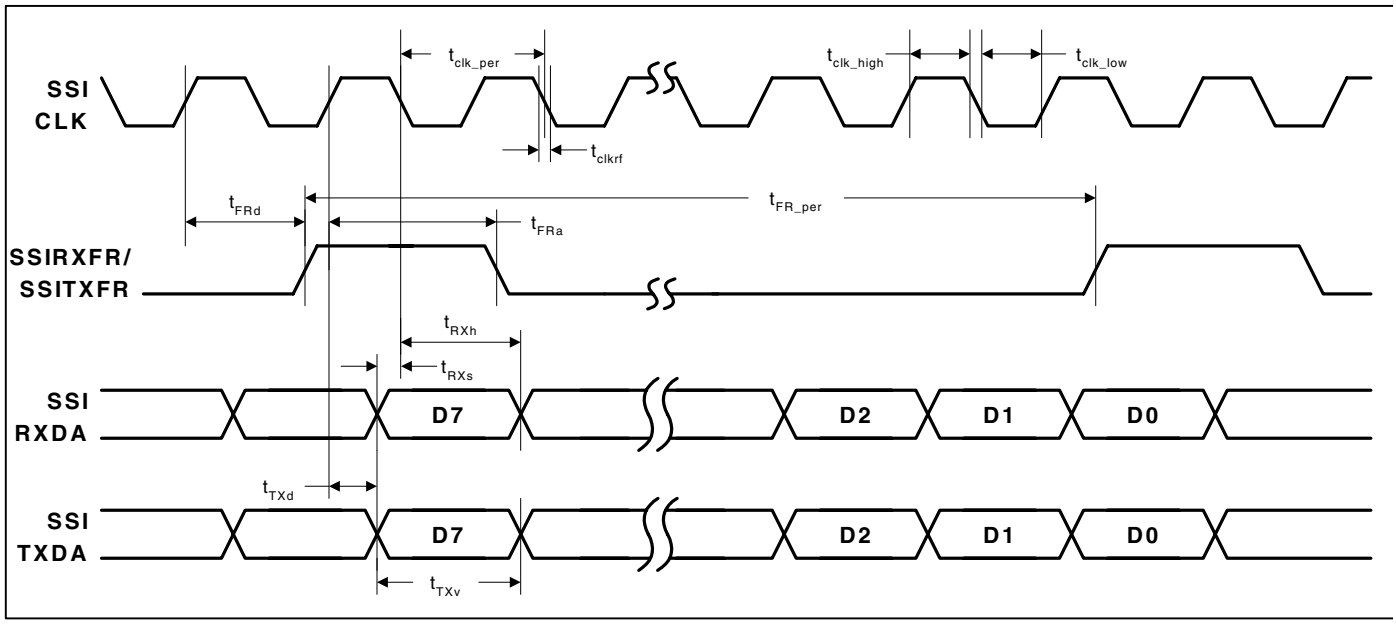

Figure 12. SSI2 Interface Timing Measurement

208-Pin LQFP Pin Diagram

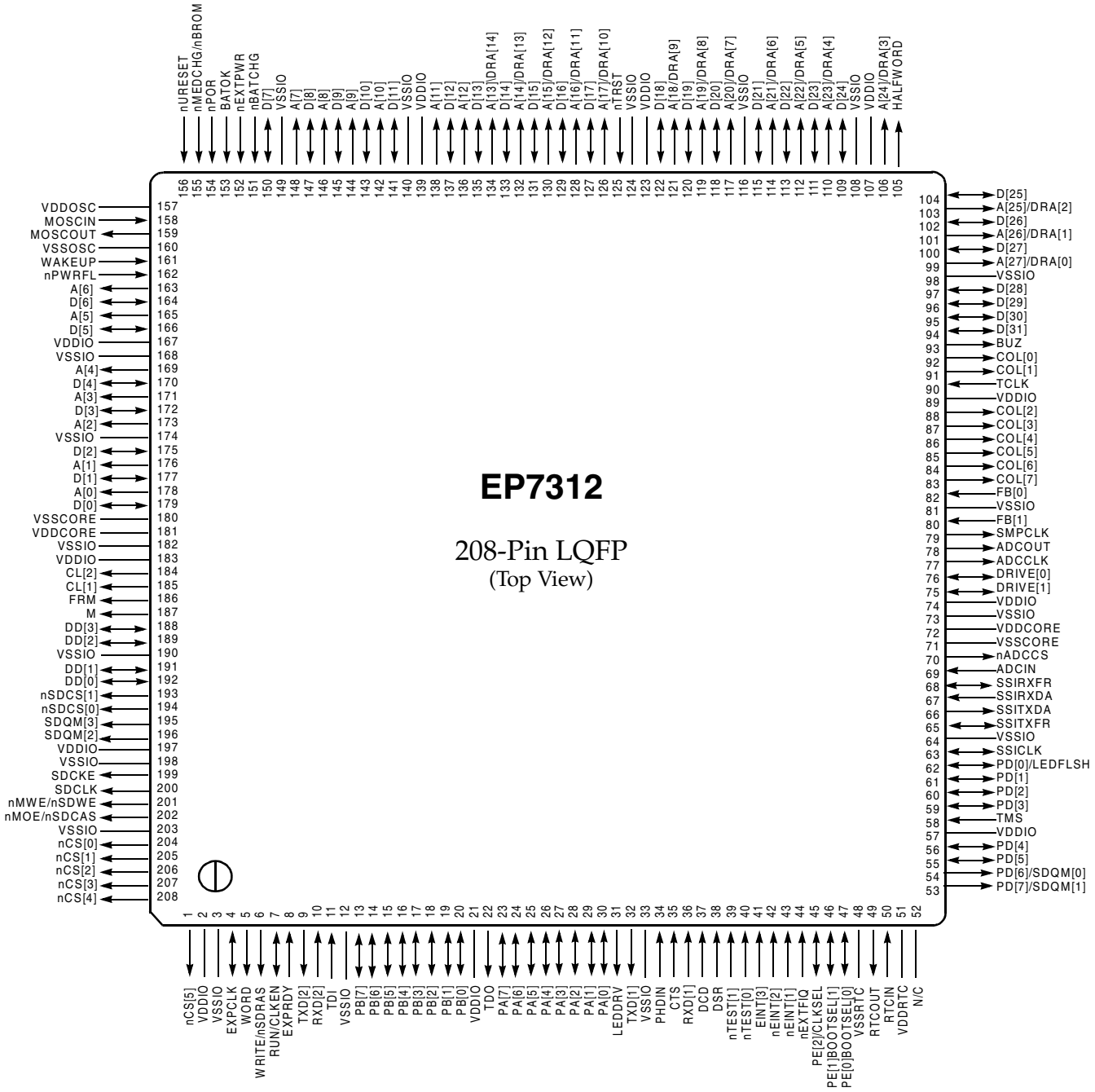

Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Note: 1. N/C should not be grounded but left as no connects.

208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
79	SMPCLK	1	Low	O	SSI1 ADC sample clock
80	FB[1]			I	PWM feedback input
81	VSSIO			Pad Gnd	I/O ground
82	FB[0]			I	PWM feedback input
83	COL[7]	1	High	O	Keyboard scanner column drive
84	COL[6]	1	High	O	Keyboard scanner column drive
85	COL[5]	1	High	O	Keyboard scanner column drive
86	COL[4]	1	High	O	Keyboard scanner column drive
87	COL[3]	1	High	O	Keyboard scanner column drive
88	COL[2]	1	High	O	Keyboard scanner column drive
89	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
90	TCLK			I	JTAG clock
91	COL[1]	1	High	O	Keyboard scanner column drive
92	COL[0]	1	High	O	Keyboard scanner column drive
93	BUZ	1	Low	O	Buzzer drive output
94	D[31]	1	Low	I/O	Data I/O
95	D[30]	1	Low	I/O	Data I/O
96	D[29]	1	Low	I/O	Data I/O
97	D[28]	1	Low	I/O	Data I/O
98	VSSIO			Pad Gnd	I/O ground
99	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
100	D[27]	1	Low	I/O	Data I/O
101	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
102	D[26]	1	Low	I/O	Data I/O
103	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
104	D[25]	1	Low	I/O	Data I/O
105	HALFWORD	1	Low	O	Halfword access select output
106	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
107	VDDIO		—	Pad Pwr	Digital I/O power, 3.3 V
108	VSSIO		—	Pad Gnd	I/O ground
109	D[24]	1	Low	I/O	Data I/O
110	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
111	D[23]	1	Low	I/O	Data I/O
112	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
113	D[22]	1	Low	I/O	Data I/O
114	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
115	D[21]	1	Low	I/O	Data I/O
116	VSSIO			Pad Gnd	I/O ground
117	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

204-Ball TFBGA Package Characteristics

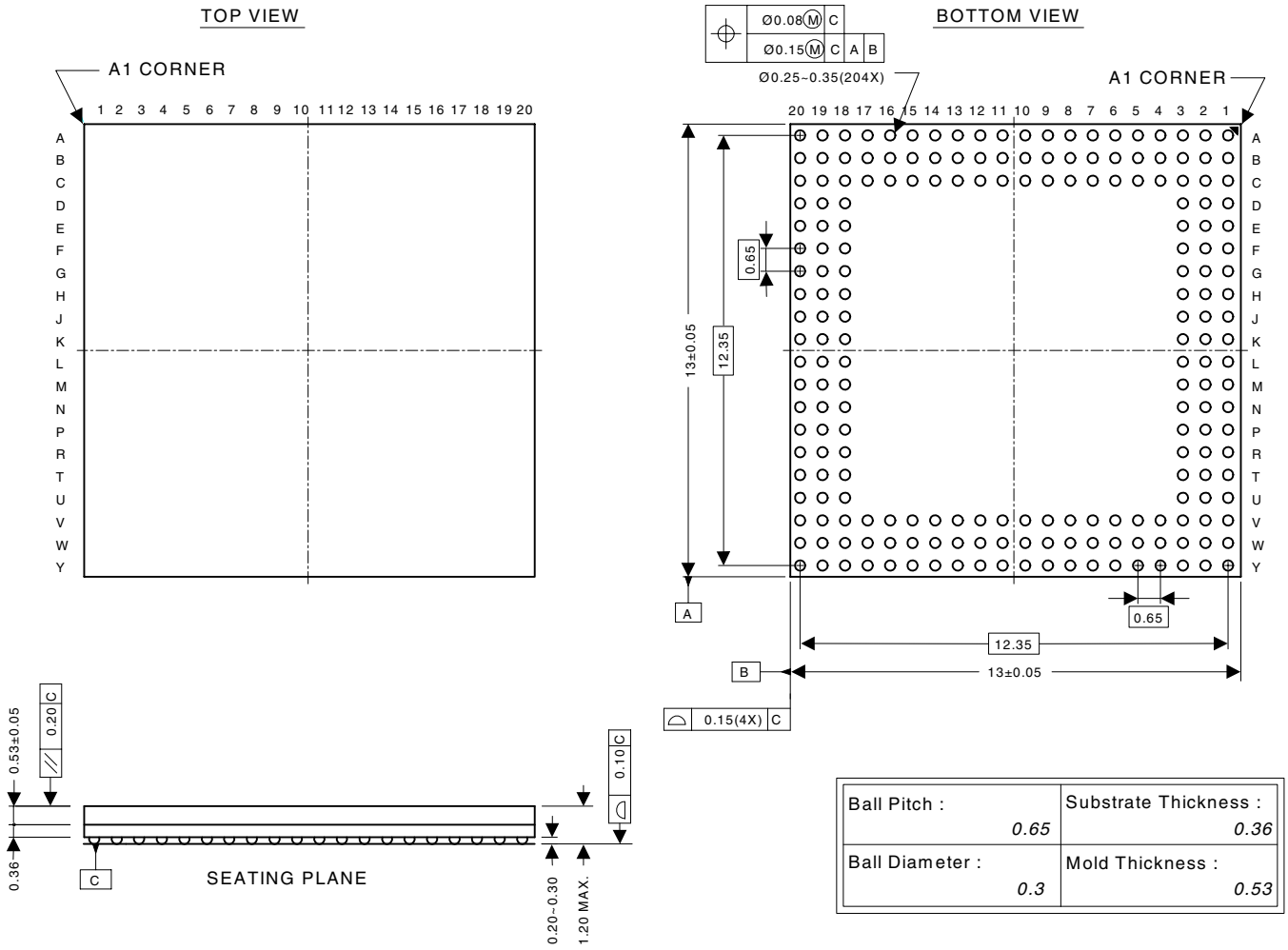

Figure 17. 204-Ball TFBGA Package

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A
J2	PA[5]	1	Input‡	I/O	GPIO port A
J3	PA[6]	1	Input‡	I/O	GPIO port A
J18	A[11]	1	Low	O	System byte address
J19	D[13]	1	Low	I/O	Data I/O
J20	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
K1	PA[1]	1	Input‡	I/O	GPIO port A
K2	PA[2]	1	Input‡	I/O	GPIO port A
K3	VDDIO			Pad power	Digital I/O power, 3.3V
K18	D[14]	1	Low	I/O	Data I/O
K19	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
K20	D[15]	1	Low	I/O	Data I/O
L1	TXD[1]	1	High	O	UART 1 transmit data out
L2	LEDDRV	1	Low	O	IR LED drive
L3	PA[3]	1	Input‡	I/O	GPIO port A
L18	VDDIO			Pad power	Digital I/O power, 3.3V
L19	D[16]	1	Low	I/O	Data I/O
L20	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
M1	RXD[1]			I	UART 1 receive data input
M2	CTS			I	UART 1 clear to send input
M3	PA[0]	1	Input‡	I/O	GPIO port A
M18	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
M19	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
M20	nTRST			I	JTAG async reset input
N1	DSR			I	UART 1 data set ready input
N2	nTEST[1]	With p/u*		I	Test mode select input
N3	PHDIN			I	Photodiode input

256-Ball PBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	SDCLK	SDQM[3]	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE/ nSDCAS	VDDIO	nSDCS[1]	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE/ nSDRAS	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE/ nSDWE	nSDCS[0]	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	SDQM[2]	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	SDCKE	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSCore	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]/ DRA[14]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]/ DRA[10]	A[16]/ DRA[11]	A[15]/ DRA[12]	A[14]/ DRA[13]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]/ DRA[5]	A[21]/ DRA[6]	VSSIO	A[18]/ DRA[9]	A[19]/ DRA[8]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]/ DRA[4]	VDDIO	A[20]/ DRA[7]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]/ DRA[0]	A[25]/ DRA[2]	VDDIO	A[24]\ DRA[3]	R
T	VDDRTC	PD[7]/ SDQM[1]	PD[6]/ SDQM[0]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]/ DRA[1]	D[25]	VSSIO	T

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
M4	PE[0]/BOOTSEL[0]	1	Input‡	I	GPIO port E / Boot mode select
M5	TMS	with p/u*		I	JTAG mode select
M6	VDDIO			Pad power	Digital I/O power, 3.3V
M7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	2	High / Low	I/O	PWM drive output
M9	FB[0]			I	PWM feedback input
M10	COL[0]	1	High	O	Keyboard scanner column drive
M11	D[27]	1	Low	I/O	Data I/O
M12	VSSIO			Pad ground	I/O ground
M13	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
M14	VDDIO			Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
M16	D[21]	1	Low	I/O	Data I/O
N1	nEXTFIQ			I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
N3	VSSIO			Pad ground	I/O ground
N4	VDDIO			Pad power	Digital I/O power, 3.3V
N5	PD[5]	1	Low	I/O	GPIO port D
N6	PD[2]	1	Low	I/O	GPIO port D
N7	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	1	Low	O	SSI1 ADC serial clock
N9	SMPCLK	1	Low	O	SSI1 ADC sample clock
N10	COL[2]	1	High	O	Keyboard scanner column drive
N11	D[29]	1	Low	I/O	Data I/O
N12	D[26]	1	Low	I/O	Data I/O
N13	HALFWORD	1	Low	O	Halfword access select output
N14	VSSIO			Pad ground	I/O ground
N15	D[22]	1	Low	I/O	Data I/O
N16	D[23]	1	Low	I/O	Data I/O
P1	VSSRTC			RTC ground	Real time clock ground
P2	RTCOUT			O	Real time clock oscillator output
P3	VSSIO			Pad ground	I/O ground
P4	VSSIO			Pad ground	I/O ground
P5	VDDIO			Pad power	Digital I/O power, 3.3V
P6	VSSIO			Pad ground	I/O ground
P7	VSSIO			Pad ground	I/O ground
P8	VDDIO			Pad power	Digital I/O power, 3.3V
P9	VSSIO			Pad ground	I/O ground
P10	VDDIO			Pad power	Digital I/O power, 3.3V
P11	VSSIO			Pad ground	I/O ground
P12	VSSIO			Pad ground	I/O ground
P13	VDDIO			Pad power	Digital I/O power
P14	VSSIO			Pad ground	I/O ground
P15	D[24]	1	Low	I/O	Data I/O
P16	VDDIO			Pad power	Digital I/O power, 3.3V
R1	RTCIN			I/O	Real time clock oscillator input
R2	VDDIO			Pad power	Digital I/O power, 3.3V

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	E1	G4	PB[4]	I/O	26
17	F1	F2	PB[3]	I/O	29
18	G2	H7	PB[2]	I/O	32
19	G1	G1	PB[1]	I/O	35
20	H3	H6	PB[0]	I/O	38
23	H1	H1	PA[7]	I/O	41
24	J3	H5	PA[6]	I/O	44
25	J2	H2	PA[5]	I/O	47
26	J1	H4	PA[4]	I/O	50
27	L3	J1	PA[3]	I/O	53
28	K2	J4	PA[2]	I/O	56
29	K1	J2	PA[1]	I/O	59
30	M3	J5	PA[0]	I/O	62
31	L2	K1	LEDDRV	O	65
32	L1	J6	TXD1	O	67
34	N3	K2	PHDIN	I	69
35	M2	J7	CTS	I	70
36	M1	L1	RXD1	I	71
37	P3	K4	DCD	I	72
38	N1	L2	DSR	I	73
39	N2	K5	nTEST1	I	74
40	R3	M1	nTEST0	I	75
41	P1	K6	EINT3	I	76
42	P2	M2	nEINT2	I	77
43	T3	L4	nEINT1	I	78
44	R1	N1	nEXTFIQ	I	79
45	R2	L5	PE[2]/CLKSEL	I/O	80
46	T1	N2	PE[1]/ BOOTSEL[1]	I/O	83
47	T2	M4	PE[0]/BOOTSEL0	I/O	86
53	V4	T2	PD[7]/SDQM[1]	I/O	89
54	W4	T3	PD[6/SDQM[0]]	I/O	92

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
55	Y4	N5	PD[5]	I/O	95
56	V5	R3	PD[4]	I/O	98
59	Y5	T4	PD[3]	I/O	101
60	V6	N6	PD[2]	I/O	104
61	W6	R4	PD[1]	I/O	107
62	Y6	L7	PD[0]/LEDFLSH	O	110
68	W8	T6	SSIRXFR	I/O	122
69	Y8	K8	ADCIN	I	125
70	V9	R6	nADCCS	O	126
75	W10	M8	DRIVE1	I/O	128
76	Y10	T8	DRIVE0	I/O	131
77	V11	N8	ADCCLK	O	134
78	W11	R8	ADCOUT	O	136
79	Y11	N9	SMPCLK	O	138
80	Y12	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	Y13	L9	COL6	O	144
85	W13	T10	COL5	O	146
86	V13	K9	COL4	O	148
87	Y14	R10	COL3	O	150
88	W14	N10	COL2	O	152
91	Y15	R11	COL1	O	154
92	W15	M10	COL0	O	156
93	V15	T12	BUZ	O	158
94	Y16	L10	D[31]	I/O	160
95	W16	R12	D[30]	I/O	163
96	V16	N11	D[29]	I/O	166
97	Y17	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	Y18	M11	D[27]	I/O	174
101	V17	T14	A[26]/DRA[1]	O	177
102	W18	N12	D[26]	I/O	179
103	Y19	R14	A[25]/DRA[2]	O	182
104	Y20	T15	D[25]	I/O	184
105	U18	N13	HALFWORD	O	187
106	V209	R16	A[24]/DRA[3]	O	189
109	U19	P15	D[24]	I/O	191

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
155	E18	E13	nMEDCHG/nBROM	I	283
156	B20	B16	nURESET	I	284
161	B16	B14	WAKEUP	I	285
162	A16	D11	nPWRFL	I	286
163	C15	A13	A[6]	O	287
164	B15	F10	D[6]	I/O	289
165	A15	B13	A[5]	O	292
166	C14	E10	D[5]	I/O	294
169	B14	B12	A[4]	O	297
170	A14	D10	D[4]	I/O	299
171	C13	A11	A[3]	O	302
172	B13	G9	D[3]	I/O	304
173	A13	B11	A[2]	O	307
175	C12	A10	D[2]	I/O	309
176	B12	F9	A[1]	O	312
177	A12	B10	D[1]	I/O	314
178	C11	E9	A[0]	O	317
179	B11	A9	D[0]	I/O	319
184	B10	D8	CL2	O	322
185	A10	B8	CL1	O	324
186	A9	E8	FRM	O	326
187	B9	A7	M	O	328
188	C9	F8	DD[3]	O	330
189	A8	B7	DD[2]	O	333
191	B8	A6	DD[1]	O	336
192	C8	G8	DD[0]	O	339
193	A7	B6	nSDCS[1]	O	342
194	B7	D7	nSDCS[0]	O	344
195	C7	A5	SDQM[3]	I/O	346
196	A6	E7	SDQM[2]	I/O	349
199	B6	F7	SDCKE	I/O	352
200	C6	A4	SDCLK	I/O	355
201	A5	D6	nMWE/nSDWE	O	358
202	B5	B4	nMOE/nSDCAS	O	360
204	C5	E6	nCS[0]	O	362
205	A4	A3	nCS[1]	O	364


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