Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	90MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cvz-90

FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Table of Contents

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:

http://www.cirrus.com/corporate/contacts/sales.cfm

64-Key Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7312. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state. The Keypad Interface has these features:

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Table 10 shows the Keypad Interface Pin Assignments.

Table 10. Keypad Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7312 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources. The Interrupt controller has these features:

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

Table 11 shows the interrupt controller pin assignments.

Table 11. Interrupt Controller Pin Assignments

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Real-Time Clock

The EP7312 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Table 12 shows the Real-Time Clock pin assignments.

Table 12. Real-Time Clock Pin Assignments

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

PLL and Clocking

The EP7312 processor and peripheral clocks have these features:

- Processor and peripheral clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz, and at 45 MHz when the processor is set to 90 MHz.

Table 13 shows the PLL and clocking pin assignments.

Table 13. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Pin Multiplexing

Table 18 shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the *EP7312 User's Manual* for more information).

Table 18. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 19 shows the pins that have been multiplexed in the EP7312.

Table 19. Pin Multiplexing

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @2.5 V[1] I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{IDLE} at 90 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	7 11	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

SDRAM Burst Write Cycle

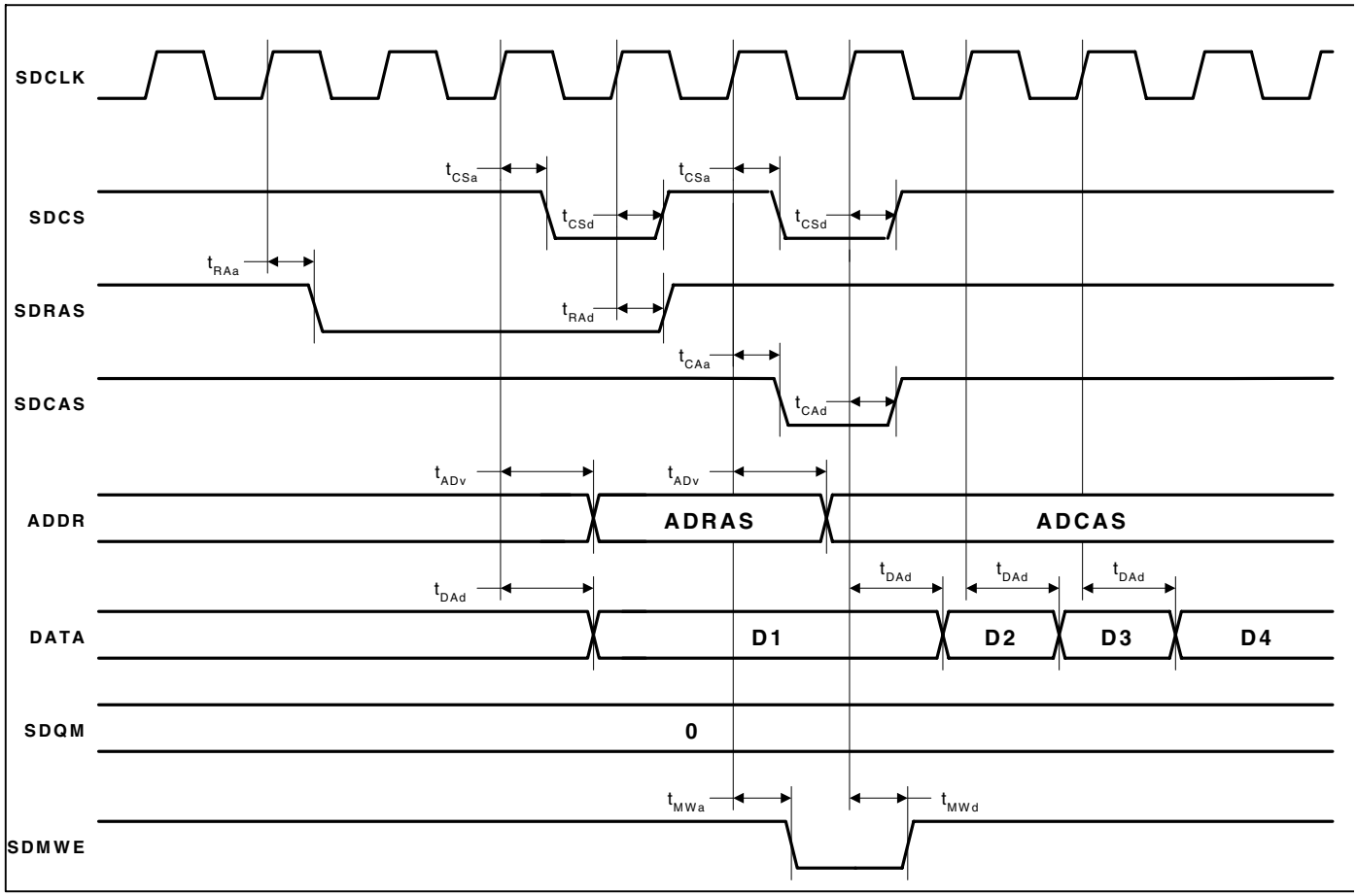

Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

SDRAM Refresh Cycle

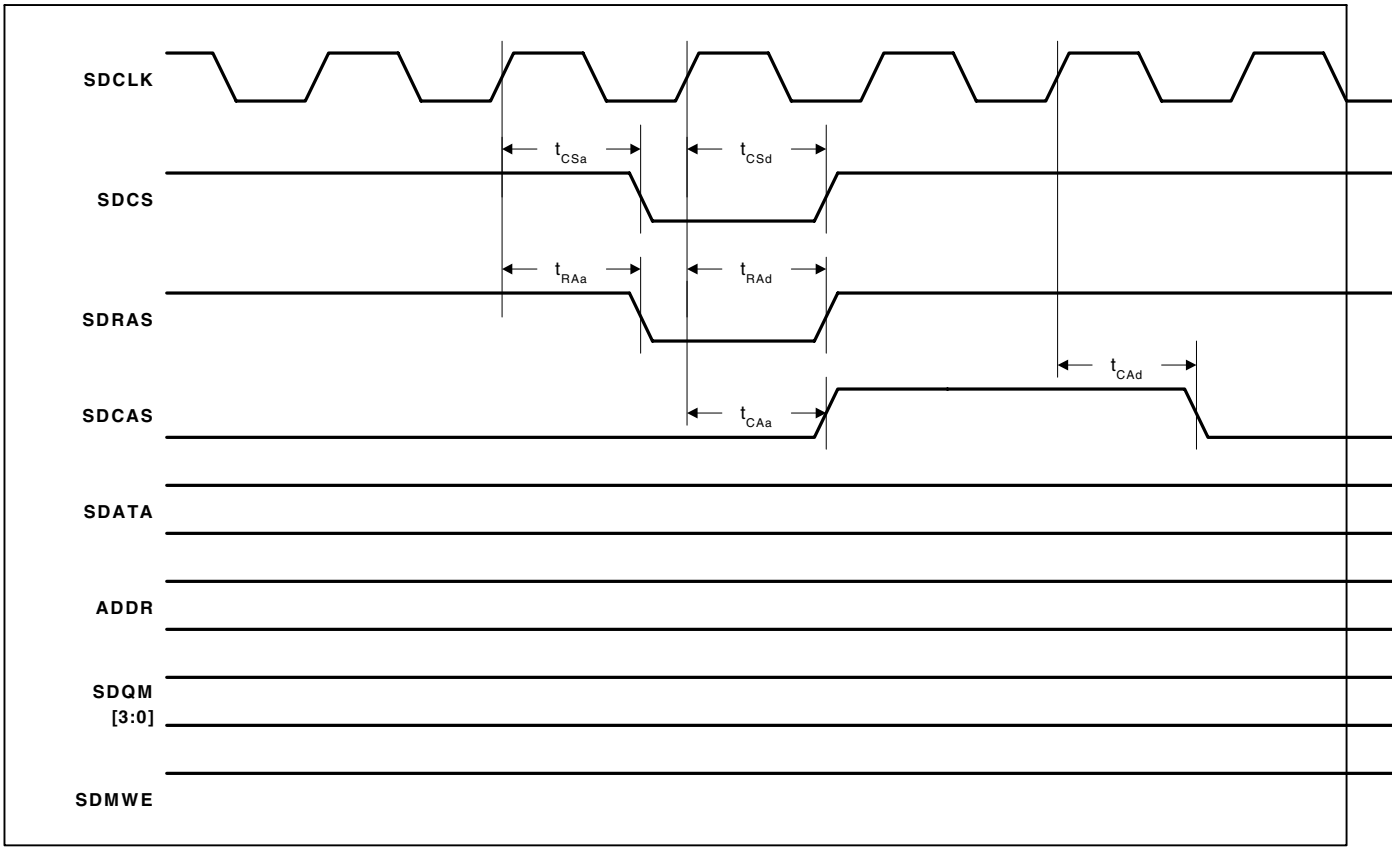

Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

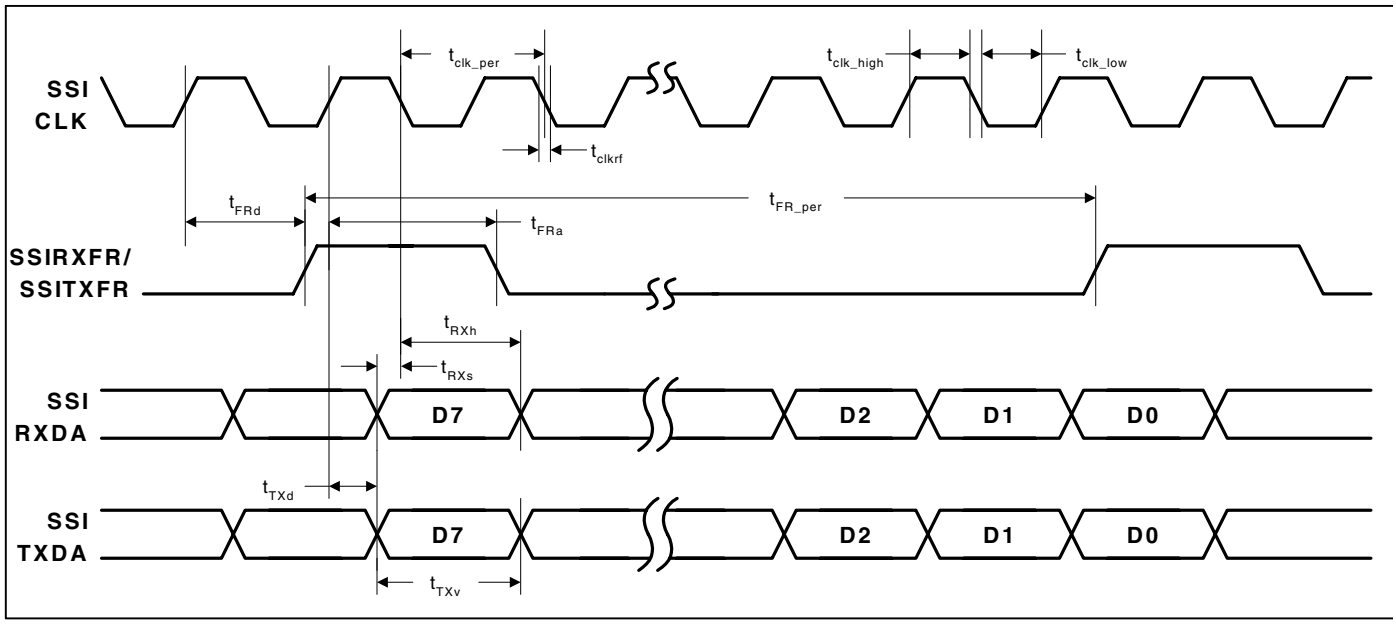

Figure 12. SSI2 Interface Timing Measurement

Packages

208-Pin LQFP Package Characteristics

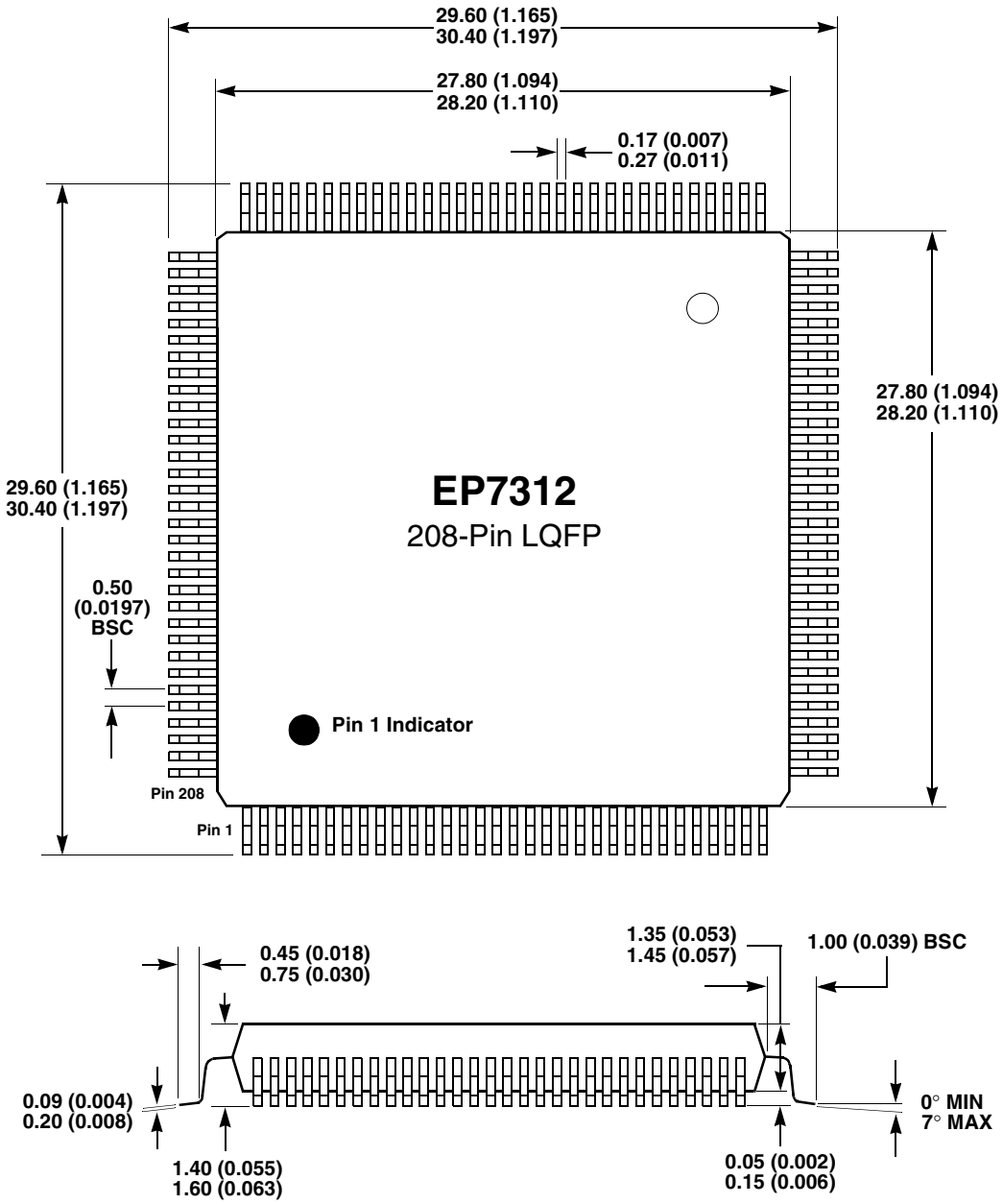

Figure 15. 208-Pin LQFP Package Outline Drawing

Note: 1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 16. For pin descriptions see the EP7312 User's Manual.

208-Pin LQFP Pin Diagram

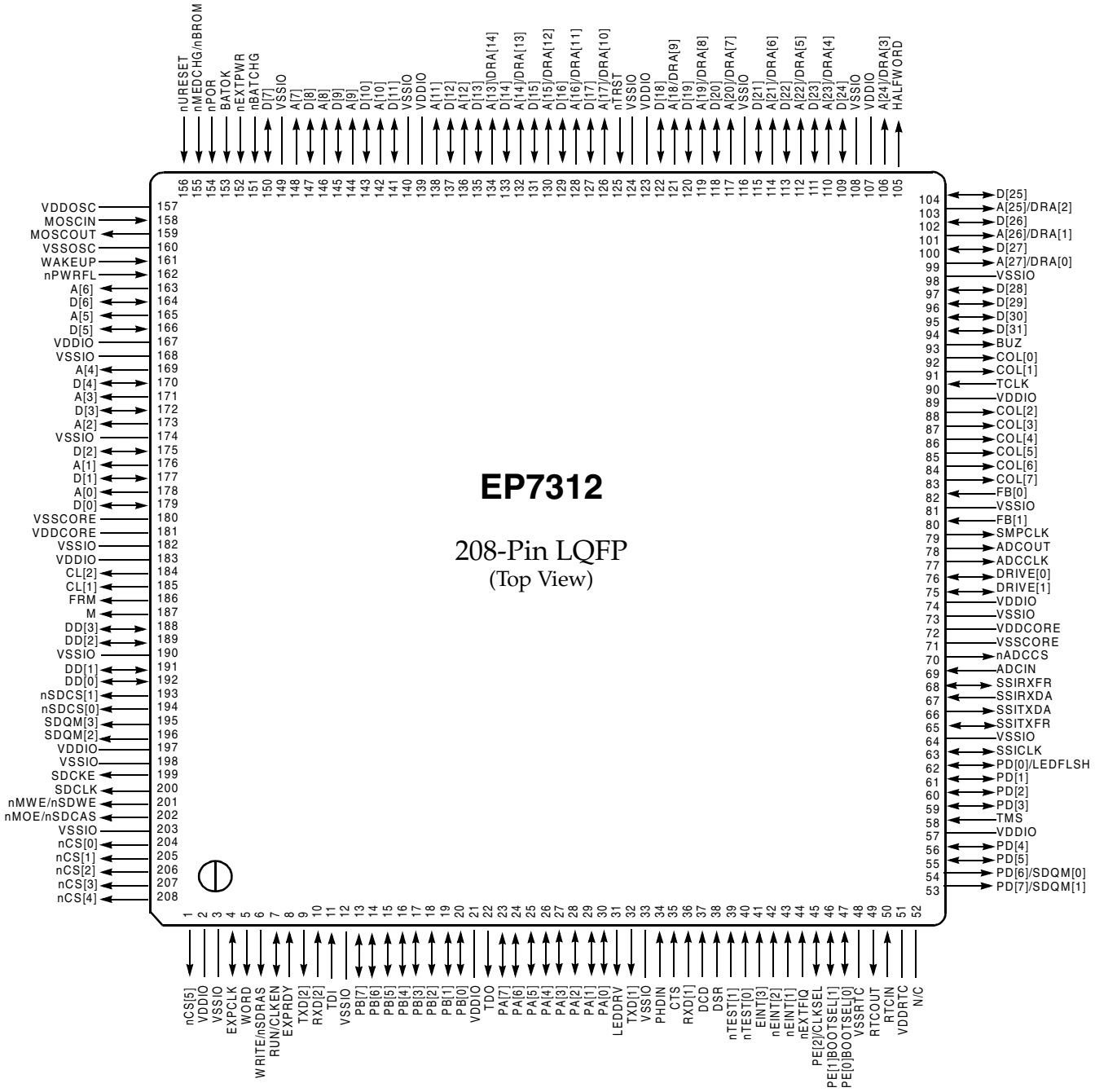

Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Note: 1. N/C should not be grounded but left as no connects.

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
38	DSR			I	UART 1 data set ready input
39	nTEST[1]	With p/u*		I	Test mode select input
40	nTEST[0]	With p/u*		I	Test mode select input
41	EINT[3]			I	External interrupt
42	nEINT[2]			I	External interrupt input
43	nEINT[1]			I	External interrupt input
44	nEXTFIQ			I	External fast interrupt input
45	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
46	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
47	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / Boot mode select
48	VSSRTC			RTC Gnd	Real time clock ground
49	RTCOUT			O	Real time clock oscillator output
50	RTCIN			I	Real time clock oscillator input
51	VDDRTC			RTC power	Real time clock power, 2.5 V
52	N/C				
53	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
54	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
55	PD[5]	1	Low	I/O	GPIO port D
56	PD[4]	1	Low	I/O	GPIO port D
57	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
58	TMS	with p/u*		I	JTAG mode select
59	PD[3]	1	Low	I/O	GPIO port D
60	PD[2]	1	Low	I/O	GPIO port D
61	PD[1]	1	Low	I/O	GPIO port D
62	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
63	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
64	VSSIO			Pad Gnd	I/O ground
65	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 serial clock
66	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
67	SSIRXDA			I	DAI/CODEC/SSI2 serial data input
68	SSIRXFR		Input‡	I/O	DAI/CODEC/SSI2 frame sync
69	ADCIN			I	SSI1 ADC serial input
70	nADCCS	1	High	O	SSI1 ADC chip select
71	VSSCORE			Core ground	Core ground
72	VDDCORE			Core Pwr	Core power, 2.5 V
73	VSSIO			Pad Gnd	I/O ground
74	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
75	DRIVE[1]	2	High / Low	I/O	PWM drive output
76	DRIVE[0]	2	High / Low	I/O	PWM drive output
77	ADCCLK	1	Low	O	SSI1 ADC serial clock
78	ADCOUT	1	Low	O	SSI1 ADC serial data output

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
79	SMPCLK	1	Low	O	SSI1 ADC sample clock
80	FB[1]			I	PWM feedback input
81	VSSIO			Pad Gnd	I/O ground
82	FB[0]			I	PWM feedback input
83	COL[7]	1	High	O	Keyboard scanner column drive
84	COL[6]	1	High	O	Keyboard scanner column drive
85	COL[5]	1	High	O	Keyboard scanner column drive
86	COL[4]	1	High	O	Keyboard scanner column drive
87	COL[3]	1	High	O	Keyboard scanner column drive
88	COL[2]	1	High	O	Keyboard scanner column drive
89	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
90	TCLK			I	JTAG clock
91	COL[1]	1	High	O	Keyboard scanner column drive
92	COL[0]	1	High	O	Keyboard scanner column drive
93	BUZ	1	Low	O	Buzzer drive output
94	D[31]	1	Low	I/O	Data I/O
95	D[30]	1	Low	I/O	Data I/O
96	D[29]	1	Low	I/O	Data I/O
97	D[28]	1	Low	I/O	Data I/O
98	VSSIO			Pad Gnd	I/O ground
99	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
100	D[27]	1	Low	I/O	Data I/O
101	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
102	D[26]	1	Low	I/O	Data I/O
103	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
104	D[25]	1	Low	I/O	Data I/O
105	HALFWORD	1	Low	O	Halfword access select output
106	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
107	VDDIO		—	Pad Pwr	Digital I/O power, 3.3 V
108	VSSIO		—	Pad Gnd	I/O ground
109	D[24]	1	Low	I/O	Data I/O
110	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
111	D[23]	1	Low	I/O	Data I/O
112	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
113	D[22]	1	Low	I/O	Data I/O
114	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
115	D[21]	1	Low	I/O	Data I/O
116	VSSIO			Pad Gnd	I/O ground
117	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
M4	PE[0]/BOOTSEL[0]	1	Input‡	I	GPIO port E / Boot mode select
M5	TMS	with p/u*		I	JTAG mode select
M6	VDDIO			Pad power	Digital I/O power, 3.3V
M7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	2	High / Low	I/O	PWM drive output
M9	FB[0]			I	PWM feedback input
M10	COL[0]	1	High	O	Keyboard scanner column drive
M11	D[27]	1	Low	I/O	Data I/O
M12	VSSIO			Pad ground	I/O ground
M13	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
M14	VDDIO			Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
M16	D[21]	1	Low	I/O	Data I/O
N1	nEXTFIQ			I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
N3	VSSIO			Pad ground	I/O ground
N4	VDDIO			Pad power	Digital I/O power, 3.3V
N5	PD[5]	1	Low	I/O	GPIO port D
N6	PD[2]	1	Low	I/O	GPIO port D
N7	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	1	Low	O	SSI1 ADC serial clock
N9	SMPCLK	1	Low	O	SSI1 ADC sample clock
N10	COL[2]	1	High	O	Keyboard scanner column drive
N11	D[29]	1	Low	I/O	Data I/O
N12	D[26]	1	Low	I/O	Data I/O
N13	HALFWORD	1	Low	O	Halfword access select output
N14	VSSIO			Pad ground	I/O ground
N15	D[22]	1	Low	I/O	Data I/O
N16	D[23]	1	Low	I/O	Data I/O
P1	VSSRTC			RTC ground	Real time clock ground
P2	RTCOUT			O	Real time clock oscillator output
P3	VSSIO			Pad ground	I/O ground
P4	VSSIO			Pad ground	I/O ground
P5	VDDIO			Pad power	Digital I/O power, 3.3V
P6	VSSIO			Pad ground	I/O ground
P7	VSSIO			Pad ground	I/O ground
P8	VDDIO			Pad power	Digital I/O power, 3.3V
P9	VSSIO			Pad ground	I/O ground
P10	VDDIO			Pad power	Digital I/O power, 3.3V
P11	VSSIO			Pad ground	I/O ground
P12	VSSIO			Pad ground	I/O ground
P13	VDDIO			Pad power	Digital I/O power
P14	VSSIO			Pad ground	I/O ground
P15	D[24]	1	Low	I/O	Data I/O
P16	VDDIO			Pad power	Digital I/O power, 3.3V
R1	RTCIN			I/O	Real time clock oscillator input
R2	VDDIO			Pad power	Digital I/O power, 3.3V

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	E1	G4	PB[4]	I/O	26
17	F1	F2	PB[3]	I/O	29
18	G2	H7	PB[2]	I/O	32
19	G1	G1	PB[1]	I/O	35
20	H3	H6	PB[0]	I/O	38
23	H1	H1	PA[7]	I/O	41
24	J3	H5	PA[6]	I/O	44
25	J2	H2	PA[5]	I/O	47
26	J1	H4	PA[4]	I/O	50
27	L3	J1	PA[3]	I/O	53
28	K2	J4	PA[2]	I/O	56
29	K1	J2	PA[1]	I/O	59
30	M3	J5	PA[0]	I/O	62
31	L2	K1	LEDDRV	O	65
32	L1	J6	TXD1	O	67
34	N3	K2	PHDIN	I	69
35	M2	J7	CTS	I	70
36	M1	L1	RXD1	I	71
37	P3	K4	DCD	I	72
38	N1	L2	DSR	I	73
39	N2	K5	nTEST1	I	74
40	R3	M1	nTEST0	I	75
41	P1	K6	EINT3	I	76
42	P2	M2	nEINT2	I	77
43	T3	L4	nEINT1	I	78
44	R1	N1	nEXTFIQ	I	79
45	R2	L5	PE[2]/CLKSEL	I/O	80
46	T1	N2	PE[1]/ BOOTSEL[1]	I/O	83
47	T2	M4	PE[0]/BOOTSEL0	I/O	86
53	V4	T2	PD[7]/SDQM[1]	I/O	89
54	W4	T3	PD[6/SDQM[0]]	I/O	92

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
206	B4	D5	nCS[2]	O	366
207	A3	B3	nCS[3]	O	368
208	C4	A2	nCS[4]	O	370

1) See EP7312 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase "h" appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, '11' designates a binary number). Numbers not indicated by an "h", 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the *EP7312 User's Manual*. The use of "TBD" indicates values that are "to be determined," "n/a" designates "not available," and "n/c" indicates a pin that is a "no connect."

Pin Description Conventions

Abbreviations used for signal directions are listed in Table 26.

Table 26. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output


CIRRUS LOGIC®