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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-cvz

FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:

http://www.cirrus.com/corporate/contacts/sales.cfm

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

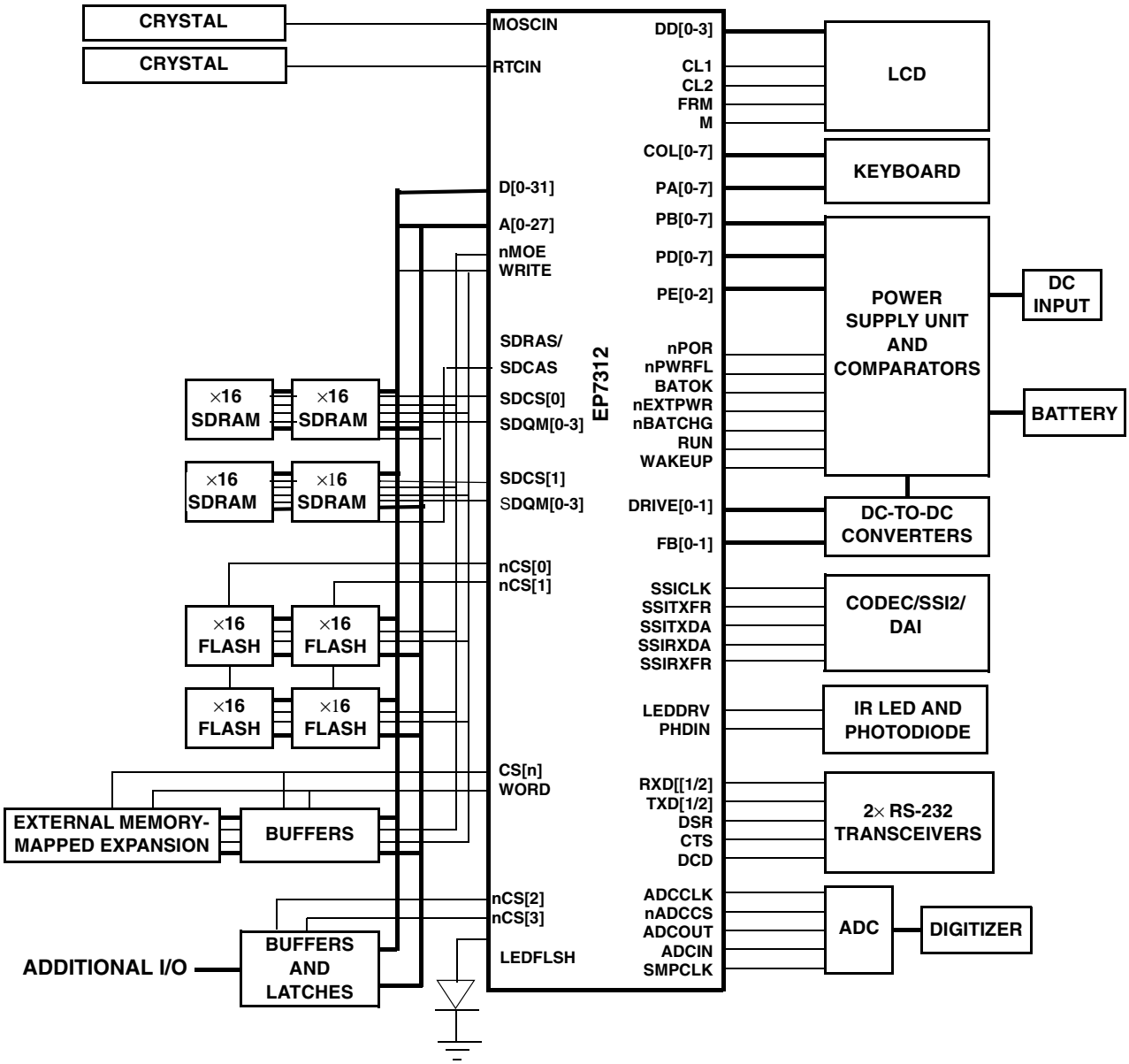


Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

SDRAM Interface

Figure 3 through Figure 6 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK rising edge to SDCS assert delay time	t_{CSa}	0	2	4	ns
SDCLK rising edge to SDCS deassert delay time	t_{CSd}	– 3	2	10	ns
SDCLK rising edge to SDRAS assert delay time	t_{RAa}	1	3	7	ns
SDCLK rising edge to SDRAS deassert delay time	t_{RAd}	– 3	1	10	ns
SDCLK rising edge to SDRAS invalid delay time	t_{RAnv}	2	4	7	ns
SDCLK rising edge to SDCAS assert delay time	t_{CAa}	– 2	2	5	ns
SDCLK rising edge to SDCAS deassert delay time	t_{CAd}	– 5	0	3	ns
SDCLK rising edge to ADDR transition time	t_{ADv}	– 3	1	5	ns
SDCLK rising edge to ADDR invalid delay time	t_{ADx}	– 2	2	5	ns
SDCLK rising edge to SDMWE assert delay time	t_{MWa}	– 2	1	5	ns
SDCLK rising edge to SDMWE deassert delay time	t_{MWd}	– 4	0	4	ns
DATA transition to SDCLK rising edge time	t_{DAs}	-	-	2	ns
SDCLK rising edge to DATA transition hold time	t_{DAh}	-	-	1	ns
SDCLK rising edge to DATA transition delay time	t_{DAd}	0	-	15	ns

SDRAM Burst Read Cycle

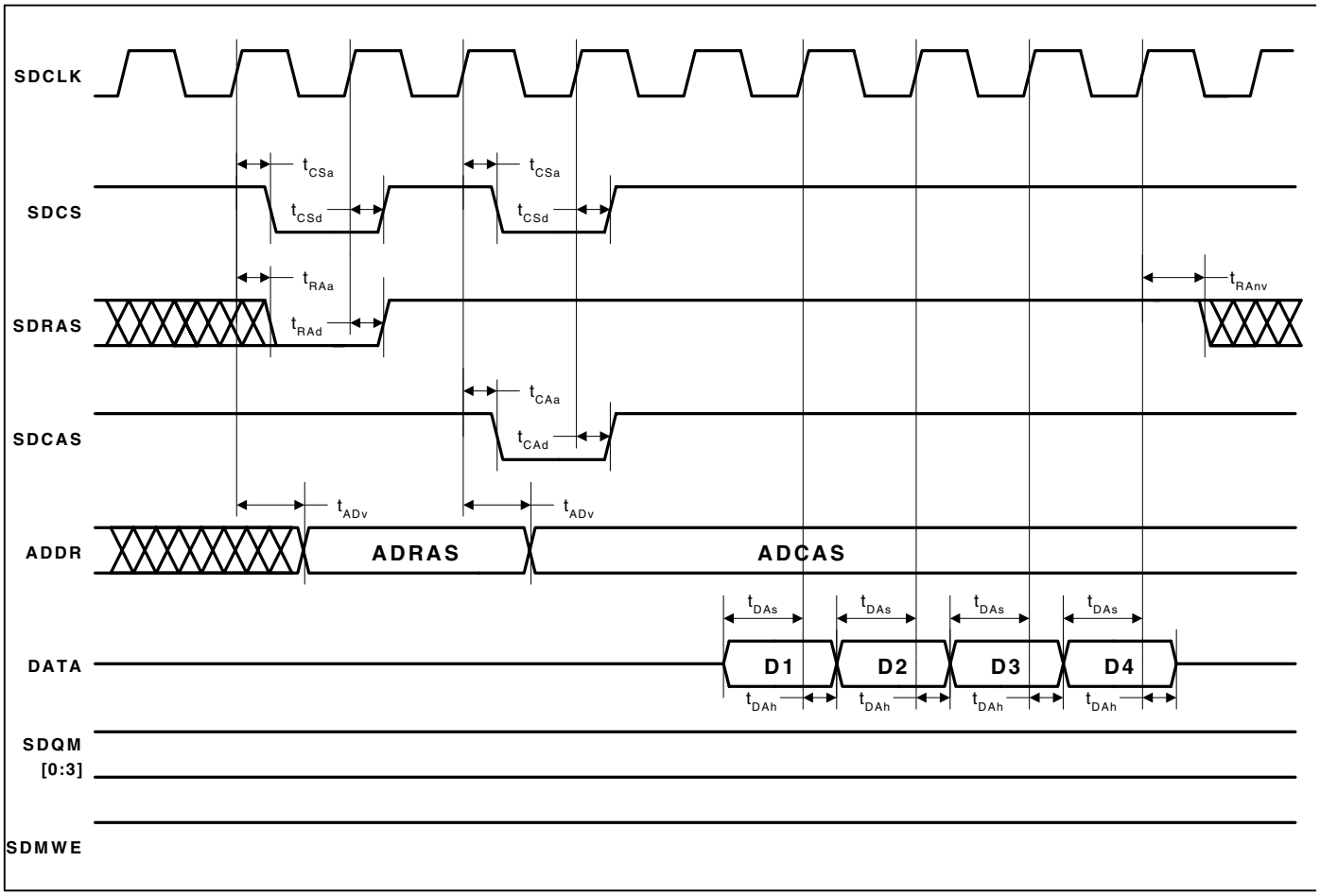


Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal.

SDRAM Refresh Cycle

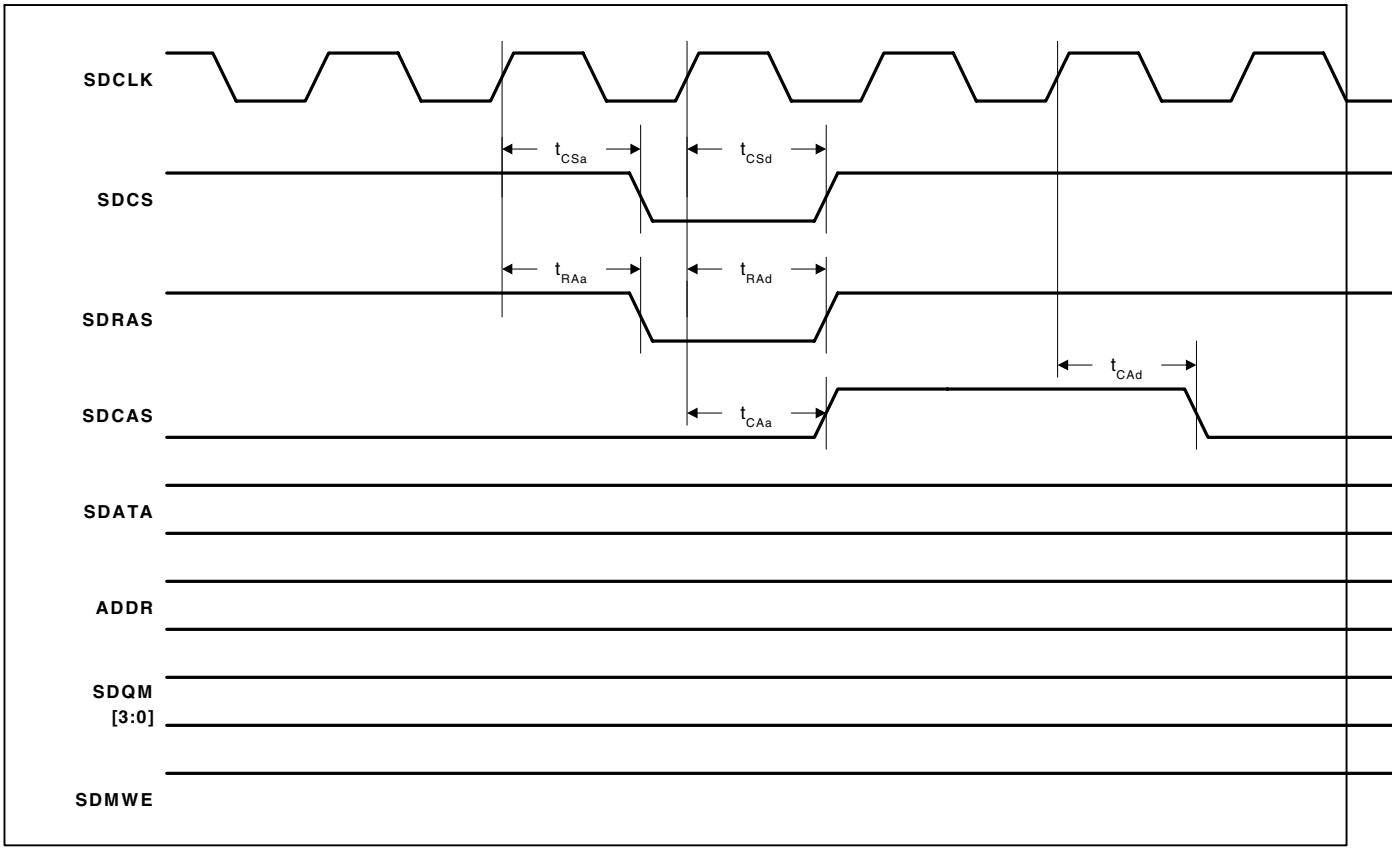


Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Write Cycle

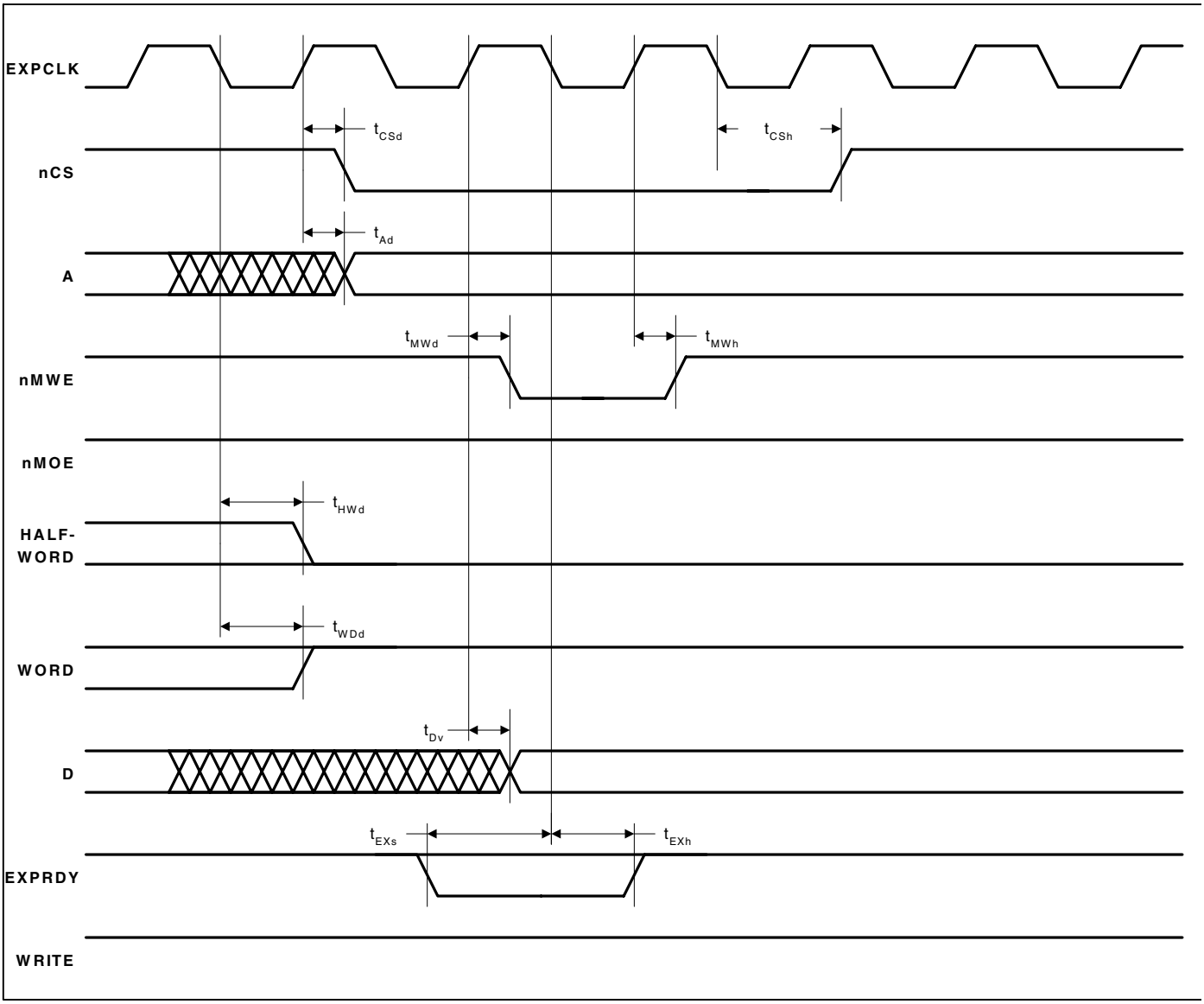


Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

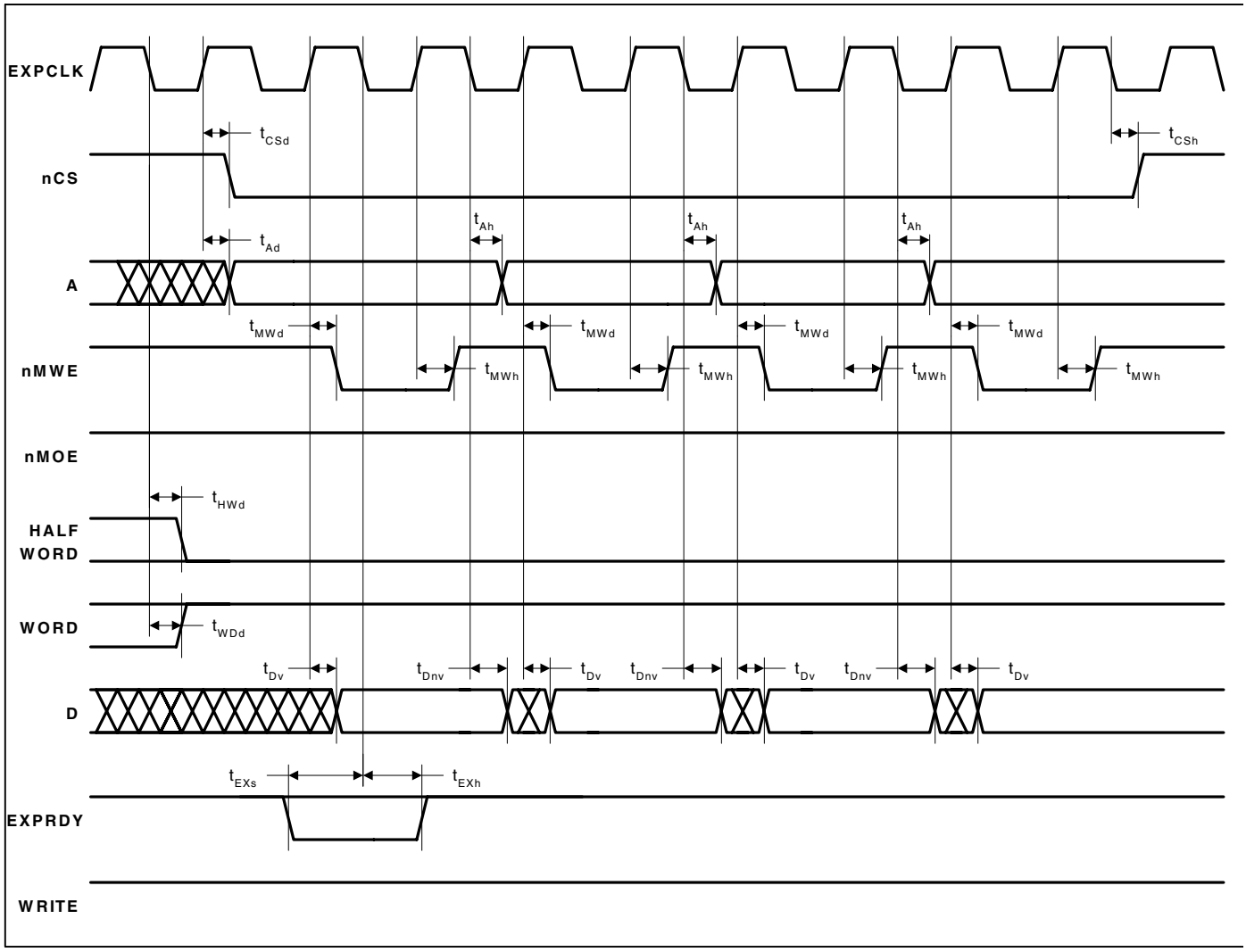


Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

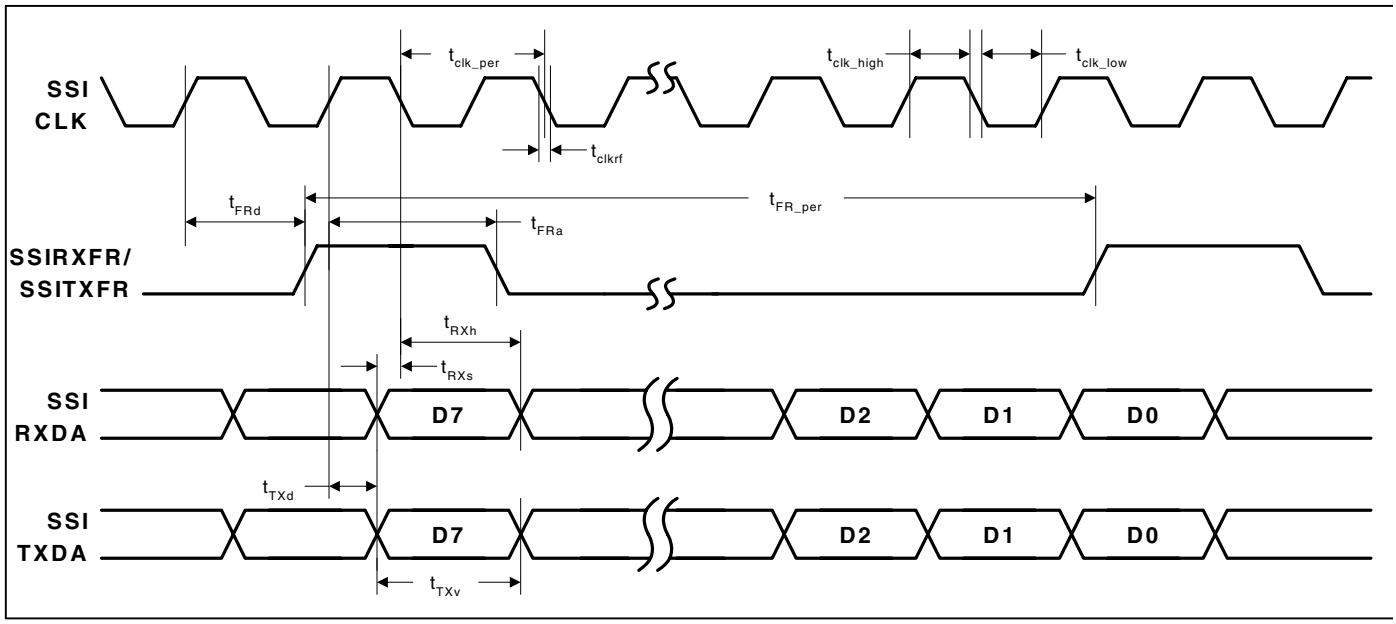


Figure 12. SSI2 Interface Timing Measurement

208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
38	DSR			I	UART 1 data set ready input
39	nTEST[1]	With p/u*		I	Test mode select input
40	nTEST[0]	With p/u*		I	Test mode select input
41	EINT[3]			I	External interrupt
42	nEINT[2]			I	External interrupt input
43	nEINT[1]			I	External interrupt input
44	nEXTFIQ			I	External fast interrupt input
45	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
46	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
47	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / Boot mode select
48	VSSRTC			RTC Gnd	Real time clock ground
49	RTCOUT			O	Real time clock oscillator output
50	RTCIN			I	Real time clock oscillator input
51	VDDRTC			RTC power	Real time clock power, 2.5 V
52	N/C				
53	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
54	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
55	PD[5]	1	Low	I/O	GPIO port D
56	PD[4]	1	Low	I/O	GPIO port D
57	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
58	TMS	with p/u*		I	JTAG mode select
59	PD[3]	1	Low	I/O	GPIO port D
60	PD[2]	1	Low	I/O	GPIO port D
61	PD[1]	1	Low	I/O	GPIO port D
62	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
63	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
64	VSSIO			Pad Gnd	I/O ground
65	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 serial clock
66	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
67	SSIRXDA			I	DAI/CODEC/SSI2 serial data input
68	SSIRXFR		Input‡	I/O	DAI/CODEC/SSI2 frame sync
69	ADCIN			I	SSI1 ADC serial input
70	nADCCS	1	High	O	SSI1 ADC chip select
71	VSSCORE			Core ground	Core ground
72	VDDCORE			Core Pwr	Core power, 2.5 V
73	VSSIO			Pad Gnd	I/O ground
74	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
75	DRIVE[1]	2	High / Low	I/O	PWM drive output
76	DRIVE[0]	2	High / Low	I/O	PWM drive output
77	ADCCLK	1	Low	O	SSI1 ADC serial clock
78	ADCOUT	1	Low	O	SSI1 ADC serial data output

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

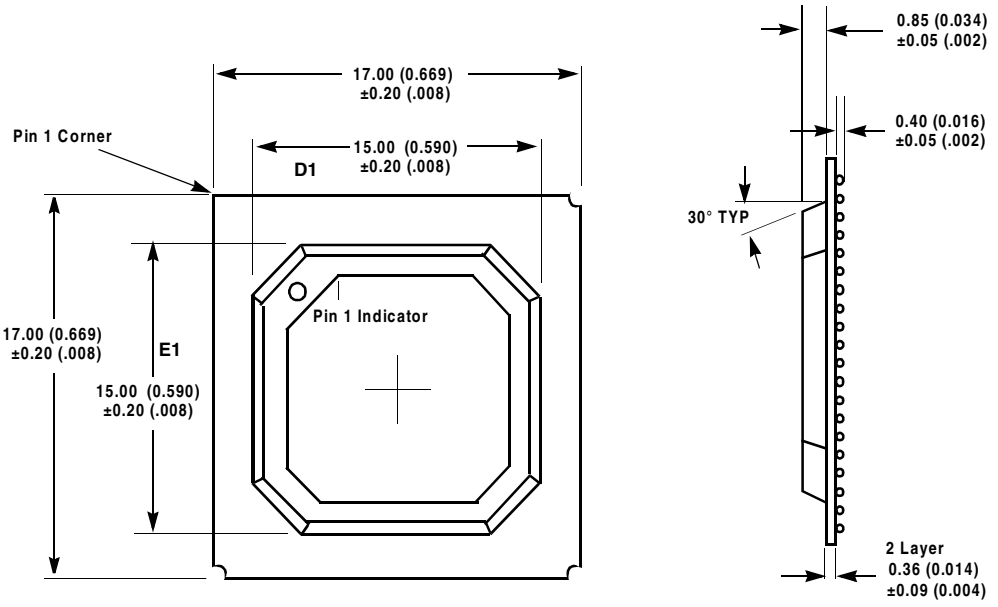
Pin No.	Signal	Strength†	Reset State	Type	Description
79	SMPCLK	1	Low	O	SSI1 ADC sample clock
80	FB[1]			I	PWM feedback input
81	VSSIO			Pad Gnd	I/O ground
82	FB[0]			I	PWM feedback input
83	COL[7]	1	High	O	Keyboard scanner column drive
84	COL[6]	1	High	O	Keyboard scanner column drive
85	COL[5]	1	High	O	Keyboard scanner column drive
86	COL[4]	1	High	O	Keyboard scanner column drive
87	COL[3]	1	High	O	Keyboard scanner column drive
88	COL[2]	1	High	O	Keyboard scanner column drive
89	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
90	TCLK			I	JTAG clock
91	COL[1]	1	High	O	Keyboard scanner column drive
92	COL[0]	1	High	O	Keyboard scanner column drive
93	BUZ	1	Low	O	Buzzer drive output
94	D[31]	1	Low	I/O	Data I/O
95	D[30]	1	Low	I/O	Data I/O
96	D[29]	1	Low	I/O	Data I/O
97	D[28]	1	Low	I/O	Data I/O
98	VSSIO			Pad Gnd	I/O ground
99	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
100	D[27]	1	Low	I/O	Data I/O
101	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
102	D[26]	1	Low	I/O	Data I/O
103	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
104	D[25]	1	Low	I/O	Data I/O
105	HALFWORD	1	Low	O	Halfword access select output
106	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
107	VDDIO		—	Pad Pwr	Digital I/O power, 3.3 V
108	VSSIO		—	Pad Gnd	I/O ground
109	D[24]	1	Low	I/O	Data I/O
110	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
111	D[23]	1	Low	I/O	Data I/O
112	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
113	D[22]	1	Low	I/O	Data I/O
114	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
115	D[21]	1	Low	I/O	Data I/O
116	VSSIO			Pad Gnd	I/O ground
117	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

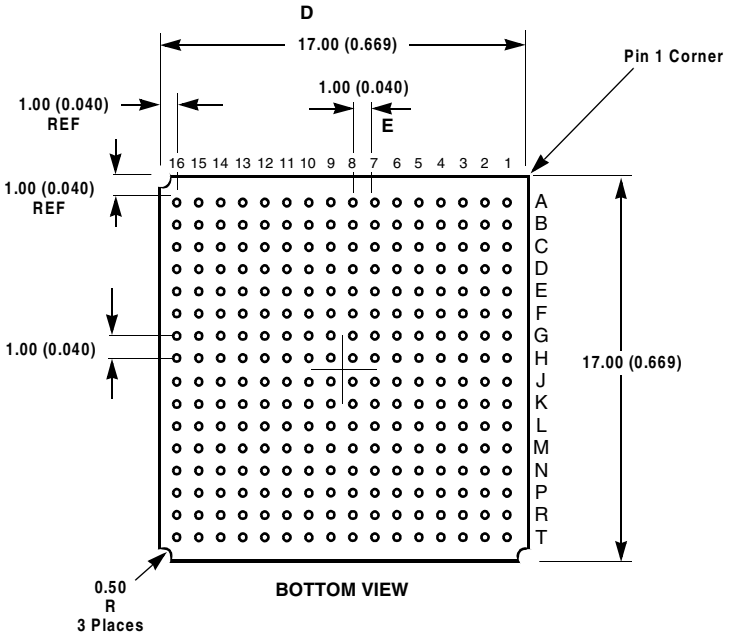
Pin No.	Signal	Strength†	Reset State	Type	Description
161	WAKEUP	Schmitt		I	System wake up input
162	nPWRFL			I	Power fail sense input
163	A[6]	1	Low	O	System byte address
164	D[6]	1	Low	I/O	Data I/O
165	A[5]	1	Low	Out	System byte address
166	D[5]	1	Low	I/O	Data I/O
167	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
168	VSSIO			Pad Gnd	I/O ground
169	A[4]	1	Low	O	System byte address
170	D[4]	1	Low	I/O	Data I/O
171	A[3]	2	Low	O	System byte address
172	D[3]	1	Low	I/O	Data I/O
173	A[2]	2	Low	O	System byte address
174	VSSIO			Pad Gnd	I/O ground
175	D[2]	1	Low	I/O	Data I/O
176	A[1]	2	Low	O	System byte address
177	D[1]	1	Low	I/O	Data I/O
178	A[0]	2	Low	O	System byte address
179	D[0]	1	Low	I/O	Data I/O
180	VSSCORE			Core ground	Core ground
181	VDDCORE			Core Pwr	Core power, 2.5 V
182	VSSIO			Pad ground	I/O ground
183	VDDIO			Pad Power	Digital I/O power, 3.3 V
184	CL[2]	1	Low	O	LCD pixel clock out
185	CL[1]	1	Low	O	LCD line clock
186	FRM	1	Low	O	LCD frame synchronization pulse
187	M	1	Low	O	LCD AC bias drive
188	DD[3]	1	Low	I/O	LCD serial display data
189	DD[2]	1	Low	I/O	LCD serial display data
190	VSSIO			Pad Gnd	I/O ground
191	DD[1]	1	Low	I/O	LCD serial display data
192	DD[0]	1	Low	I/O	LCD serial display data
193	nSDCS[1]	1	High	O	SDRAM chip select 1
194	nSDCS[0]	1	High	O	SDRAM chip select 0
195	SDQM[3]	2	Low	I/O	SDRAM byte lane mask
196	SDQM[2]	2	Low	I/O	SDRAM byte lane mask
197	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
198	VSSIO			Pad Gnd	I/O ground
199	SDCKE	2	Low	I/O	SDRAM clock enable output
200	SDCLK	2	Low	I/O	SDRAM clock out
201	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
202	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
203	VSSIO			Pad Gnd	I/O ground
204	nCS[0]	1	High	O	Chip select 0
205	nCS[1]	1	High	O	Chip select 1

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output



TOP VIEW **SIDE VIEW**



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	E1	G4	PB[4]	I/O	26
17	F1	F2	PB[3]	I/O	29
18	G2	H7	PB[2]	I/O	32
19	G1	G1	PB[1]	I/O	35
20	H3	H6	PB[0]	I/O	38
23	H1	H1	PA[7]	I/O	41
24	J3	H5	PA[6]	I/O	44
25	J2	H2	PA[5]	I/O	47
26	J1	H4	PA[4]	I/O	50
27	L3	J1	PA[3]	I/O	53
28	K2	J4	PA[2]	I/O	56
29	K1	J2	PA[1]	I/O	59
30	M3	J5	PA[0]	I/O	62
31	L2	K1	LEDDRV	O	65
32	L1	J6	TXD1	O	67
34	N3	K2	PHDIN	I	69
35	M2	J7	CTS	I	70
36	M1	L1	RXD1	I	71
37	P3	K4	DCD	I	72
38	N1	L2	DSR	I	73
39	N2	K5	nTEST1	I	74
40	R3	M1	nTEST0	I	75
41	P1	K6	EINT3	I	76
42	P2	M2	nEINT2	I	77
43	T3	L4	nEINT1	I	78
44	R1	N1	nEXTFIQ	I	79
45	R2	L5	PE[2]/CLKSEL	I/O	80
46	T1	N2	PE[1]/ BOOTSEL[1]	I/O	83
47	T2	M4	PE[0]/BOOTSEL0	I/O	86
53	V4	T2	PD[7]/SDQM[1]	I/O	89
54	W4	T3	PD[6/SDQM[0]]	I/O	92

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase "h" appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, '11' designates a binary number). Numbers not indicated by an "h", 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the *EP7312 User's Manual*. The use of "TBD" indicates values that are "to be determined," "n/a" designates "not available," and "n/c" indicates a pin that is a "no connect."

Pin Description Conventions

Abbreviations used for signal directions are listed in Table 26.

Table 26. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output

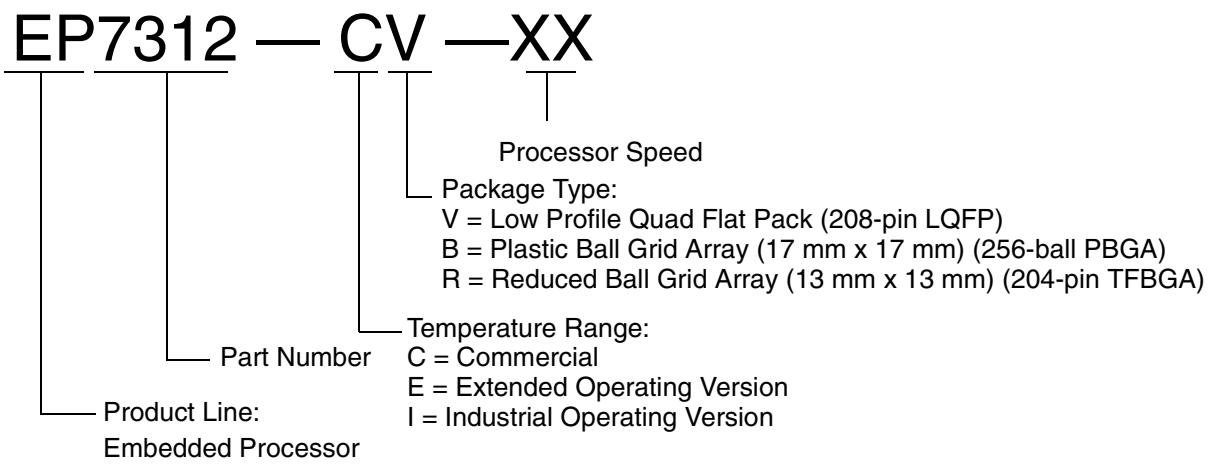
Ordering Information

Here is the list of EP7312 parts that are available:

- EP7312-CV
- EP7312-IV
- EP7312-CB
- EP7312-CR
- EP7312-CV-90
- EP7312-CB-90
- EP7312-CR-90
- EP7312-IB
- EP7312-IR
- EP7312-IV-90
- EP7312-IB-90
- EP7312-IR-90

Ordering Information Legend

Here is the legend for understanding the ordering information on page 1.



Note: Go to the Cirrus Logic Internet site at http://cirrus.com/corporate/contacts to find contact information for your local sales representative.