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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-ib

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

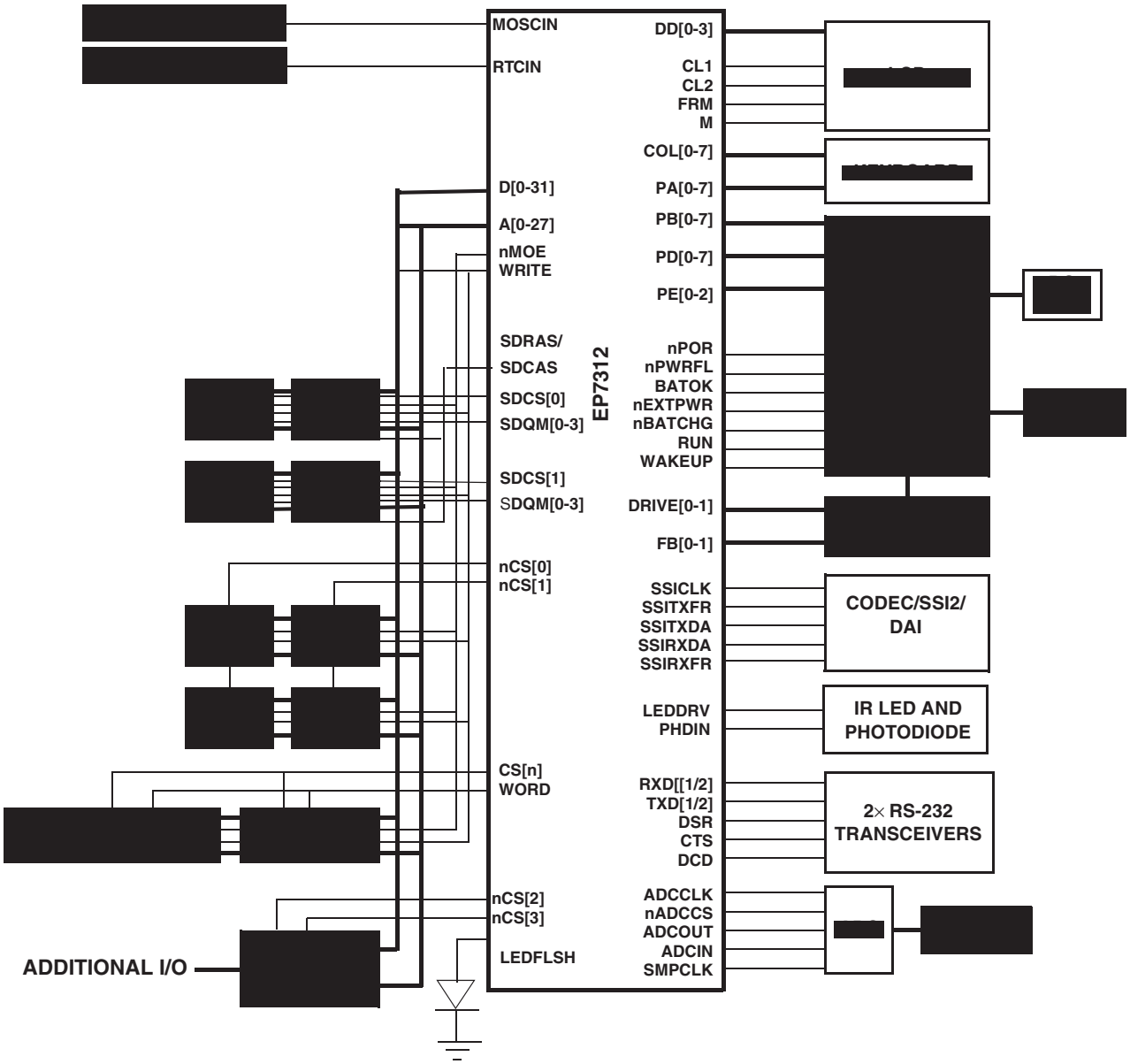

Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

Pin Multiplexing

Table 18 shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the EP7312 User's Manual for more information).

Table 18. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 19 shows the pins that have been multiplexed in the EP7312.

Table 19. Pin Multiplexing

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

Table 14. DC-to-DC Converter Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

Table 15. General Purpose Input/Output Pin Assignments

Pin Mnemonic		I/O	Pin Description
PA[7:0]		I	GPIO port A
PB[7:0]		I	GPIO port B
PD[0]/LEDFLSH	(Note)	I/O	GPIO port D
PD[5:1]		I/O	GPIO port D
PD[7:6]/SDQM[1:0]	(Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0]	(Note)	I	GPIO port E
PE[2]/CLKSEL	(Note)	I	GPIO port E

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

Table 16. Hardware Debug Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Table 17. LED Flasher Pin Assignments

Pin Mnemonic		I/O	Pin Description
PD[0]/LEDFLSH	(Note)	O	LED flasher driver

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.