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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-ibz

Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

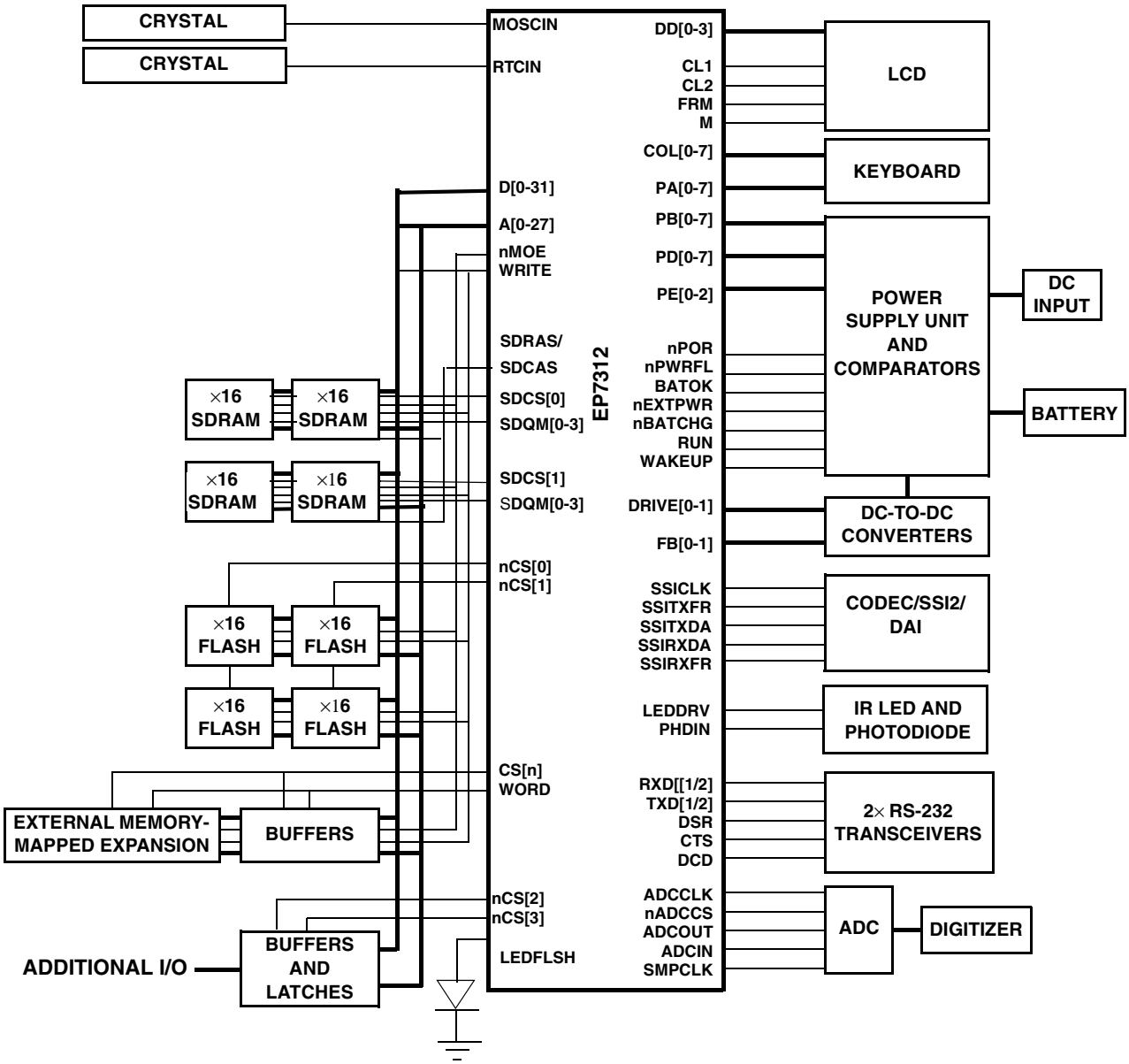

Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	

SDRAM Burst Read Cycle

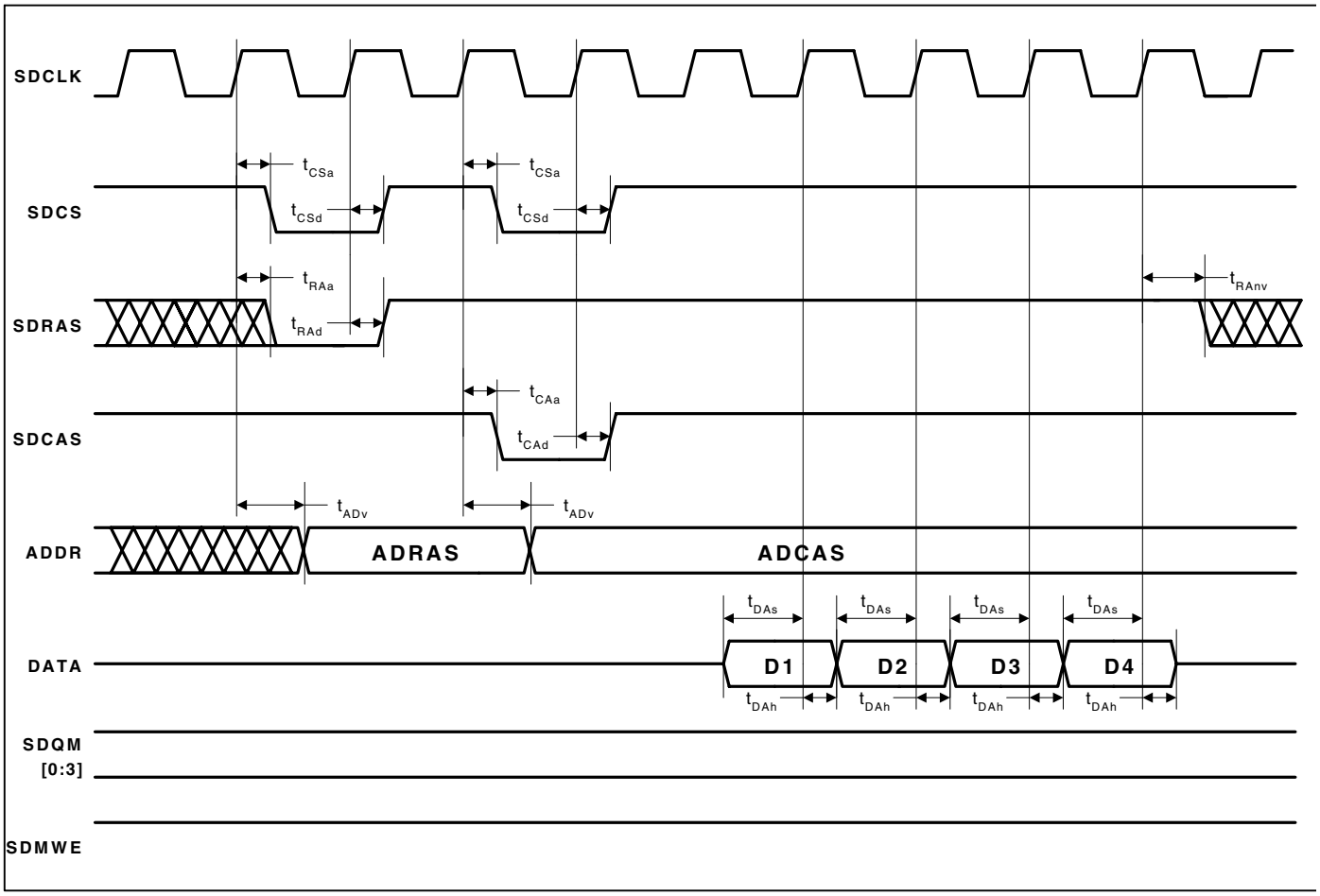

Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal.

Static Memory Burst Read Cycle

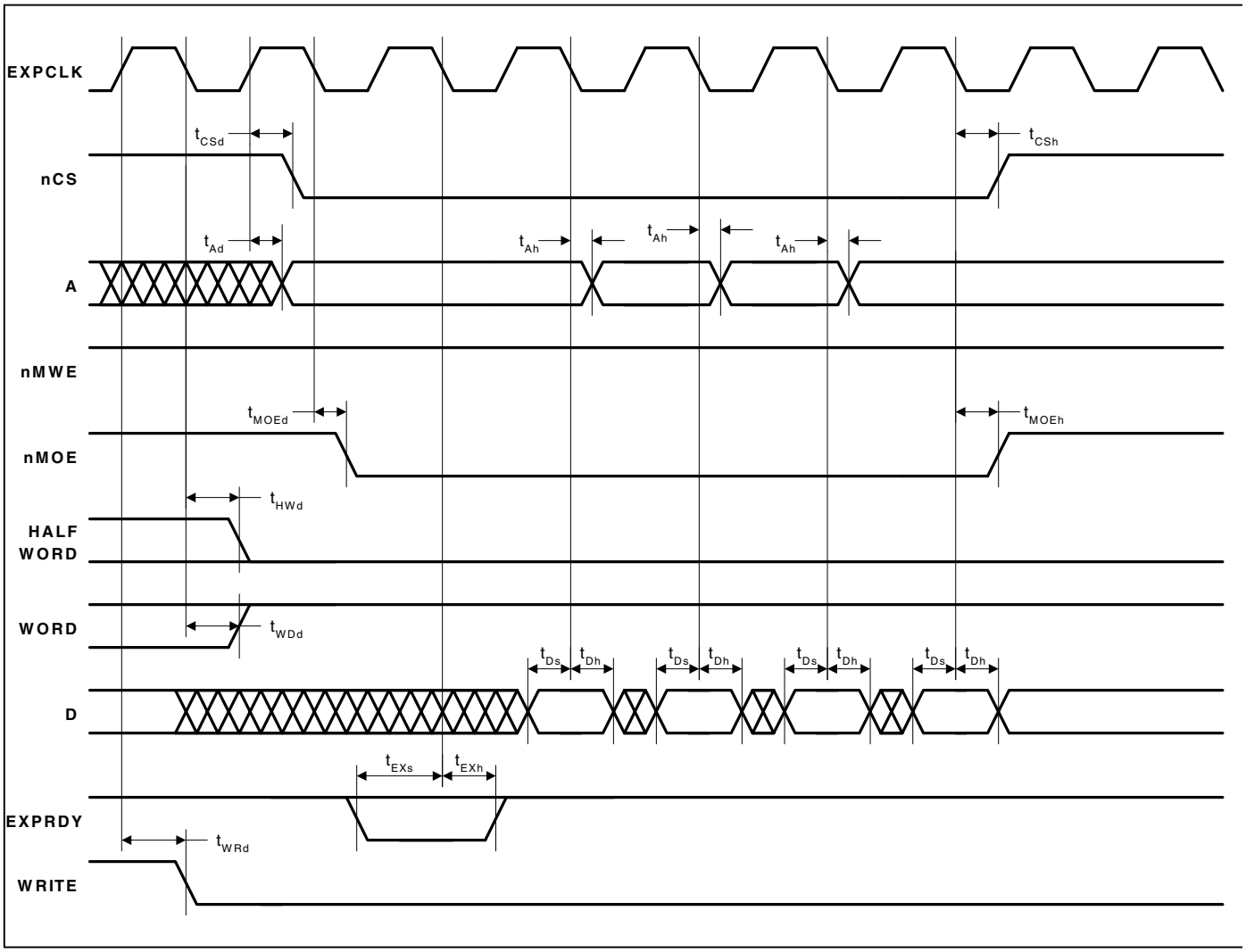

Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

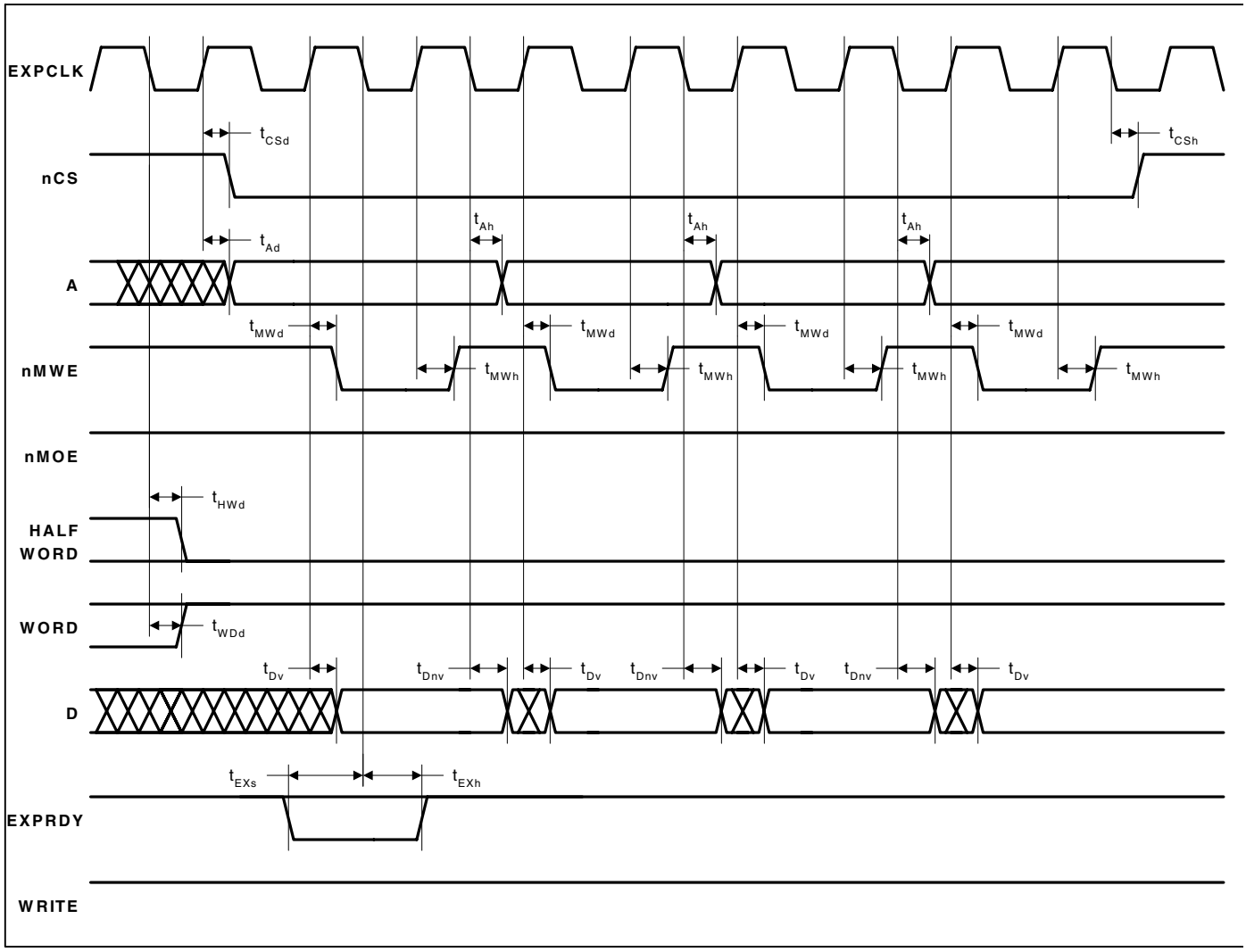

Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
38	DSR			I	UART 1 data set ready input
39	nTEST[1]	With p/u*		I	Test mode select input
40	nTEST[0]	With p/u*		I	Test mode select input
41	EINT[3]			I	External interrupt
42	nEINT[2]			I	External interrupt input
43	nEINT[1]			I	External interrupt input
44	nEXTFIQ			I	External fast interrupt input
45	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
46	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
47	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / Boot mode select
48	VSSRTC			RTC Gnd	Real time clock ground
49	RTCOUT			O	Real time clock oscillator output
50	RTCIN			I	Real time clock oscillator input
51	VDDRTC			RTC power	Real time clock power, 2.5 V
52	N/C				
53	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
54	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
55	PD[5]	1	Low	I/O	GPIO port D
56	PD[4]	1	Low	I/O	GPIO port D
57	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
58	TMS	with p/u*		I	JTAG mode select
59	PD[3]	1	Low	I/O	GPIO port D
60	PD[2]	1	Low	I/O	GPIO port D
61	PD[1]	1	Low	I/O	GPIO port D
62	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
63	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
64	VSSIO			Pad Gnd	I/O ground
65	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 serial clock
66	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
67	SSIRXDA			I	DAI/CODEC/SSI2 serial data input
68	SSIRXFR		Input‡	I/O	DAI/CODEC/SSI2 frame sync
69	ADCIN			I	SSI1 ADC serial input
70	nADCCS	1	High	O	SSI1 ADC chip select
71	VSSCORE			Core ground	Core ground
72	VDDCORE			Core Pwr	Core power, 2.5 V
73	VSSIO			Pad Gnd	I/O ground
74	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
75	DRIVE[1]	2	High / Low	I/O	PWM drive output
76	DRIVE[0]	2	High / Low	I/O	PWM drive output
77	ADCCLK	1	Low	O	SSI1 ADC serial clock
78	ADCOUT	1	Low	O	SSI1 ADC serial data output

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
118	D[20]	1	Low	I/O	Data I/O
119	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
120	D[19]	1	Low	I/O	Data I/O
121	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
122	D[18]	1	Low	I/O	Data I/O
123	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
124	VSSIO			Pad Gnd	I/O ground
125	nTRST			I	JTAG async reset input
126	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
127	D[17]	1	Low	I/O	Data I/O
128	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
129	D[16]	1	Low	I/O	Data I/O
130	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
131	D[15]	1	Low	I/O	Data I/O
132	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
133	D[14]	1	Low	I/O	Data I/O
134	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
135	D[13]	1	Low	I/O	Data I/O
136	A[12]	1	Low	O	System byte address
137	D[12]	1	Low	I/O	Data I/O
138	A[11]	1	Low	O	System byte address
139	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
140	VSSIO			Pad Gnd	I/O ground
141	D[11]	1	Low	I/O	Data I/O
142	A[10]	1	Low	O	System byte address
143	D[10]	1	Low	I/O	Data I/O
144	A[9]	1	Low	O	System byte address
145	D[9]	1	Low	I/O	Data I/O
146	A[8]	1	Low	O	System byte address
147	D[8]	1	Low	I/O	Data I/O
148	A[7]	1	Low	O	System byte address
149	VSSIO			Pad Gnd	I/O ground
150	D[7]	1	Low	I/O	Data I/O
151	nBATCHG			I	Battery changed sense input
152	nEXTPWR			I	External power supply sense input
153	BATOK			I	Battery OK input
154	nPOR	Schmitt		I	Power-on reset input
155	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
156	nURESET	Schmitt		I	User reset input
157	VDDOSC			Oscillator Power	Oscillator power in, 2.5 V
158	MOSCIN			I	Main oscillator input
159	MOSCOUT			O	Main oscillator output
160	VSSOSC			Oscillator Ground	Oscillator Ground

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
161	WAKEUP	Schmitt		I	System wake up input
162	nPWRFL			I	Power fail sense input
163	A[6]	1	Low	O	System byte address
164	D[6]	1	Low	I/O	Data I/O
165	A[5]	1	Low	Out	System byte address
166	D[5]	1	Low	I/O	Data I/O
167	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
168	VSSIO			Pad Gnd	I/O ground
169	A[4]	1	Low	O	System byte address
170	D[4]	1	Low	I/O	Data I/O
171	A[3]	2	Low	O	System byte address
172	D[3]	1	Low	I/O	Data I/O
173	A[2]	2	Low	O	System byte address
174	VSSIO			Pad Gnd	I/O ground
175	D[2]	1	Low	I/O	Data I/O
176	A[1]	2	Low	O	System byte address
177	D[1]	1	Low	I/O	Data I/O
178	A[0]	2	Low	O	System byte address
179	D[0]	1	Low	I/O	Data I/O
180	VSSCORE			Core ground	Core ground
181	VDDCORE			Core Pwr	Core power, 2.5 V
182	VSSIO			Pad ground	I/O ground
183	VDDIO			Pad Power	Digital I/O power, 3.3 V
184	CL[2]	1	Low	O	LCD pixel clock out
185	CL[1]	1	Low	O	LCD line clock
186	FRM	1	Low	O	LCD frame synchronization pulse
187	M	1	Low	O	LCD AC bias drive
188	DD[3]	1	Low	I/O	LCD serial display data
189	DD[2]	1	Low	I/O	LCD serial display data
190	VSSIO			Pad Gnd	I/O ground
191	DD[1]	1	Low	I/O	LCD serial display data
192	DD[0]	1	Low	I/O	LCD serial display data
193	nSDCS[1]	1	High	O	SDRAM chip select 1
194	nSDCS[0]	1	High	O	SDRAM chip select 0
195	SDQM[3]	2	Low	I/O	SDRAM byte lane mask
196	SDQM[2]	2	Low	I/O	SDRAM byte lane mask
197	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
198	VSSIO			Pad Gnd	I/O ground
199	SDCKE	2	Low	I/O	SDRAM clock enable output
200	SDCLK	2	Low	I/O	SDRAM clock out
201	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
202	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
203	VSSIO			Pad Gnd	I/O ground
204	nCS[0]	1	High	O	Chip select 0
205	nCS[1]	1	High	O	Chip select 1

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B8	DD[1]	1	Low	O	LCD serial display data
B9	M	1	Low	O	LCD AC bias drive
B10	CL[2]	1	Low	0	LCD pixel clock out
B11	D[0]	1	Low	I/O	Data I/O
B12	A[1]	2	Low	O	System byte address
B13	D[3]	2	Low	I/O	Data I/O
B14	A[4]	1	Low	O	System byte address
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	SDCLK	2	Low	O	SDRAM clock out
C7	SDQM[3]	2	Low	O	SDRAM byte lane mask
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
Y20	VDDIO			Pad power	Digital I/O power, 3.3V

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

256-Ball PBGA Package Characteristics

Figure 18. 256-Ball PBGA Package

Note: 1) For pin locations see Table 22.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7312 design, contact Cirrus Logic for the latest package information.

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table 22. 256-Ball PBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	nCS[4]	1	High	O	Chip select 4
A3	nCS[1]	1	High	O	Chip select 1
A4	SDCLK	2	Low	O	SDRAM clock out
A5	SDQM[3]	2	Low	O	SDRAM byte lane mask
A6	DD[1]	1	Low	O	LCD serial display data
A7	M	1	Low	O	LCD AC bias drive
A8	VDDIO			Pad power	Digital I/O power, 3.3 V
A9	D[0]	1	Low	I/O	Data I/O
A10	D[2]	1	Low	I/O	Data I/O
A11	A[3]	2	Low	O	System byte address
A12	VDDIO			Pad power	Digital I/O power, 3.3V
A13	A[6]	1	Low	O	System byte address
A14	MOSCOUT			O	Main oscillator out
A15	VDDOSC			Oscillator power	Oscillator power in, 2.5 V
A16	VSSIO			Pad ground	I/O ground
B1	nCS[5]	1	Low	O	Chip select 5
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[3]	1	High	O	Chip select 3
B4	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO			Pad power	Digital I/O power, 3.3 V
B6	nSDCS[1]	1	High	O	SDRAM chip select 1
B7	DD[2]	1	Low	O	LCD serial display data
B8	CL[1]	1	Low	O	LCD line clock
B9	VDDCORE			Core power	Digital core power, 2.5V
B10	D[1]	1	Low	I/O	Data I/O
B11	A[2]	2	Low	O	System byte address
B12	A[4]	1	Low	O	System byte address
B13	A[5]	1	Low	O	System byte address
B14	WAKEUP	Schmitt		I	System wake up input
B15	VDDIO			Pad power	Digital I/O power, 3.3 V
B16	nURESET	Schmitt		I	User reset input
C1	VDDIO			Pad power	Digital I/O power, 3.3V
C2	EXPCLK	1		I	Expansion clock input
C3	VSSIO			Pad ground	I/O ground
C4	VDDIO			Pad power	Digital I/O power, 3.3 V
C5	VSSIO			Pad ground	I/O ground
C6	VSSIO			Pad ground	I/O ground
C7	VSSIO			Pad ground	I/O ground
C8	VDDIO			Pad power	Digital I/O power, 3.3 V
C9	VSSIO			Pad ground	I/O ground
C10	VSSIO			Pad ground	I/O ground
C11	VSSIO			Pad ground	I/O ground
C12	VDDIO			Pad power	Digital I/O power, 3.3 V

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
110	U20	M13	A[23]/DRA[4]	O	194
111	T19	N16	D[23]	I/O	196
112	T20	L12	A[22]/DRA[5]	O	199
113	R19	N15	D[22]	I/O	201
114	R20	L13	A[21]/DRA[6]	O	204
115	T18	M16	D[21]	I/O	206
117	P19	M15	A[20]/DRA[7]	O	209
118	P20	K11	D[20]	I/O	211
119	R18	L16	A[19]/DRA[8]	O	214
120	N19	K12	D[19]	I/O	216
121	N20	L15	A[18]/DRA[9]	O	219
122	P18	K13	D[18]	I/O	221
126	M19	J10	A[17]/DRA[10]	O	224
127	N18	J16	D[17]	I/O	226
128	L20	J11	A[16]/DRA[11]	O	229
129	L19	J15	D[16]	I/O	231
130	M18	J12	A[15]/DRA[12]	O	234
131	K20	H16	D[15]	I/O	236
132	K19	J13	A[14]/DRA[13]	O	239
133	K18	H15	D[14]	I/O	241
134	J20	H13	A[13]/DRA[14]	O	244
135	J19	G16	D[13]	I/O	246
136	H20	H12	A[12]	O	249
137	H19	G15	D[12]	I/O	251
138	J18	H11	A[11]	O	254
141	G20	F15	D[11]	I/O	256
142	H18	H10	A[10]	O	259
143	F20	E16	D[10]	I/O	261
144	G19	G13	A[9]	O	264
145	E20	E15	D[9]	I/O	266
146	F19	G12	A[8]	O	269
147	G18	D16	D[8]	I/O	271
148	D20	G11	A[7]	O	274
150	F18	D15	D[7]	I/O	276
151	D19	F13	nBATCHG	I	279
152	E19	C16	nEXTPWR	I	280
153	C19	F12	BATOK	I	281
154	C20	C15	nPOR	I	282

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
155	E18	E13	nMEDCHG/nBROM	I	283
156	B20	B16	nURESET	I	284
161	B16	B14	WAKEUP	I	285
162	A16	D11	nPWRFL	I	286
163	C15	A13	A[6]	O	287
164	B15	F10	D[6]	I/O	289
165	A15	B13	A[5]	O	292
166	C14	E10	D[5]	I/O	294
169	B14	B12	A[4]	O	297
170	A14	D10	D[4]	I/O	299
171	C13	A11	A[3]	O	302
172	B13	G9	D[3]	I/O	304
173	A13	B11	A[2]	O	307
175	C12	A10	D[2]	I/O	309
176	B12	F9	A[1]	O	312
177	A12	B10	D[1]	I/O	314
178	C11	E9	A[0]	O	317
179	B11	A9	D[0]	I/O	319
184	B10	D8	CL2	O	322
185	A10	B8	CL1	O	324
186	A9	E8	FRM	O	326
187	B9	A7	M	O	328
188	C9	F8	DD[3]	O	330
189	A8	B7	DD[2]	O	333
191	B8	A6	DD[1]	O	336
192	C8	G8	DD[0]	O	339
193	A7	B6	nSDCS[1]	O	342
194	B7	D7	nSDCS[0]	O	344
195	C7	A5	SDQM[3]	I/O	346
196	A6	E7	SDQM[2]	I/O	349
199	B6	F7	SDCKE	I/O	352
200	C6	A4	SDCLK	I/O	355
201	A5	D6	nMWE/nSDWE	O	358
202	B5	B4	nMOE/nSDCAS	O	360
204	C5	E6	nCS[0]	O	362
205	A4	A3	nCS[1]	O	364

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
206	B4	D5	nCS[2]	O	366
207	A3	B3	nCS[3]	O	368
208	C4	A2	nCS[4]	O	370

1) See EP7312 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase "h" appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, '11' designates a binary number). Numbers not indicated by an "h", 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the *EP7312 User's Manual*. The use of "TBD" indicates values that are "to be determined," "n/a" designates "not available," and "n/c" indicates a pin that is a "no connect."

Pin Description Conventions

Abbreviations used for signal directions are listed in Table 26.

Table 26. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output


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