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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7TDMI |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 74MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | Keypad, LCD, Touchscreen |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 2.7V, 3.0V, 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | Hardware ID |
| Package / Case | 208-LQFP |
| Supplier Device Package | 208-LQFP |
| Purchase URL | https://www.e-xfl.com/product-detail/cirrus-logic/ep7312-iv |

## FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

## OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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## Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:

**http://www.cirrus.com/corporate/contacts/sales.cfm**



## 64-Key Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7312. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state. The Keypad Interface has these features:

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Table 10 shows the Keypad Interface Pin Assignments.

**Table 10. Keypad Interface Pin Assignments**

| Pin Mnemonic | I/O | Pin Description |
|---|---|---|
| COL[7:0] | O | Keyboard scanner column drive |

## Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7312 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources. The Interrupt controller has these features:

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

Table 11 shows the interrupt controller pin assignments.

**Table 11. Interrupt Controller Pin Assignments**

| Pin Mnemonic | I/O | Pin Description |
|---|---|---|
| nEINT[2:1] | I | External interrupt |
| EINT[3] | I | External interrupt |
| nEXTFIQ | I | External Fast Interrupt input |
| nMEDCHG/nBROM (Note) | I | Media change interrupt input |

*Note: Pins are multiplexed. See Table 19 on page 11 for more information.*

## Real-Time Clock

The EP7312 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Table 12 shows the Real-Time Clock pin assignments.

**Table 12. Real-Time Clock Pin Assignments**

| Pin Mnemonic | Pin Description |
|---|---|
| RTCIN | Real-Time Clock Oscillator Input |
| RTCOUT | Real-Time Clock Oscillator Output |
| VDDRTC | Real-Time Clock Oscillator Power |
| VSSRTC | Real-Time Clock Oscillator Ground |

## PLL and Clocking

The EP7312 processor and peripheral clocks have these features:

- Processor and peripheral clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz, and at 45 MHz when the processor is set to 90 MHz.

Table 13 shows the PLL and clocking pin assignments.

**Table 13. PLL and Clocking Pin Assignments**

| Pin Mnemonic | Pin Description |
|---|---|
| MOSCIN | Main Oscillator Input |
| MOSCOUT | Main Oscillator Output |
| VDDOSC | Main Oscillator Power |
| VSSOSC | Main Oscillator Ground |

## DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

**Table 14. DC-to-DC Converter Interface Pin Assignments**

| Pin Mnemonic | I/O | Pin Description |
|---|---|---|
| DRIVE[1:0] | I/O | PWM drive output |
| FB[1:0] | I | PWM feedback input |

## Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

## General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

**Table 15. General Purpose Input/Output Pin Assignments**

| Pin Mnemonic | | I/O | Pin Description |
|---|---|---|---|
| PA[7:0] | | I | GPIO port A |
| PB[7:0] | | I | GPIO port B |
| PD[0]/LEDFLSH | (Note) | I/O | GPIO port D |
| PD[5:1] | | I/O | GPIO port D |
| PD[7:6]/SDQM[1:0] | (Note) | I/O | GPIO port D |
| PE[1:0]/BOOTSEL[1:0] | (Note) | I | GPIO port E |
| PE[2]/CLKSEL | (Note) | I | GPIO port E |

*Note: Pins are multiplexed. See Table 19 on page 11 for more information.*

## Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

**Table 16. Hardware Debug Interface Pin Assignments**

| Pin Mnemonic | I/O | Pin Description |
|---|---|---|
| TCLK | I | JTAG clock |
| TDI | I | JTAG data input |
| TDO | O | JTAG data output |
| nTRST | I | JTAG async reset input |
| TMS | I | JTAG mode select |

## LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

**Table 17. LED Flasher Pin Assignments**

| Pin Mnemonic | | I/O | Pin Description |
|---|---|---|---|
| PD[0]/LEDFLSH | (Note) | O | LED flasher driver |

*Note: Pins are multiplexed. See Table 19 on page 11 for more information.*

## Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

## Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.

## Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| EXPCLK rising edge to nCS assert delay time | $t_{CSd}$ | 2 | 8 | 20 | ns |
| EXPCLK falling edge to nCS deassert hold time | $t_{CSh}$ | 2 | 7 | 20 | ns |
| EXPCLK rising edge to A assert delay time | $t_{Ad}$ | 4 | 9 | 16 | ns |
| EXPCLK falling edge to A deassert hold time | $t_{Ah}$ | 3 | 10 | 19 | ns |
| EXPCLK rising edge to nMWE assert delay time | $t_{MWd}$ | 3 | 6 | 10 | ns |
| EXPCLK rising edge to nMWE deassert hold time | $t_{MWh}$ | 3 | 6 | 10 | ns |
| EXPCLK falling edge to nMOE assert delay time | $t_{MOEd}$ | 3 | 7 | 10 | ns |
| EXPCLK falling edge to nMOE deassert hold time | $t_{MOEh}$ | 2 | 7 | 10 | ns |
| EXPCLK falling edge to HALFWORD deassert delay time | $t_{HWd}$ | 2 | 8 | 20 | ns |
| EXPCLK falling edge to WORD assert delay time | $t_{WDd}$ | 2 | 8 | 16 | ns |
| EXPCLK rising edge to data valid delay time | $t_{Dv}$ | 8 | 13 | 21 | ns |
| EXPCLK falling edge to data invalid delay time | $t_{Dnv}$ | 6 | 15 | 30 | ns |
| Data setup to EXPCLK falling edge time | $t_{Ds}$ | - | - | 1 | ns |
| EXPCLK falling edge to data hold time | $t_{Dh}$ | - | - | 3 | ns |
| EXPCLK rising edge to WRITE assert delay time | $t_{WRd}$ | 5 | 11 | 23 | ns |
| EXPREADY setup to EXPCLK falling edge time | $t_{EXs}$ | - | - | 0 | ns |
| EXPCLK falling edge to EXPREADY hold time | $t_{EXh}$ | - | - | 0 | ns |

## *Static Memory Single Read Cycle*

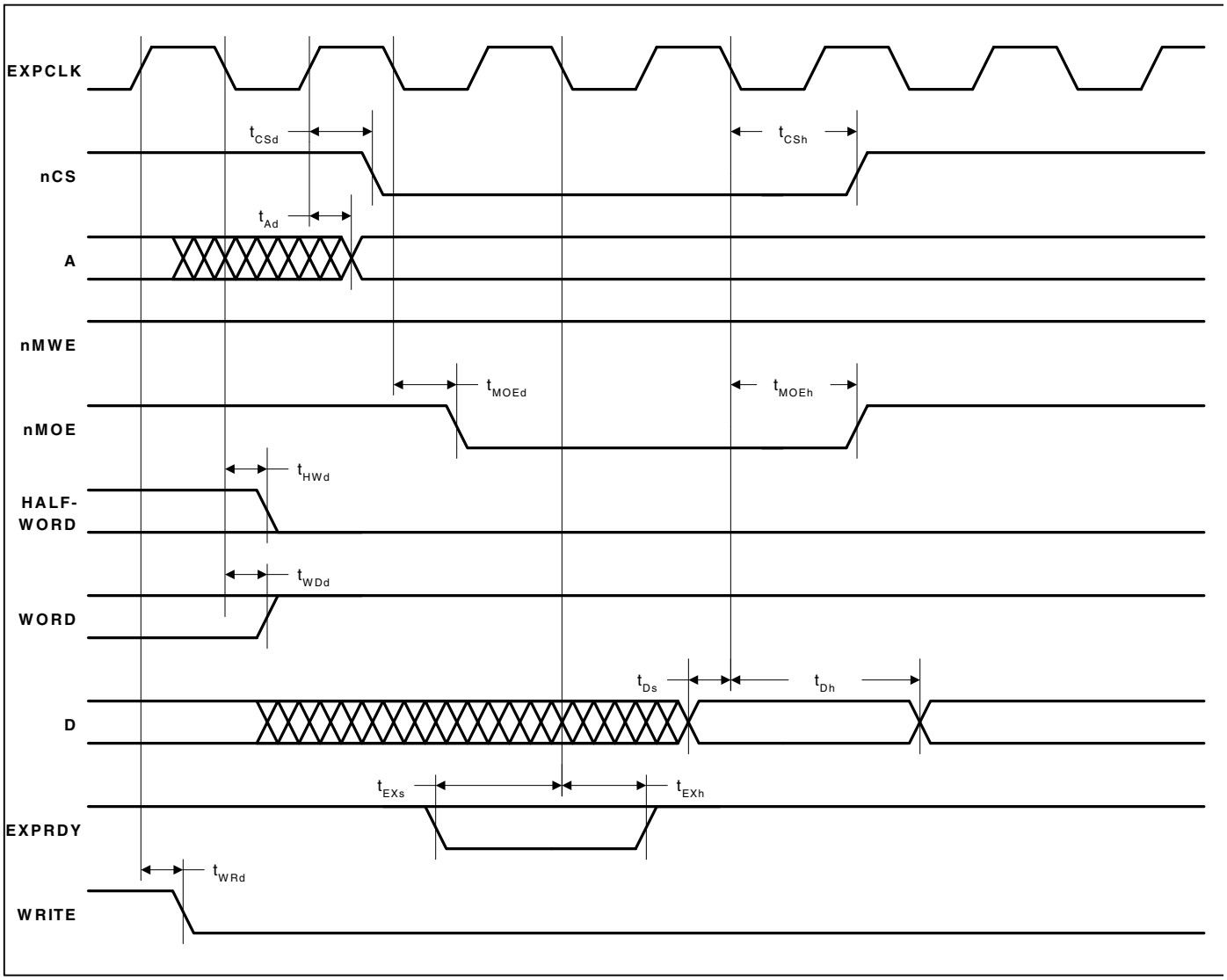



**Figure 7. Static Memory Single Read Cycle Timing Measurement**

*Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.*
*2. Address, Halfword, Word, and Write hold state until next cycle.*

## *Static Memory Burst Read Cycle*

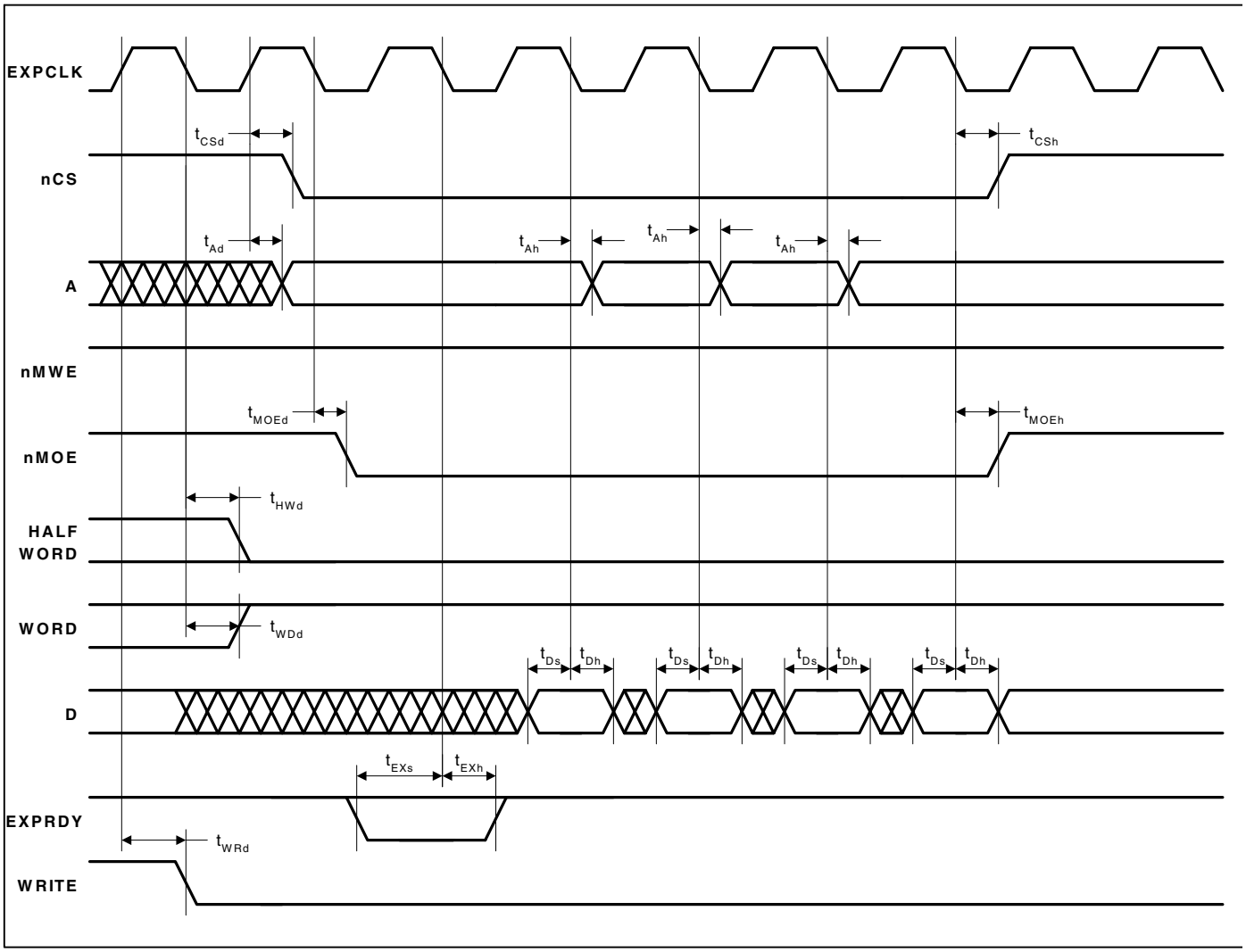



**Figure 9. Static Memory Burst Read Cycle Timing Measurement**

*Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.*
*2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.*
*3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.*
*4. Address, Halfword, Word, and Write hold state until next cycle.*

## SSI2 Interface

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| SSICLK period (slave mode) | $t_{clk\_per}$ | 185 | 2050 | ns |
| SSICLK high time | $t_{clk\_high}$ | 925 | 1025 | ns |
| SSICLK low time | $t_{clk\_low}$ | 925 | 1025 | ns |
| SSICLK rise/fall time | $t_{clkrf}$ | 3 | 18 | ns |
| SSICLK rising edge to RX and/or TX frame sync high time | $t_{FRd}$ | - | 3 | ns |
| SSICLK rising edge to RX and/or TX frame sync low time | $t_{FRa}$ | - | 8 | ns |
| SSIRXFR and/or SSITXFR period | $t_{FR\_per}$ | 960 | 990 | ns |
| SSIRXDA setup to SSICLK falling edge time | $t_{RXs}$ | 3 | 7 | ns |
| SSIRXDA hold from SSICLK falling edge time | $t_{RXh}$ | 3 | 7 | ns |
| SSICLK rising edge to SSITXDA data valid delay time | $t_{TXd}$ | - | 2 | ns |
| SSITXDA valid time | $t_{TXv}$ | 960 | 990 | ns |

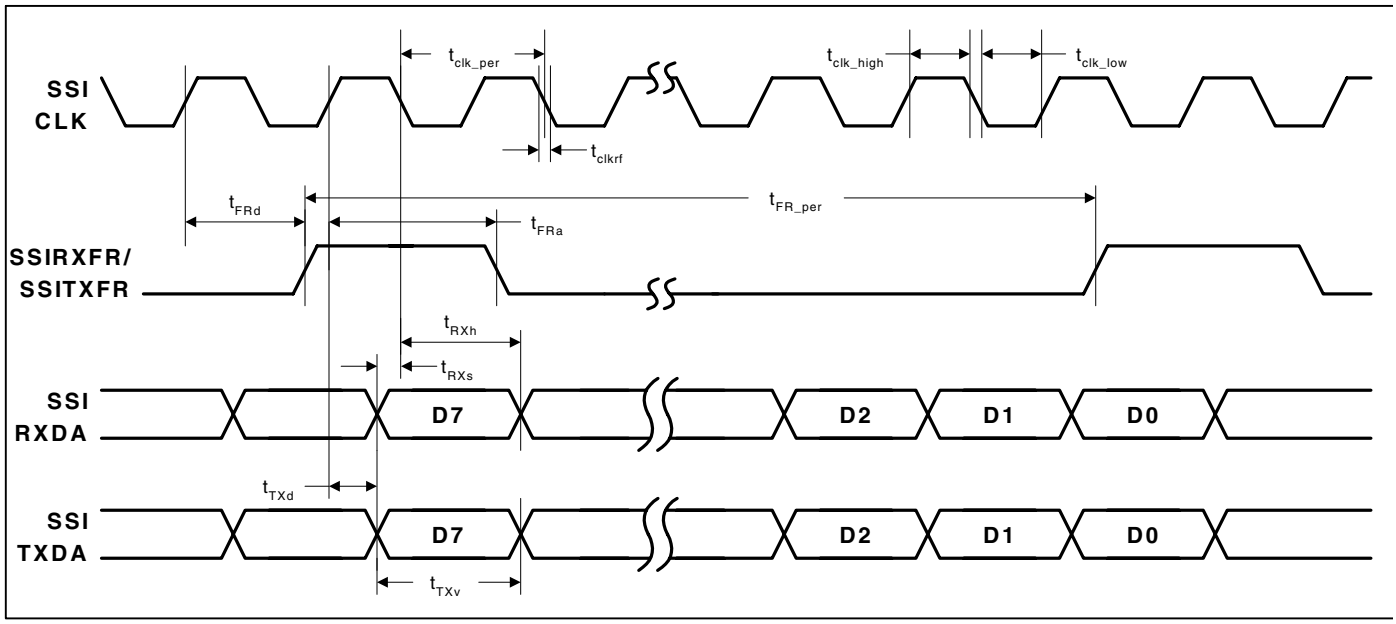



**Figure 12. SSI2 Interface Timing Measurement**

## JTAG Interface

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| TCK clock period | $t_{clk\_per}$ | 2 | - | ns |
| TCK clock high time | $t_{clk\_high}$ | 1 | - | ns |
| TCK clock low time | $t_{clk\_low}$ | 1 | - | ns |
| JTAG port setup time | $t_{JPs}$ | - | 0 | ns |
| JTAG port hold time | $t_{JPh}$ | - | 3 | ns |
| JTAG port clock to output | $t_{JPco}$ | - | 10 | ns |
| JTAG port high impedance to valid output | $t_{JPzx}$ | - | 12 | ns |
| JTAG port valid output to high impedance | $t_{JPxz}$ | - | 19 | ns |

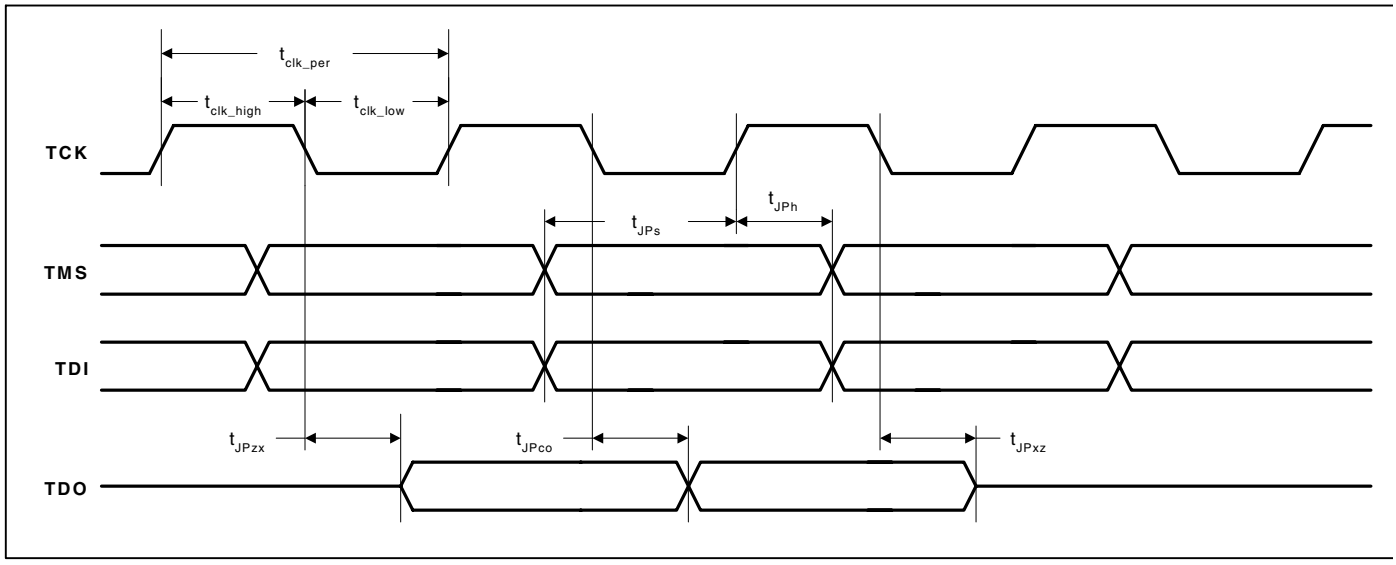



**Figure 14. JTAG Timing Measurement**

## 208-Pin LQFP Pin Diagram

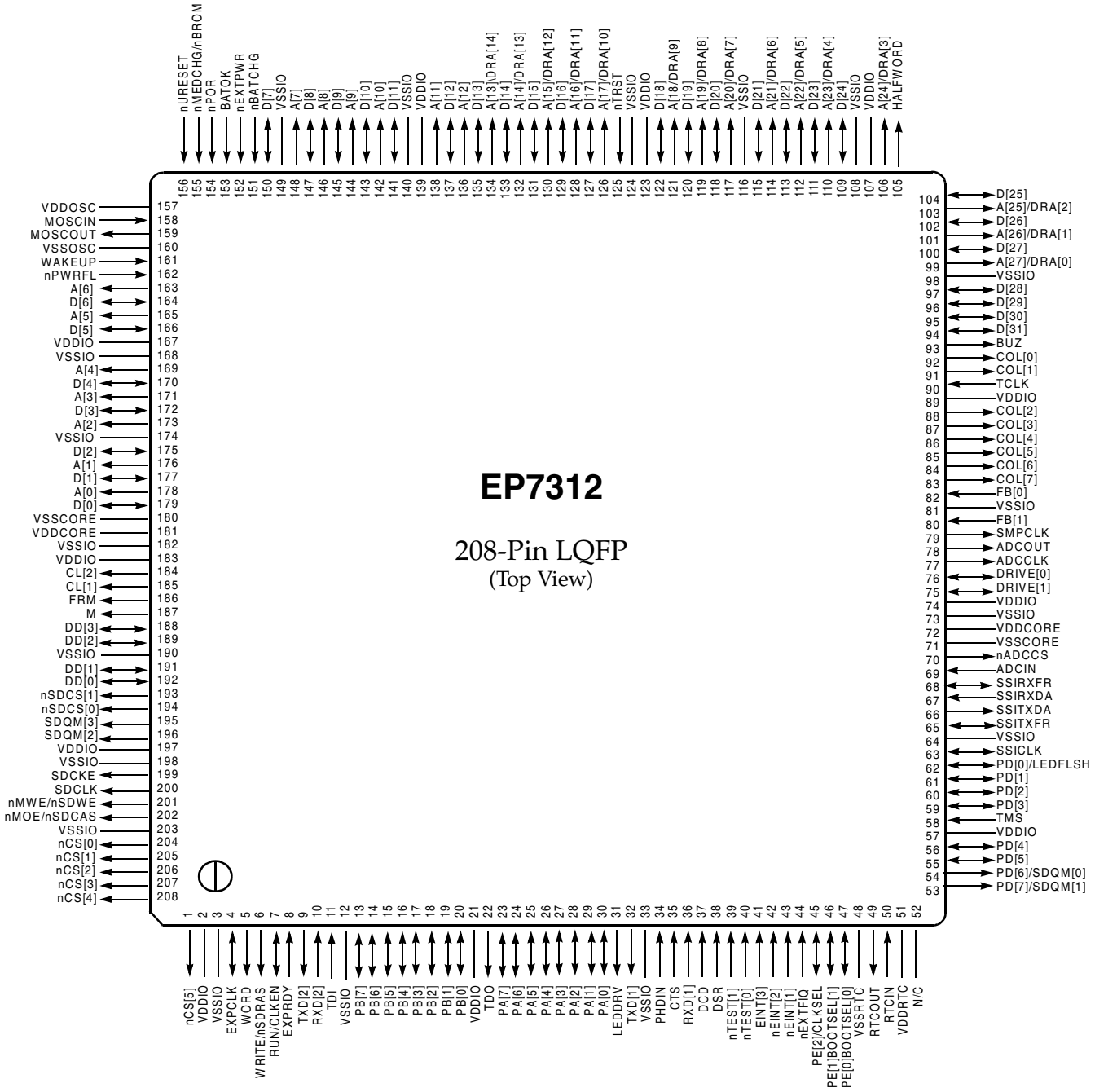



**Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram**

*Note: 1. N/C should not be grounded but left as no connects.*

# 208-Pin LQFP Numeric Pin Listing

**Table 20. 208-Pin LQFP Numeric Pin Listing**

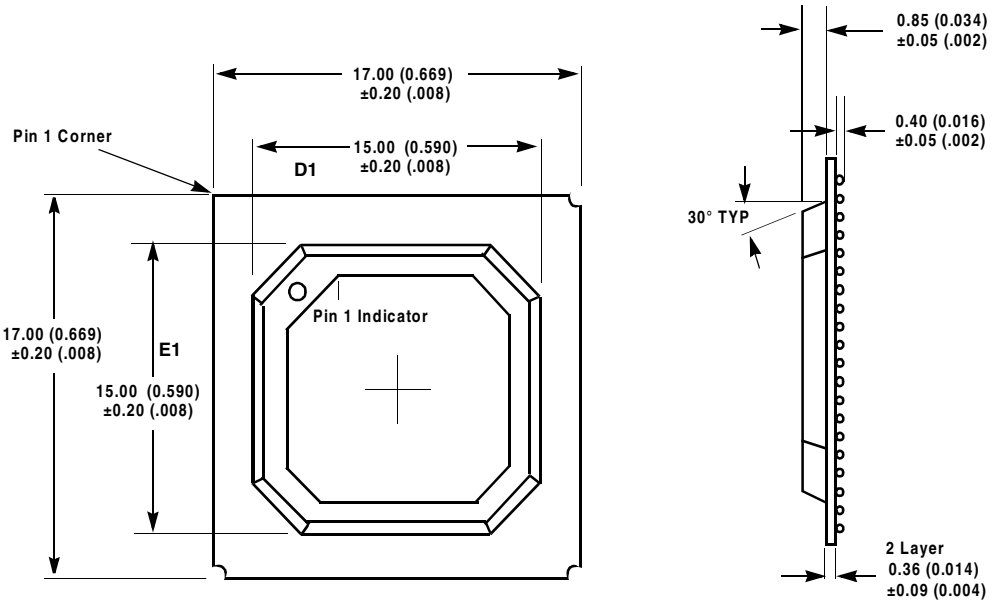
| Pin No. | Signal | Strength† | Reset State | Type | Description |
|---|---|---|---|---|---|
| 1 | nCS[5] | 1 | Low | O | Chip select 5 |
| 2 | VDDIO | | | Pad Pwr | Digital I/O power, 3.3 V |
| 3 | VSSIO | | | Pad Gnd | I/O ground |
| 4 | EXPCLK | 1 | | I | Expansion clock input |
| 5 | WORD | 1 | Low | O | Word access select output |
| 6 | WRITE/nSDRAS | 1 | Low | O | Transfer direction / SDRAM RAS signal output |
| 7 | RUN/CLKEN | 1 | Low | O | Run output / clock enable output |
| 8 | EXPRDY | 1 | | I | Expansion port ready input |
| 9 | TXD[2] | 1 | High | O | UART 2 transmit data output |
| 10 | RXD[2] | | | I | UART 2 receive data input |
| 11 | TDI | with p/u* | | I | JTAG data input |
| 12 | VSSIO | | | Pad Gnd | I/O ground |
| 13 | PB[7] | 1 | Input‡ | I/O | GPIO port B |
| 14 | PB[6] | 1 | Input‡ | I/O | GPIO port B |
| 15 | PB[5] | 1 | Input‡ | I/O | GPIO port B |
| 16 | PB[4] | 1 | Input‡ | I/O | GPIO port B |
| 17 | PB[3] | 1 | Input‡ | I/O | GPIO port B |
| 18 | PB[2] | 1 | Input‡ | I/O | GPIO port B |
| 19 | PB[1] | 1 | Input‡ | I/O | GPIO port B |
| 20 | PB[0] | 1 | Input‡ | I/O | GPIO port B |
| 21 | VDDIO | | | Pad Pwr | Digital I/O power, 3.3 V |
| 22 | TDO | 1 | Input‡ | O | JTAG data out |
| 23 | PA[7] | 1 | Input‡ | I/O | GPIO port A |
| 24 | PA[6] | 1 | Input‡ | I/O | GPIO port A |
| 25 | PA[5] | 1 | Input‡ | I/O | GPIO port A |
| 26 | PA[4] | 1 | Input‡ | I/O | GPIO port A |
| 27 | PA[3] | 1 | Input‡ | I/O | GPIO port A |
| 28 | PA[2] | 1 | Input‡ | I/O | GPIO port A |
| 29 | PA[1] | 1 | Input‡ | I/O | GPIO port A |
| 30 | PA[0] | 1 | Input‡ | I/O | GPIO port A |
| 31 | LEDDRV | 1 | Low | O | IR LED drive |
| 32 | TXD[1] | 1 | High | O | UART 1 transmit data out |
| 33 | VSSIO | 1 | High | Pad Gnd | I/O ground |
| 34 | PHDIN | | | I | Photodiode input |
| 35 | CTS | | | I | UART 1 clear to send input |
| 36 | RXD[1] | | | I | UART 1 receive data input |
| 37 | DCD | | | I | UART 1 data carrier detect |

**Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)**

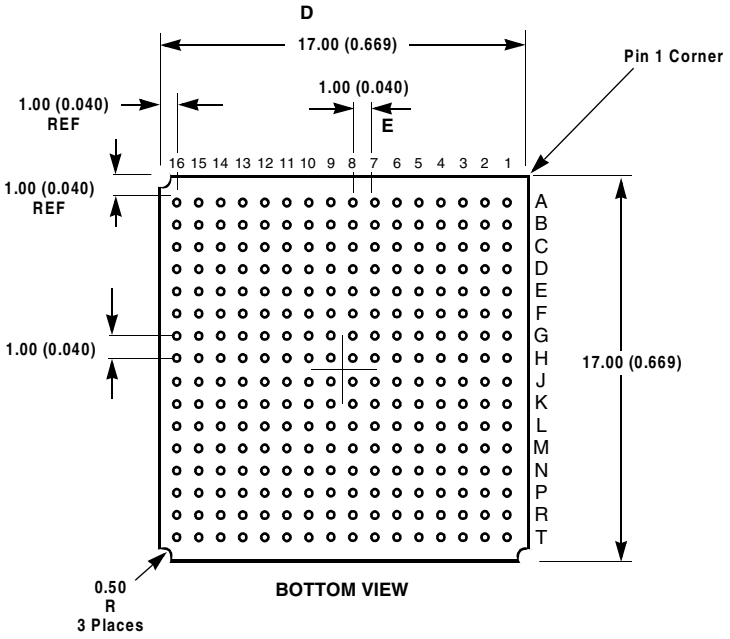
| Pin No. | Signal | Strength† | Reset State | Type | Description |
|---|---|---|---|---|---|
| 118 | D[20] | 1 | Low | I/O | Data I/O |
| 119 | A[19]/DRA[8] | 1 | Low | O | System byte address / SDRAM address |
| 120 | D[19] | 1 | Low | I/O | Data I/O |
| 121 | A[18]/DRA[9] | 1 | Low | O | System byte address / SDRAM address |
| 122 | D[18] | 1 | Low | I/O | Data I/O |
| 123 | VDDIO | | | Pad Pwr | Digital I/O power, 3.3 V |
| 124 | VSSIO | | | Pad Gnd | I/O ground |
| 125 | nTRST | | | I | JTAG async reset input |
| 126 | A[17]/DRA[10] | 1 | Low | O | System byte address / SDRAM address |
| 127 | D[17] | 1 | Low | I/O | Data I/O |
| 128 | A[16]/DRA[11] | 1 | Low | O | System byte address / SDRAM address |
| 129 | D[16] | 1 | Low | I/O | Data I/O |
| 130 | A[15]/DRA[12] | 1 | Low | O | System byte address / SDRAM address |
| 131 | D[15] | 1 | Low | I/O | Data I/O |
| 132 | A[14]/DRA[13] | 1 | Low | O | System byte address / SDRAM address |
| 133 | D[14] | 1 | Low | I/O | Data I/O |
| 134 | A[13]/DRA[14] | 1 | Low | O | System byte address / SDRAM address |
| 135 | D[13] | 1 | Low | I/O | Data I/O |
| 136 | A[12] | 1 | Low | O | System byte address |
| 137 | D[12] | 1 | Low | I/O | Data I/O |
| 138 | A[11] | 1 | Low | O | System byte address |
| 139 | VDDIO | | | Pad Pwr | Digital I/O power, 3.3 V |
| 140 | VSSIO | | | Pad Gnd | I/O ground |
| 141 | D[11] | 1 | Low | I/O | Data I/O |
| 142 | A[10] | 1 | Low | O | System byte address |
| 143 | D[10] | 1 | Low | I/O | Data I/O |
| 144 | A[9] | 1 | Low | O | System byte address |
| 145 | D[9] | 1 | Low | I/O | Data I/O |
| 146 | A[8] | 1 | Low | O | System byte address |
| 147 | D[8] | 1 | Low | I/O | Data I/O |
| 148 | A[7] | 1 | Low | O | System byte address |
| 149 | VSSIO | | | Pad Gnd | I/O ground |
| 150 | D[7] | 1 | Low | I/O | Data I/O |
| 151 | nBATCHG | | | I | Battery changed sense input |
| 152 | nEXTPWR | | | I | External power supply sense input |
| 153 | BATOK | | | I | Battery OK input |
| 154 | nPOR | Schmitt | | I | Power-on reset input |
| 155 | nMEDCHG/nBROM | | | I | Media change interrupt input / internal ROM boot enable |
| 156 | nURESET | Schmitt | | I | User reset input |
| 157 | VDDOSC | | | Oscillator Power | Oscillator power in, 2.5 V |
| 158 | MOSCIN | | | I | Main oscillator input |
| 159 | MOSCOUT | | | O | Main oscillator output |
| 160 | VSSOSC | | | Oscillator Ground | Oscillator Ground |

**Table 21. 204-Ball TFBGA Ball Listing (Continued)**

| Ball Location | Name | Strength† | Reset State | Type | Description |
|---|---|---|---|---|---|
| W11 | ADCOUT | 1 | Low | O | SSI1 ADC serial data output |
| W12 | FB[0] | | | I | PWM feedback input |
| W13 | COL[5] | 1 | High | O | Keyboard scanner column drive |
| W14 | COL[2] | 1 | High | O | Keyboard scanner column drive |
| W15 | COL[0] | 1 | High | O | Keyboard scanner column drive |
| W16 | D[30] | 1 | Low | I/O | Data I/O |
| W17 | A[27]/DRA[0] | 2 | Low | O | System byte address / SDRAM address |
| W18 | D[26] | 1 | Low | I/O | Data I/O |
| W19 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| W20 | D[25] | 1 | Low | I/O | Data I/O |
| Y1 | VSSIO | | | Pad ground | I/O ground |
| Y2 | VSSIO | | | Pad ground | I/O ground |
| Y3 | VSSIO | | | Pad ground | I/O ground |
| Y4 | PD[5] | 1 | Low | I/O | GPIO port D |
| Y5 | PD[3] | 1 | Low | I/O | GPIO port D |
| Y6 | PD[0]/LEDFLSH | 1 | Low | I/O | GPIO port D / LED blinker output |
| Y7 | SSITXDA | 1 | Low | O | DAI/CODEC/SSI2 serial data output |
| Y8 | ADCIN | | | I | SSI1 ADC serial input |
| Y9 | VDDCORE | | | Core power | Digital core power, 2.5V |
| Y10 | DRIVE[0] | 2 | Input‡ | I/O | PWM drive output |
| Y11 | SMPCLK | 1 | Low | O | SSI1 ADC sample clock |
| Y12 | FB[1] | | | I | PWM feedback input |
| Y13 | COL[6] | 1 | High | O | Keyboard scanner column drive |
| Y14 | COL[3] | 1 | High | O | Keyboard scanner column drive |
| Y15 | COL[1] | 1 | High | O | Keyboard scanner column drive |
| Y16 | D[31] | 1 | Low | I/O | Data I/O |
| Y17 | D[28] | 1 | Low | I/O | Data I/O |
| Y18 | D[27] | 1 | Low | I/O | Data I/O |
| Y19 | A[25]/DRA[2] | 2 | Low | O | System byte address / SDRAM address |




**TOP VIEW** **SIDE VIEW**




**BOTTOM VIEW**

**JEDEC #: MO-151**
**Ball Diameter: 0.50 mm ± 0.10 mm**
**17 ¥ 17 ¥ 1.61 mm body**

## 256-Ball PBGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VDDIO | nCS[4] | nCS[1] | SDCLK | SDQM[3] | DD[1] | M | VDDIO | D[0] | D[2] | A[3] | VDDIO | A[6] | MOSCOUT | VDDOSC | VSSIO | A |
| B | nCS[5] | VDDIO | nCS[3] | nMOE/ nSDCAS | VDDIO | nSDCS[1] | DD[2] | CL[1] | VDDCORE | D[1] | A[2] | A[4] | A[5] | WAKEUP | VDDIO | nURESET | B |
| C | VDDIO | EXPCLK | VSSIO | VDDIO | VSSIO | VSSIO | VSSIO | VDDIO | VSSIO | VSSIO | VSSIO | VDDIO | VSSIO | VSSIO | nPOR | nEXTPWR | C |
| D | WRITE/ nSDRAS | EXPRDY | VSSIO | VDDIO | nCS[2] | nMWE/ nSDWE | nSDCS[0] | CL[2] | VSSRTC | D[4] | nPWRFL | MOSCIN | VDDIO | VSSIO | D[7] | D[8] | D |
| E | RXD[2] | PB[7] | TDI | WORD | VSSIO | nCS[0] | SDQM[2] | FRM | A[0] | D[5] | VSSOSC | VSSIO | nMEDCHG/ nBROM | VDDIO | D[9] | D[10] | E |
| F | PB[5] | PB[3] | VSSIO | TXD[2] | RUN/ CLKEN | VSSIO | SDCKE | DD[3] | A[1] | D[6] | VSSRTC | BATOK | nBATCHG | VSSIO | D[11] | VDDIO | F |
| G | PB[1] | VDDIO | TDO | PB[4] | PB[6] | VSSCore | VSSRTC | DD[0] | D[3] | VSSRTC | A[7] | A[8] | A[9] | VSSIO | D[12] | D[13] | G |
| H | PA[7] | PA[5] | VSSIO | PA[4] | PA[6] | PB[0] | PB[2] | VSSRTC | VSSRTC | A[10] | A[11] | A[12] | A[13]/ DRA[14] | VSSIO | D[14] | D[15] | H |
| J | PA[3] | PA[1] | VSSIO | PA[2] | PA[0] | TXD[1] | CTS | VSSRTC | VSSRTC | A[17]/ DRA[10] | A[16]/ DRA[11] | A[15]/ DRA[12] | A[14]/ DRA[13] | nTRST | D[16] | D[17] | J |
| K | LEDDRV | PHDIN | VSSIO | DCD | nTEST[1] | EINT[3] | VSSRTC | ADCIN | COL[4] | TCLK | D[20] | D[19] | D[18] | VSSIO | VDDIO | VDDIO | K |
| L | RXD[1] | DSR | VDDIO | nEINT[1] | PE[2]/ CLKSEL | VSSRTC | PD[0]/ LEDFLSH | VSSRTC | COL[6] | D[31] | VSSRTC | A[22]/ DRA[5] | A[21]/ DRA[6] | VSSIO | A[18]/ DRA[9] | A[19]/ DRA[8] | L |
| M | nTEST[0] | nEINT[2] | VDDIO | PE[0]/ BOOTSEL[0] | TMS | VDDIO | SSITXFR | DRIVE[1] | FB[0] | COL[0] | D[27] | VSSIO | A[23]/ DRA[4] | VDDIO | A[20]/ DRA[7] | D[21] | M |
| N | nEXTFIQ | PE[1]/ BOOTSEL[1] | VSSIO | VDDIO | PD[5] | PD[2] | SSIRXDA | ADCCLK | SMPCLK | COL[2] | D[29] | D[26] | HALFWORD | VSSIO | D[22] | D[23] | N |
| P | VSSRTC | RTCOUT | VSSIO | VSSIO | VDDIO | VSSIO | VSSIO | VDDIO | VSSIO | VDDIO | VSSIO | VSSIO | VDDIO | VSSIO | D[24] | VDDIO | P |
| R | RTCIN | VDDIO | PD[4] | PD[1] | SSITXDA | nADCCS | VDDIO | ADCOUT | COL[7] | COL[3] | COL[1] | D[30] | A[27]/ DRA[0] | A[25]/ DRA[2] | VDDIO | A[24]\ DRA[3] | R |
| T | VDDRTC | PD[7]/ SDQM[1] | PD[6]/ SDQM[0] | PD[3] | SSICLK | SSIRXFR | VDDCORE | DRIVE[0] | FB[1] | COL[5] | VDDIO | BUZ | D[28] | A[26]/ DRA[1] | D[25] | VSSIO | T |

**Table 22. 256-Ball PBGA Ball Listing (Continued)**

| Ball Location | Name | Strength† | Reset State | Type | Description |
|---|---|---|---|---|---|
| C13 | VSSIO | | | Pad ground | I/O ground |
| C14 | VSSIO | | | Pad ground | I/O ground |
| C15 | nPOR | Schmitt | | I | Power-on reset input |
| C16 | nEXTPWR | | | I | External power supply sense input |
| D1 | WRITE/nSDRAS | 1 | Low | O | Transfer direction / SDRAM RAS signal output |
| D2 | EXPRDY | 1 | | I | Expansion port ready input |
| D3 | VSSIO | | | Pad ground | I/O ground |
| D4 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| D5 | nCS[2] | 1 | High | O | Chip select 2 |
| D6 | nMWE/nSDWE | 1 | High | O | ROM, expansion write enable/ SDRAM write enable control signal |
| D7 | nSDCS[0] | 1 | High | O | SDRAM chip select 2 |
| D8 | CL[2] | 1 | Low | O | LCD pixel clock out |
| D9 | VSSRTC | | | Core ground | Real time clock ground |
| D10 | D[4] | 1 | Low | I/O | Data I/O |
| D11 | nPWRFL | | | I | Power fail sense input |
| D12 | MOSCIN | | | I | Main oscillator input |
| D13 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| D14 | VSSIO | | | Pad ground | I/O ground |
| D15 | D[7] | 1 | Low | I/O | Data I/O |
| D16 | D[8] | 1 | Low | I/O | Data I/O |
| E1 | RXD[2] | | | I | UART 2 receive data input |
| E2 | PB[7] | 1 | Input‡ | I | GPIO port B |
| E3 | TDI | with p/u* | | I | JTAG data input |
| E4 | WORD | 1 | Low | O | Word access select output |
| E5 | VSSIO | | | Pad ground | I/O ground |
| E6 | nCS[0] | 1 | High | O | Chip select 0 |
| E7 | SDQM[2] | 2 | Low | O | SDRAM byte lane mask |
| E8 | FRM | 1 | Low | O | LCD frame synchronization pulse |
| E9 | A[0] | 2 | Low | O | System byte address |
| E10 | D[5] | 1 | Low | I/O | Data I/O |
| E11 | VSSOSC | | | Oscillator ground | PLL ground |
| E12 | VSSIO | | | Pad ground | I/O ground |
| E13 | nMEDCHG/nBROM | | | I | Media change interrupt input / internal ROM boot enable |
| E14 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| E15 | D[9] | 1 | Low | I/O | Data I/O |
| E16 | D[10] | 1 | Low | I/O | Data I/O |
| F1 | PB[5] | 1 | Input‡ | I | GPIO port B |
| F2 | PB[3] | 1 | Input‡ | I | GPIO port B |
| F3 | VSSIO | | | Pad ground | I/O ground |
| F4 | TXD[2] | 1 | High | O | UART 2 transmit data output |
| F5 | RUN/CLKEN | 1 | Low | O | Run output / clock enable output |
| F6 | VSSIO | | | Pad ground | I/O ground |
| F7 | SDCKE | 2 | Low | O | SDRAM clock enable output |
| F8 | DD[3] | 1 | Low | O | LCD serial display data |
| F9 | A[1] | 2 | Low | O | System byte address |

**Table 22. 256-Ball PBGA Ball Listing (Continued)**

| Ball Location | Name | Strength† | Reset State | Type | Description |
|---|---|---|---|---|---|
| J5 | PA[0] | 1 | Input‡ | I/O | GPIO port A |
| J6 | TXD[1] | 1 | High | O | UART 1 transmit data out |
| J7 | CTS | | | I | UART 1 clear to send input |
| J8 | VSSRTC | | | RTC ground | Real time clock ground |
| J9 | VSSRTC | | | RTC ground | Real time clock ground |
| J10 | A[17]/DRA[10] | 1 | Low | O | System byte address / SDRAM address |
| J11 | A[16]/DRA[11] | 1 | Low | O | System byte address / SDRAM address |
| J12 | A[15]/DRA[12] | 1 | Low | O | System byte address / SDRAM address |
| J13 | A[14]/DRA[13] | 1 | Low | O | System byte address / SDRAM address |
| J14 | nTRST | | | I | JTAG async reset input |
| J15 | D[16] | 1 | Low | I/O | Data I/O |
| J16 | D[17] | 1 | Low | I/O | Data I/O |
| K1 | LEDDRV | 1 | Low | O | IR LED drive |
| K2 | PHDIN | | | I | Photodiode input |
| K3 | VSSIO | | | Pad ground | I/O ground |
| K4 | DCD | | | I | UART 1 data carrier detect |
| K5 | nTEST[1] | With p/u* | | I | Test mode select input |
| K6 | EINT[3] | | | I | External interrupt |
| K7 | VSSRTC | | | RTC ground | Real time clock ground |
| K8 | ADCIN | | | I | SSI1 ADC serial input |
| K9 | COL[4] | 1 | High | O | Keyboard scanner column drive |
| K10 | TCLK | | | I | JTAG clock |
| K11 | D[20] | 1 | Low | I/O | Data I/O |
| K12 | D[19] | 1 | Low | I/O | Data I/O |
| K13 | D[18] | 1 | Low | I/O | Data I/O |
| K14 | VSSIO | | | Pad ground | I/O ground |
| K15 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| K16 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| L1 | RXD[1] | | | I | UART 1 receive data input |
| L2 | DSR | | | I | UART 1 data set ready input |
| L3 | VDDIO | | | Pad power | Digital I/O power, 3.3V |
| L4 | nEINT[1] | | | I | External interrupt input |
| L5 | PE[2]/CLKSEL | 1 | Input‡ | I/O | GPIO port E / clock input mode select |
| L6 | VSSRTC | | | RTC ground | Real time clock ground |
| L7 | PD[0]/LEDFLSH | 1 | Low | I/O | GPIO port D / LED blinker output |
| L8 | VSSRTC | | | Core ground | Real time clock ground |
| L9 | COL[6] | 1 | High | O | Keyboard scanner column drive |
| L10 | D[31] | 1 | Low | I/O | Data I/O |
| L11 | VSSRTC | | | RTC ground | Real time clock ground |
| L12 | A[22]/DRA[5] | 1 | Low | O | System byte address / SDRAM address |
| L13 | A[21]/DRA[6] | 1 | Low | O | System byte address / SDRAM address |
| L14 | VSSIO | | | Pad ground | I/O ground |
| L15 | A[18]/DRA[9] | 1 | Low | O | System byte address / SDRAM address |
| L16 | A[19]/DRA[8] | 1 | Low | O | System byte address / SDRAM address |
| M1 | nTEST[0] | With p/u* | | I | Test mode select input |
| M2 | nEINT[2] | | | I | External interrupt input |
| M3 | VDDIO | | | Pad power | Digital I/O power, 3.3V |

**Table 23. JTAG Boundary Scan Signal Ordering (Continued)**

| LQFP Pin No. | TFBGA Ball | PBGA Ball | Signal | Type | Position |
|---|---|---|---|---|---|
| 55 | Y4 | N5 | PD[5] | I/O | 95 |
| 56 | V5 | R3 | PD[4] | I/O | 98 |
| 59 | Y5 | T4 | PD[3] | I/O | 101 |
| 60 | V6 | N6 | PD[2] | I/O | 104 |
| 61 | W6 | R4 | PD[1] | I/O | 107 |
| 62 | Y6 | L7 | PD[0]/LEDFLSH | O | 110 |
| 68 | W8 | T6 | SSIRXFR | I/O | 122 |
| 69 | Y8 | K8 | ADCIN | I | 125 |
| 70 | V9 | R6 | nADCCS | O | 126 |
| 75 | W10 | M8 | DRIVE1 | I/O | 128 |
| 76 | Y10 | T8 | DRIVE0 | I/O | 131 |
| 77 | V11 | N8 | ADCCLK | O | 134 |
| 78 | W11 | R8 | ADCOUT | O | 136 |
| 79 | Y11 | N9 | SMPCLK | O | 138 |
| 80 | Y12 | T9 | FB1 | I | 140 |
| 82 | Y11 | M9 | FB0 | I | 141 |
| 83 | Y12 | R9 | COL7 | O | 142 |
| 84 | Y13 | L9 | COL6 | O | 144 |
| 85 | W13 | T10 | COL5 | O | 146 |
| 86 | V13 | K9 | COL4 | O | 148 |
| 87 | Y14 | R10 | COL3 | O | 150 |
| 88 | W14 | N10 | COL2 | O | 152 |
| 91 | Y15 | R11 | COL1 | O | 154 |
| 92 | W15 | M10 | COL0 | O | 156 |
| 93 | V15 | T12 | BUZ | O | 158 |
| 94 | Y16 | L10 | D[31] | I/O | 160 |
| 95 | W16 | R12 | D[30] | I/O | 163 |
| 96 | V16 | N11 | D[29] | I/O | 166 |
| 97 | Y17 | T13 | D[28] | I/O | 169 |
| 99 | Y16 | R13 | A[27]/DRA[0] | Out | 172 |
| 100 | Y18 | M11 | D[27] | I/O | 174 |
| 101 | V17 | T14 | A[26]/DRA[1] | O | 177 |
| 102 | W18 | N12 | D[26] | I/O | 179 |
| 103 | Y19 | R14 | A[25]/DRA[2] | O | 182 |
| 104 | Y20 | T15 | D[25] | I/O | 184 |
| 105 | U18 | N13 | HALFWORD | O | 187 |
| 106 | V209 | R16 | A[24]/DRA[3] | O | 189 |
| 109 | U19 | P15 | D[24] | I/O | 191 |

**Table 23. JTAG Boundary Scan Signal Ordering (Continued)**

| LQFP Pin No. | TFBGA Ball | PBGA Ball | Signal | Type | Position |
|---|---|---|---|---|---|
| 110 | U20 | M13 | A[23]/DRA[4] | O | 194 |
| 111 | T19 | N16 | D[23] | I/O | 196 |
| 112 | T20 | L12 | A[22]/DRA[5] | O | 199 |
| 113 | R19 | N15 | D[22] | I/O | 201 |
| 114 | R20 | L13 | A[21]/DRA[6] | O | 204 |
| 115 | T18 | M16 | D[21] | I/O | 206 |
| 117 | P19 | M15 | A[20]/DRA[7] | O | 209 |
| 118 | P20 | K11 | D[20] | I/O | 211 |
| 119 | R18 | L16 | A[19]/DRA[8] | O | 214 |
| 120 | N19 | K12 | D[19] | I/O | 216 |
| 121 | N20 | L15 | A[18]/DRA[9] | O | 219 |
| 122 | P18 | K13 | D[18] | I/O | 221 |
| 126 | M19 | J10 | A[17]/DRA[10] | O | 224 |
| 127 | N18 | J16 | D[17] | I/O | 226 |
| 128 | L20 | J11 | A[16]/DRA[11] | O | 229 |
| 129 | L19 | J15 | D[16] | I/O | 231 |
| 130 | M18 | J12 | A[15]/DRA[12] | O | 234 |
| 131 | K20 | H16 | D[15] | I/O | 236 |
| 132 | K19 | J13 | A[14]/DRA[13] | O | 239 |
| 133 | K18 | H15 | D[14] | I/O | 241 |
| 134 | J20 | H13 | A[13]/DRA[14] | O | 244 |
| 135 | J19 | G16 | D[13] | I/O | 246 |
| 136 | H20 | H12 | A[12] | O | 249 |
| 137 | H19 | G15 | D[12] | I/O | 251 |
| 138 | J18 | H11 | A[11] | O | 254 |
| 141 | G20 | F15 | D[11] | I/O | 256 |
| 142 | H18 | H10 | A[10] | O | 259 |
| 143 | F20 | E16 | D[10] | I/O | 261 |
| 144 | G19 | G13 | A[9] | O | 264 |
| 145 | E20 | E15 | D[9] | I/O | 266 |
| 146 | F19 | G12 | A[8] | O | 269 |
| 147 | G18 | D16 | D[8] | I/O | 271 |
| 148 | D20 | G11 | A[7] | O | 274 |
| 150 | F18 | D15 | D[7] | I/O | 276 |
| 151 | D19 | F13 | nBATCHG | I | 279 |
| 152 | E19 | C16 | nEXTPWR | I | 280 |
| 153 | C19 | F12 | BATOK | I | 281 |
| 154 | C20 | C15 | nPOR | I | 282 |

# CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

## Acronyms and Abbreviations

Table 24 lists abbreviations and acronyms used in this data sheet.

**Table 24. Acronyms and Abbreviations**

| Acronym/ Abbreviation | Definition |
|---|---|
| A/D | analog-to-digital |
| ADC | analog-to-digital converter |
| CODEC | coder / decoder |
| D/A | digital-to-analog |
| DMA | direct-memory access |
| EPB | embedded peripheral bus |
| FCS | frame check sequence |
| FIFO | first in / first out |
| FIQ | fast interrupt request |
| GPIO | general purpose I/O |
| ICT | in circuit test |
| IR | infrared |
| IRQ | standard interrupt request |
| IrDA | Infrared Data Association |
| JTAG | Joint Test Action Group |
| LCD | liquid crystal display |
| LED | light-emitting diode |
| LQFP | low profile quad flat pack |
| LSB | least significant bit |
| MIPS | millions of instructions per second |
| MMU | memory management unit |
| MSB | most significant bit |
| PBGA | plastic ball grid array |
| PCB | printed circuit board |
| PDA | personal digital assistant |
| PLL | phase locked loop |
| p/u | pull-up resistor |
| RISC | reduced instruction set computer |
| RTC | Real-Time Clock |
| SIR | slow (9600–115.2 kbps) infrared |
| SRAM | static random access memory |
| SSI | synchronous serial interface |

**Table 24. Acronyms and Abbreviations (Continued)**

| Acronym/ Abbreviation | Definition |
|---|---|
| TAP | test access port |
| TLB | translation lookaside buffer |
| UART | universal asynchronous receiver |

## Units of Measurement

**Table 25. Unit of Measurement**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| fs | sample frequency |
| Hz | hertz (cycle per second) |
| kbps | kilobits per second |
| KB | kilobyte (1,024 bytes) |
| kHz | kilohertz |
| kΩ | kilo Ohm |
| Mbps | megabits (1,048,576 bits) per second |
| MB | megabyte (1,048,576 bytes) |
| MBps | megabytes per second |
| MHz | megahertz (1,000 kilohertz) |
| µA | microampere |
| µF | microfarad |
| µW | microwatt |
| µs | microsecond (1,000 nanoseconds) |
| mA | milliampere |
| mW | milliwatt |
| ms | millisecond (1,000 microseconds) |
| ns | nanosecond |
| V | volt |
| W | watt |