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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7312m-cbz

CODEC Interface

The EP7312 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the DAI and SSI2. Table 6 shows the CODEC Interface Pin Assignments.

Table 6. CODEC Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Note: See Table 18 on page 11 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the DAI and CODEC interfaces through a multiplexer. The SSI2 Interface has these features:

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Table 7 shows the SSI2 Interface pin assignments.

Table 7. SSI2 Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Note: See Table 18 on page 11 for information on pin multiplexes.

Synchronous Serial Interface

The EP7312 Synchronous Serial Interface has these features:

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Table 8 shows the Synchronous Serial Interface pin assignments.

Table 8. Serial Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM. The LCD controller has these features:

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Table 9 shows the LCD Interface pin assignments.

Table 9. LCD Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

64-Key Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7312. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state. The Keypad Interface has these features:

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Table 10 shows the Keypad Interface Pin Assignments.

Table 10. Keypad Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7312 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources. The Interrupt controller has these features:

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

Table 11 shows the interrupt controller pin assignments.

Table 11. Interrupt Controller Pin Assignments

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Real-Time Clock

The EP7312 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Table 12 shows the Real-Time Clock pin assignments.

Table 12. Real-Time Clock Pin Assignments

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

PLL and Clocking

The EP7312 processor and peripheral clocks have these features:

- Processor and peripheral clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz, and at 45 MHz when the processor is set to 90 MHz.

Table 13 shows the PLL and clocking pin assignments.

Table 13. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @2.5 V[1] I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{IDLE} at 90 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	7 11	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

SDRAM Burst Write Cycle

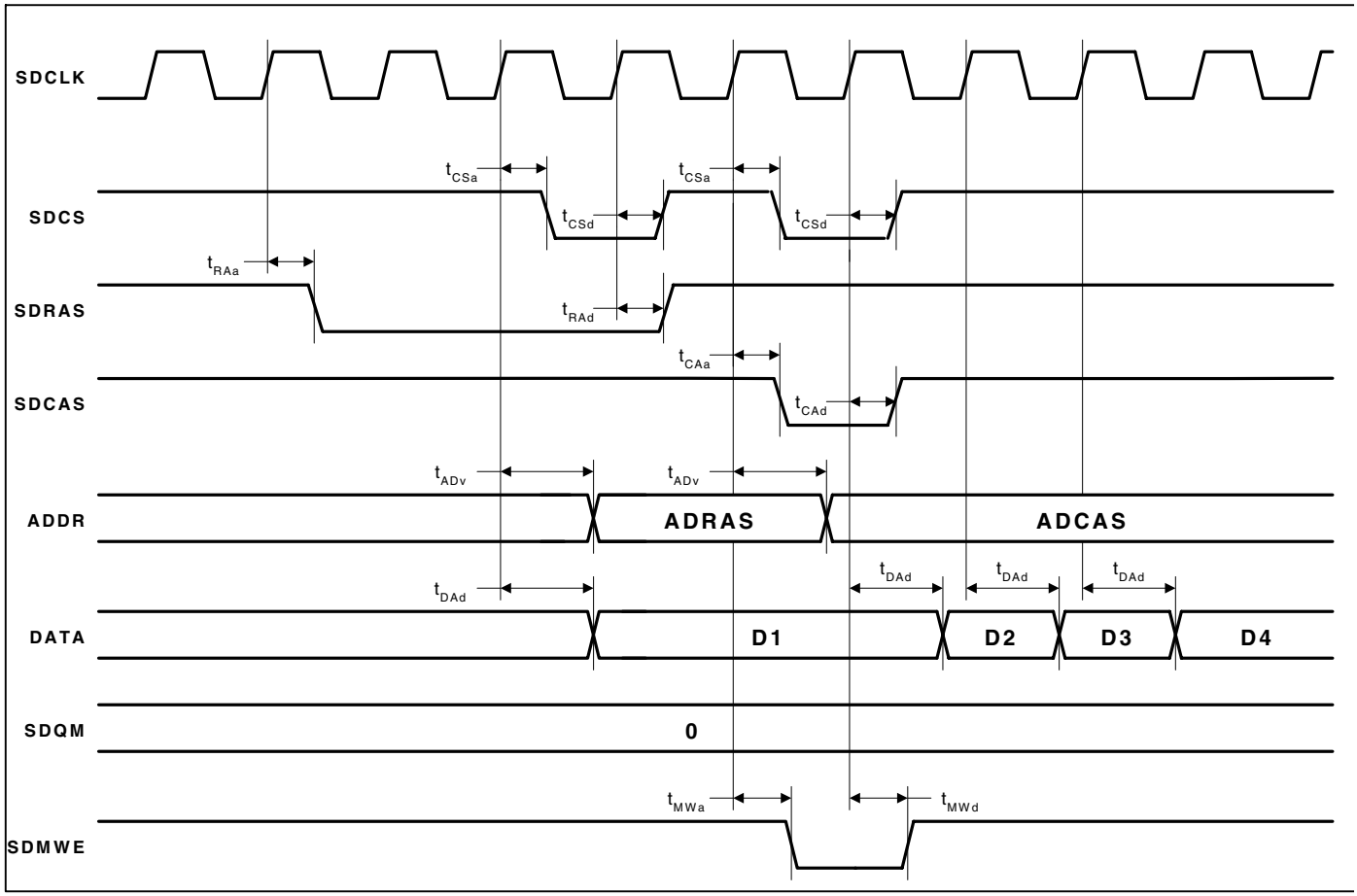


Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

Static Memory Burst Write Cycle

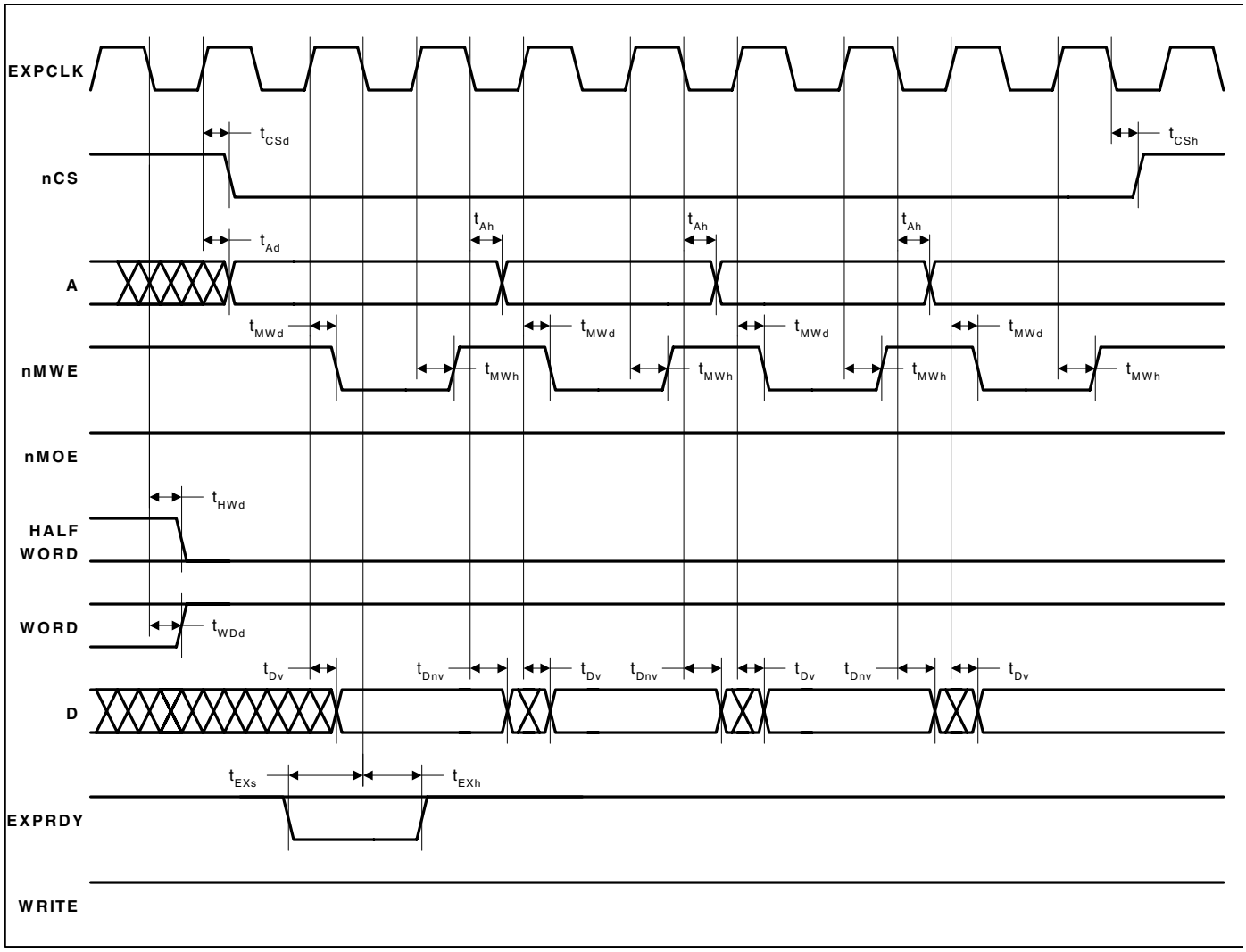


Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

Packages

208-Pin LQFP Package Characteristics

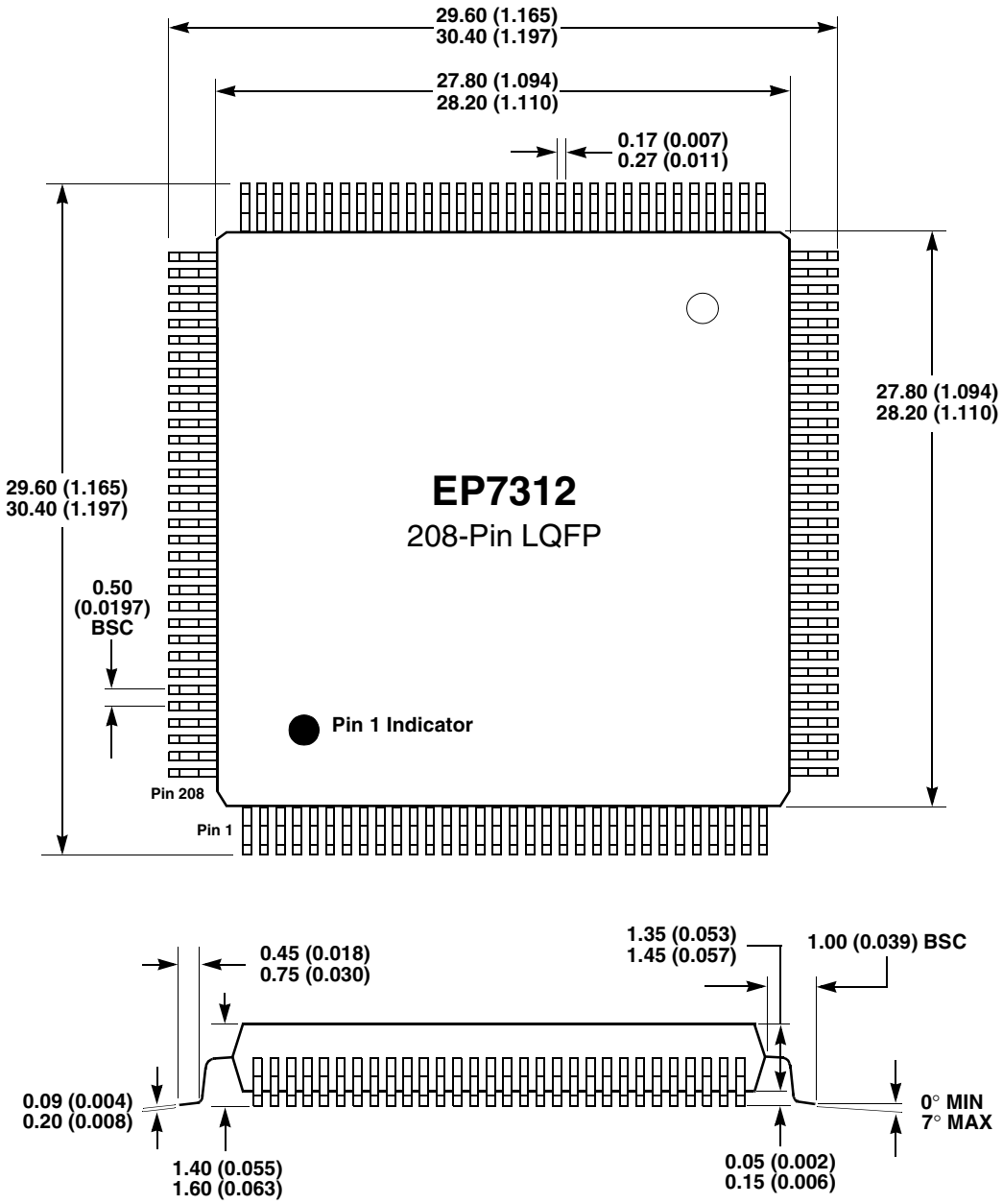


Figure 15. 208-Pin LQFP Package Outline Drawing

Note: 1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 16. For pin descriptions see the EP7312 User's Manual.

208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
79	SMPCLK	1	Low	O	SSI1 ADC sample clock
80	FB[1]			I	PWM feedback input
81	VSSIO			Pad Gnd	I/O ground
82	FB[0]			I	PWM feedback input
83	COL[7]	1	High	O	Keyboard scanner column drive
84	COL[6]	1	High	O	Keyboard scanner column drive
85	COL[5]	1	High	O	Keyboard scanner column drive
86	COL[4]	1	High	O	Keyboard scanner column drive
87	COL[3]	1	High	O	Keyboard scanner column drive
88	COL[2]	1	High	O	Keyboard scanner column drive
89	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
90	TCLK			I	JTAG clock
91	COL[1]	1	High	O	Keyboard scanner column drive
92	COL[0]	1	High	O	Keyboard scanner column drive
93	BUZ	1	Low	O	Buzzer drive output
94	D[31]	1	Low	I/O	Data I/O
95	D[30]	1	Low	I/O	Data I/O
96	D[29]	1	Low	I/O	Data I/O
97	D[28]	1	Low	I/O	Data I/O
98	VSSIO			Pad Gnd	I/O ground
99	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
100	D[27]	1	Low	I/O	Data I/O
101	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
102	D[26]	1	Low	I/O	Data I/O
103	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
104	D[25]	1	Low	I/O	Data I/O
105	HALFWORD	1	Low	O	Halfword access select output
106	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
107	VDDIO		—	Pad Pwr	Digital I/O power, 3.3 V
108	VSSIO		—	Pad Gnd	I/O ground
109	D[24]	1	Low	I/O	Data I/O
110	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
111	D[23]	1	Low	I/O	Data I/O
112	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
113	D[22]	1	Low	I/O	Data I/O
114	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
115	D[21]	1	Low	I/O	Data I/O
116	VSSIO			Pad Gnd	I/O ground
117	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
206	nCS[2]	1	High	O	Chip select 2
207	nCS[3]	1	High	O	Chip select 3
208	nCS[4]	1	High	O	Chip select 4

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
F10	D[6]	1	Low	I/O	Data I/O
F11	VSSRTC			RTC ground	Real time clock ground
F12	BATOK			I	Battery OK input
F13	nBATCHG			I	Battery changed sense input
F14	VSSIO			Pad ground	I/O ground
F15	D[11]	1	Low	I/O	Data I/O
F16	VDDIO			Pad power	Digital I/O power, 3.3V
G1	PB[1]	1	Input‡	I	GPIO port B
G2	VDDIO			Pad power	Digital I/O power, 3.3V
G3	TDO	1	Input‡	O	JTAG data out
G4	PB[4]	1	Input‡	I	GPIO port B
G5	PB[6]	1	Input‡	I	GPIO port B
G6	VSSCore			Core ground	Core ground
G7	VSSRTC			RTC ground	Real time clock ground
G8	DD[0]	1	Low	O	LCD serial display data
G9	D[3]	1	Low	I/O	Data I/O
G10	VSSRTC			RTC ground	Real time clock ground
G11	A[7]	1	Low	O	System byte address
G12	A[8]	1	Low	O	System byte address
G13	A[9]	1	Low	O	System byte address
G14	VSSIO			Pad ground	I/O ground
G15	D[12]	1	Low	I/O	Data I/O
G16	D[13]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H2	PA[5]	1	Input‡	I/O	GPIO port A
H3	VSSIO			Pad ground	I/O ground
H4	PA[4]	1	Input‡	I/O	GPIO port A
H5	PA[6]	1	Input‡	I/O	GPIO port A
H6	PB[0]	1	Input‡	I/O	GPIO port B
H7	PB[2]	1	Input‡	I/O	GPIO port B
H8	VSSRTC			RTC ground	Real time clock ground
H9	VSSRTC			RTC ground	Real time clock ground
H10	A[10]	1	Low	O	System byte address
H11	A[11]	1	Low	O	System byte address
H12	A[12]	1	Low	O	System byte address
H13	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
H14	VSSIO			Pad ground	I/O ground
H15	D[14]	1	Low	I/O	Data I/O
H16	D[15]	1	Low	I/O	Data I/O
J1	PA[3]	1	Input‡	I/O	GPIO port A
J2	PA[1]	1	Input‡	I/O	GPIO port A
J3	VSSIO			Pad ground	I/O ground
J4	PA[2]	1	Input‡	I/O	GPIO port A

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
55	Y4	N5	PD[5]	I/O	95
56	V5	R3	PD[4]	I/O	98
59	Y5	T4	PD[3]	I/O	101
60	V6	N6	PD[2]	I/O	104
61	W6	R4	PD[1]	I/O	107
62	Y6	L7	PD[0]/LEDFLSH	O	110
68	W8	T6	SSIRXFR	I/O	122
69	Y8	K8	ADCIN	I	125
70	V9	R6	nADCCS	O	126
75	W10	M8	DRIVE1	I/O	128
76	Y10	T8	DRIVE0	I/O	131
77	V11	N8	ADCCLK	O	134
78	W11	R8	ADCOUT	O	136
79	Y11	N9	SMPCLK	O	138
80	Y12	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	Y13	L9	COL6	O	144
85	W13	T10	COL5	O	146
86	V13	K9	COL4	O	148
87	Y14	R10	COL3	O	150
88	W14	N10	COL2	O	152
91	Y15	R11	COL1	O	154
92	W15	M10	COL0	O	156
93	V15	T12	BUZ	O	158
94	Y16	L10	D[31]	I/O	160
95	W16	R12	D[30]	I/O	163
96	V16	N11	D[29]	I/O	166
97	Y17	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	Y18	M11	D[27]	I/O	174
101	V17	T14	A[26]/DRA[1]	O	177
102	W18	N12	D[26]	I/O	179
103	Y19	R14	A[25]/DRA[2]	O	182
104	Y20	T15	D[25]	I/O	184
105	U18	N13	HALFWORD	O	187
106	V209	R16	A[24]/DRA[3]	O	189
109	U19	P15	D[24]	I/O	191

Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
155	E18	E13	nMEDCHG/nBROM	I	283
156	B20	B16	nURESET	I	284
161	B16	B14	WAKEUP	I	285
162	A16	D11	nPWRFL	I	286
163	C15	A13	A[6]	O	287
164	B15	F10	D[6]	I/O	289
165	A15	B13	A[5]	O	292
166	C14	E10	D[5]	I/O	294
169	B14	B12	A[4]	O	297
170	A14	D10	D[4]	I/O	299
171	C13	A11	A[3]	O	302
172	B13	G9	D[3]	I/O	304
173	A13	B11	A[2]	O	307
175	C12	A10	D[2]	I/O	309
176	B12	F9	A[1]	O	312
177	A12	B10	D[1]	I/O	314
178	C11	E9	A[0]	O	317
179	B11	A9	D[0]	I/O	319
184	B10	D8	CL2	O	322
185	A10	B8	CL1	O	324
186	A9	E8	FRM	O	326
187	B9	A7	M	O	328
188	C9	F8	DD[3]	O	330
189	A8	B7	DD[2]	O	333
191	B8	A6	DD[1]	O	336
192	C8	G8	DD[0]	O	339
193	A7	B6	nSDCS[1]	O	342
194	B7	D7	nSDCS[0]	O	344
195	C7	A5	SDQM[3]	I/O	346
196	A6	E7	SDQM[2]	I/O	349
199	B6	F7	SDCKE	I/O	352
200	C6	A4	SDCLK	I/O	355
201	A5	D6	nMWE/nSDWE	O	358
202	B5	B4	nMOE/nSDCAS	O	360
204	C5	E6	nCS[0]	O	362
205	A4	A3	nCS[1]	O	364

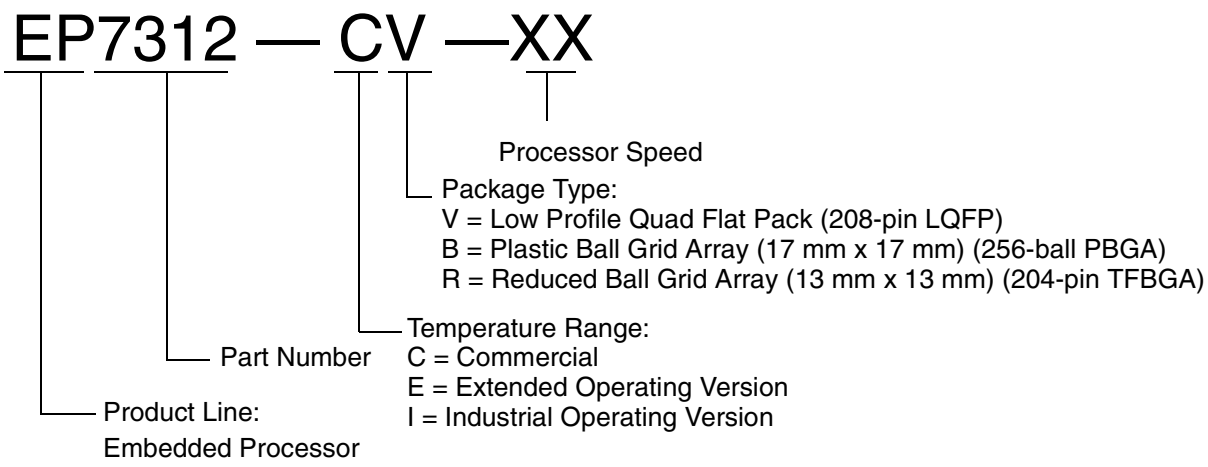
Ordering Information

Here is the list of EP7312 parts that are available:

- EP7312-CV
- EP7312-IV
- EP7312-CB
- EP7312-CR
- EP7312-CV-90
- EP7312-CB-90
- EP7312-CR-90
- EP7312-IB
- EP7312-IR
- EP7312-IV-90
- EP7312-IB-90
- EP7312-IR-90

Ordering Information Legend

Here is the legend for understanding the ordering information on page 1.



Note: Go to the Cirrus Logic Internet site at http://cirrus.com/corporate/contacts to find contact information for your local sales representative.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