Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g30f128g-e-qfn64r

- Data retention of the entire memory in EM0 to EM3

5.6 Device Information (DI) Page

The DI page contains calibration values, a unique identification number and other useful data. See the table below for a complete overview.

Table 5.4. Device Information Page Contents

DI Address	Register	Description
0x0FE08020	CMU_LFRCOCTRL	Register reset value.
0x0FE08028	CMU_HFRCOCTRL	Register reset value.
0x0FE08030	CMU_AUXHFRCOCTRL	Register reset value.
0x0FE08040	ADC0_CAL	Register reset value.
0x0FE08048	ADC0_BIASPROG	Register reset value.
0x0FE08050	DAC0_CAL	Register reset value.
0x0FE08058	DAC0_BIASPROG	Register reset value.
0x0FE08060	ACMP0_CTRL	Register reset value.
0x0FE08068	ACMP1_CTRL	Register reset value.
0x0FE08078	CMU_LCDCTRL	Register reset value.
0x0FE081B0	DI_CRC	[15:0]: DI data CRC-16.
0x0FE081B2	CAL_TEMP_0	[7:0] Calibration temperature (°C).
0x0FE081B4	ADC0_CAL_1V25	[14:8]: Gain for 1V25 reference, [6:0]: Offset for 1V25 reference.
0x0FE081B6	ADC0_CAL_2V5	[14:8]: Gain for 2V5 reference, [6:0]: Offset for 2V5 reference.
0x0FE081B8	ADC0_CAL_VDD	[14:8]: Gain for VDD reference, [6:0]: Offset for VDD reference.
0x0FE081BA	ADC0_CAL_5VDIFF	[14:8]: Gain for 5VDIFF reference, [6:0]: Offset for 5VDIFF reference.
0x0FE081BC	ADC0_CAL_2XVDD	[14:8]: Reserved (gain for this reference cannot be calibrated), [6:0]: Offset for 2XVDD reference.
0x0FE081BE	ADC0_TEMP_0_READ_1V25	[15:4] Temperature reading at 1V25 reference, [3:0] Reserved.
0x0FE081C8	DAC0_CAL_1V25	[22:16]: Gain for 1V25 reference, [13:8]: Channel 1 offset for 1V25 reference, [5:0]: Channel 0 offset for 1V25 reference.
0x0FE081CC	DAC0_CAL_2V5	[22:16]: Gain for 2V5 reference, [13:8]: Channel 1 offset for 2V5 reference, [5:0]: Channel 0 offset for 2V5 reference.
0x0FE081D0	DAC0_CAL_VDD	[22:16]: Reserved (gain for this reference cannot be calibrated), [13:8]: Channel 1 offset for VDD reference, [5:0]: Channel 0 offset for VDD reference.
0x0FE081D4	RESERVED	[31:0] Reserved
0x0FE081D8	RESERVED	[31:0] Reserved
0x0FE081DC	HFRCO_CALIB_BAND_1	[7:0]: Tuning for the 1.2 MHZ HFRCO band.
0x0FE081DD	HFRCO_CALIB_BAND_7	[7:0]: Tuning for the 6.6 MHZ HFRCO band.
0x0FE081DE	HFRCO_CALIB_BAND_11	[7:0]: Tuning for the 11 MHZ HFRCO band.

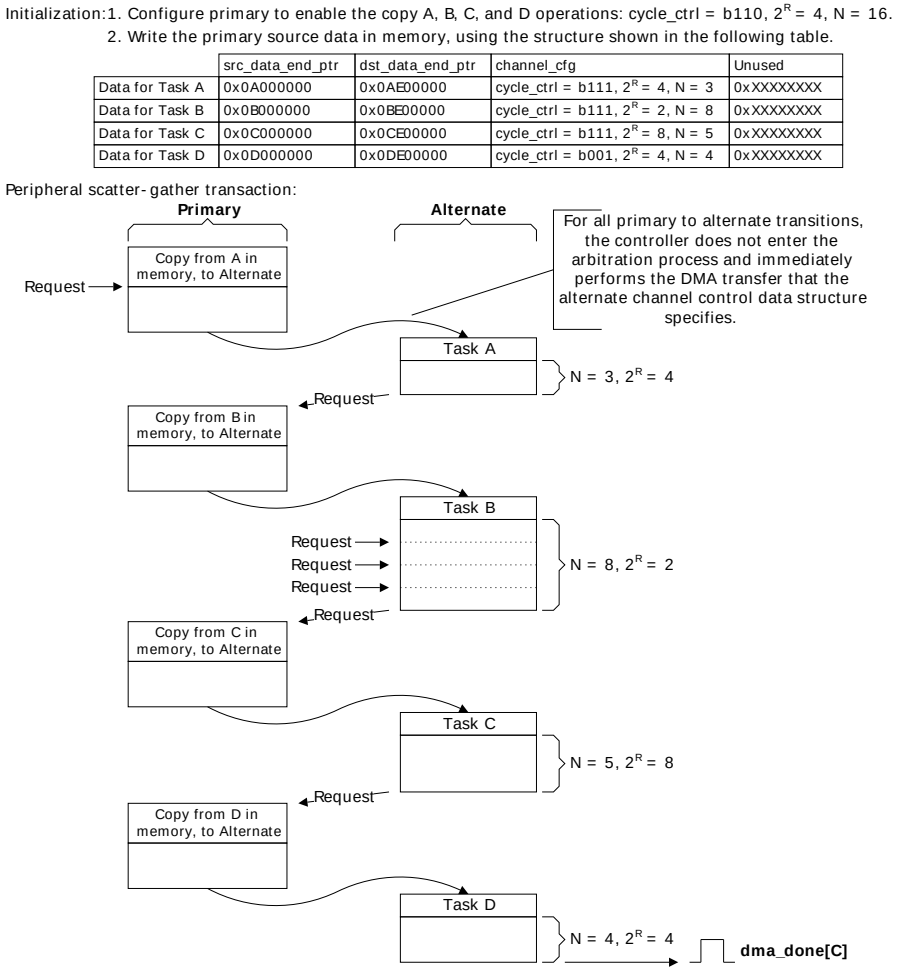
Bit	Field	Value	Description
[20:18]	src_prot_ctrl	-	Configures the state of HPROT when the controller reads the source data
[13:4]	n_minus_1	N [1]	Configures the controller to perform N DMA transfers, where N is a multiple of four
[3]	next_useburst	-	When set to 1, the controller sets the chnl_useburst_set [C] bit to 1 after the alternate transfer completes

[1]Because the R_power field is set to four, you must set N to be a multiple of four. The value given by N/4 is the number of times that you must configure the alternate data structure.

See Section 8.4.3.3 (p. 56) for more information.

Figure 8.5 (p. 52) shows a peripheral scatter-gather example.

Figure 8.5. Peripheral scatter-gather example



In Figure 8.5 (p. 52) :

Initialization

1. The host processor configures the primary data structure to operate in peripheral scatter-gather mode by setting cycle_ctrl to b110. Because a data structure for a single channel consists of four words then you must set 2^R to 4. In this example, there are four tasks and therefore N is set to 16.
2. The host processor writes the data structure for tasks A, B, C, and D to the memory locations that the primary src_data_end_ptr specifies.
3. The host processor enables the channel.

The peripheral scatter-gather transaction commences when the controller receives a request on `dma_req[]`. The transaction continues as follows:

Table 8.11 (p. 60) lists the destination addresses for a DMA transfer of 12 bytes using a halfword increment.

Table 8.11. DMA cycle of 12 bytes using a halfword increment

Initial values of channel_cfg, prior to the DMA cycle				
src_size = b00, dst_inc = b01, n_minus_1 = b1011, cycle_ctrl = 1, R_power = b11				
DMA transfers	End Pointer	Count	Difference [1]	Address
	0x5E7	11	0x16	0x5D1
	0x5E7	10	0x14	0x5D3
	0x5E7	9	0x12	0x5D5
	0x5E7	8	0x10	0x5D7
	0x5E7	7	0xE	0x5D9
	0x5E7	6	0xC	0x5DB
	0x5E7	5	0xA	0x5DD
	0x5E7	4	0x8	0x5DF
Values of channel_cfg after 2^R DMA transfers				
src_size = b00, dst_inc = b01, n_minus_1 = b011, cycle_ctrl = 1, R_power = b11				
DMA transfers	End Pointer	Count	Difference	Address
	0x5E7	3	0x6	0x5E1
	0x5E7	2	0x4	0x5E3
	0x5E7	1	0x2	0x5E5
	0x5E7	0	0x0	0x5E7
Final values of channel_cfg, after the DMA cycle				
src_size = b00, dst_inc = b01, n_minus_1 = 0, cycle_ctrl = 0 [2], R_power = b11				

[1] This value is the result of count being shifted left by the value of dst_inc.

[2] After the controller completes the DMA cycle it invalidates the channel_cfg memory location by clearing the cycle_ctrl field.

8.4.4 Interaction with the EMU

The DMA interacts with the Energy Management Unit (EMU) to allow transfers from , e.g., the LEUART to occur in EM2. The EMU can wake up the DMA sufficiently long to allow data transfers to occur. See section "DMA Support" in the LEUART documentation.

8.4.5 Interrupts

The PL230 dma_done[n:0] signals (one for each channel) as well as the dma_err signal, are available as interrupts to the Cortex-M3 core. They are combined into one interrupt vector, DMA_INT. If the interrupt for the DMA is enabled in the ARM Cortex-M3 core, an interrupt will be made if one or more of the interrupt flags in DMA_IF and their corresponding bits in DMA_IEN are set.

8.5 Examples

A basic example of how to program the DMA for transferring 42 bytes from the USART1 to memory location 0x20003420. Assumes that the channel 0 is currently disabled, and that the DMA_ALTCTRLBASE register has already been configured.

Example 8.1. DMA Transfer

1. Configure the channel select for using USART1 with DMA channel 0
   a. Write SOURCESEL=0b001101 and SIGSEL=XX to DMA_CHCTRL0
2. Configure the primary channel descriptor for DMA channel 0
   a. Write XX (read address of USART1) to src_data_end_ptr
   b. Write 0x20003420 + 40 to dst_data_end_ptr c
   c. Write these values to channel_cfg for channel 0:
      i. dst_inc=b01 (destination halfword address increment)
      ii. dst_size=b01 (halfword transfer size)
      iii. src_inc=b11 (no address increment for source)
      iv. src_size=01 (halfword transfer size)
      v. dst_prot_ctrl=000 (no cache/buffer/privilege)
      vi. src_prot_ctrl=000 (no cache/buffer/privilege)
      vii.R_power=b0000 (arbitrate after each DMA transfer)
      viiin_minus_1=d20 (transfer 21 halfwords)
      ix. next_useburst=b0 (not applicable)
      x. cycle_ctrl=b001 (basic operating mode)
3. Enable the DMA
   a. Write EN=1 to DMA_CONFIG
4. Disable the single requests for channel 0 (i.e., do not react to data available, wait for buffer full)
   a. Write DMA_CHUSEBURSTS[0]=1
5. Enable buffer-full requests for channel 0
   a. Write DMA_CHREQMASKC[0]=1
6. Use the primary data structure for channel 0
   a. Write DMA_CHALTC[0]=1
7. Enable channel 0
   a. Write DMA_CHENS[0]=1

8.7 Register Description

8.7.1 DMA_STATUS - DMA Status Registers

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x07													0x0							0
Access												R													R							R
Name												CHNUM													STATE							EN

Bit	Name	Reset	Access	Description
31:21	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
20:16	CHNUM	0x07	R	**Channel Number**
	Number of available DMA channels minus one.			
15:8	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
7:4	STATE	0x0	R	**Control Current State**
	State can be one of the following. Higher values (11-15) are undefined.			

Value	Mode	Description
0	IDLE	Idle
1	RDCHCTRLDATA	Reading channel controller data
2	RDSRCENDPTR	Reading source data end pointer
3	RDDSTENDPTR	Reading destination data end pointer
4	RDSRCDATA	Reading source data
5	WRDSTDATA	Writing destination data
6	WAITREQCLR	Waiting for DMA request to clear
7	WRCHCTRLDATA	Writing channel controller data
8	STALLED	Stalled
9	DONE	Done
10	PERSCATTRANS	Peripheral scatter-gather transition

3:1	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
0	EN	0	R	**DMA Enable Status**
	When this bit is 1, the DMA is enabled.			

8.7.2 DMA_CONFIG - DMA Configuration Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0					0
Access																											W					W
Name																											CHPROT					EN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
5	CHPROT	0	W	**Channel Protection Control**

Bit	Name	Reset	Access	Description
3:2	LFB	0x1	RW	**Clock Select for LFB**

Selects the clock source for LFBCLK.

LFB	LFBE	Mode	Description
0	0	Disabled	LFBCLK is disabled
1	0	LFRCO	LFRCO selected as LFBCLK
2	0	LFXO	LFXO selected as LFBCLK
3	0	HFCORECLKLEDIV2	$HFCORECLK_{LE}$ divided by two is selected as LFBCLK
0	1	ULFRCO	ULFRCO selected as LFBCLK

Bit	Name	Reset	Access	Description
1:0	LFA	0x1	RW	**Clock Select for LFA**

Selects the clock source for LFACLK.

LFA	LFAE	Mode	Description
0	0	Disabled	LFACLK is disabled
1	0	LFRCO	LFRCO selected as LFACLK
2	0	LFXO	LFXO selected as LFACLK
3	0	HFCORECLKLEDIV2	$HFCORECLK_{LE}$ divided by two is selected as LFACLK
0	1	ULFRCO	ULFRCO selected as LFACLK

11.5.12 CMU_STATUS - Status Register

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0	0	0	0	1	0	0	0	0	0	0	0	0	1	1
Access																		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Name																		CALBSY	LFXOSEL	LFRCOSEL	HFXOSEL	HFRCOSEL	LFXORDY	LFXOENS	LFRCORDY	LFRCOENS	AUXHFRCORDY	AUXHFRCOENS	HFXORDY	HFXOENS	HFRCORDY	HFRCOENS

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
14	CALBSY	0	R	**Calibration Busy**
	Calibration is on-going.			
13	LFXOSEL	0	R	**LFXO Selected**
	LFXO is selected as HFCLK clock source.			
12	LFRCOSEL	0	R	**LFRCO Selected**
	LFRCO is selected as HFCLK clock source.			
11	HFXOSEL	0	R	**HFXO Selected**
	HFXO is selected as HFCLK clock source.			
10	HFRCOSEL	1	R	**HFRCO Selected**
	HFRCO is selected as HFCLK clock source.			
9	LFXORDY	0	R	**LFXO Ready**
	LFXO is enabled and start-up time has exceeded.			
8	LFXOENS	0	R	**LFXO Enable Status**
	LFXO is enabled.			
7	LFRCORDY	0	R	**LFRCO Ready**

14.5.31 EBI_TFTTIMING - TFT Timing Register

Offset	Bit Position																														
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0				0x0			0x000												0x000										
Access			RW				RW			RW												RW										
Name			TFTHOLD				TFTSETUP			TFTSTART												DCLKPERIOD										

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
29:28	TFTHOLD	0x0	RW	**TFT Hold Time**
	Sets the number of internal clock cycles the RGB data is held after the active edge of EBI_DCLK.			
27:26	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
25:24	TFTSETUP	0x0	RW	**TFT Setup Time**
	Sets the number of internal clock cycles the RGB data is driven before the active edge of EBI_DCLK.			
23	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
22:12	TFTSTART	0x000	RW	**TFT Direct Drive Transaction Start**
	Sets the starting position of the External Direct Drive Transaction relative to the DCLK inactive edge.			
11	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
10:0	DCLKPERIOD	0x000	RW	**TFT Direct Drive Transaction (EBI_DCLK) Period**
	Sets the Direct Drive transaction (EBI_DCLK) period in internal cycles. Set to required cycle count minus 1.			

14.5.32 EBI_TFTPOLARITY - TFT Polarity Register

Offset	Bit Position																														
0x07C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0	0	0	0	0
Access																												RW	RW	RW	RW	RW
Name																												VSYNCPOL	HSYNCPOL	DATAENPOL	DCLKPOL	CSPOL

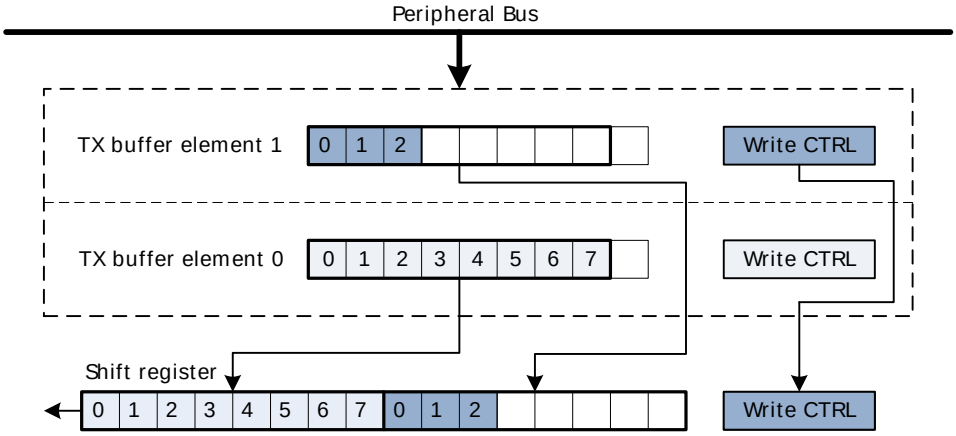
Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
4	VSYNCPOL	0	RW	**VSYNC Polarity**
	Sets the polarity of the EBI_VSYNC line.			

Value	Mode	Description
0	ACTIVELOW	VSYNC is active low.
1	ACTIVEHIGH	VSYNC is active high.

Bit	Name	Reset	Access	Description
3	HSYNCPOL	0	RW	**Address Latch Polarity**
	Sets the polarity of the EBI_HSYNC line.			

Value	Mode	Description
0	ACTIVELOW	HSYNC is active low.

Figure 16.9. USART Transmission of Large Frames



As shown in Figure 16.9 (p. 220) , frame transmission control bits are taken from the second element in FIFO.

The two buffer elements can be written at the same time using the USARTn_TXDOUBLE or USARTn_TXDOUBLEX register. The TXDATAX0 bitfield then refers to buffer element 0, and TXDATAX1 refers to buffer element 1.

Figure 16.10. USART Transmission of Large Frames, MSBF

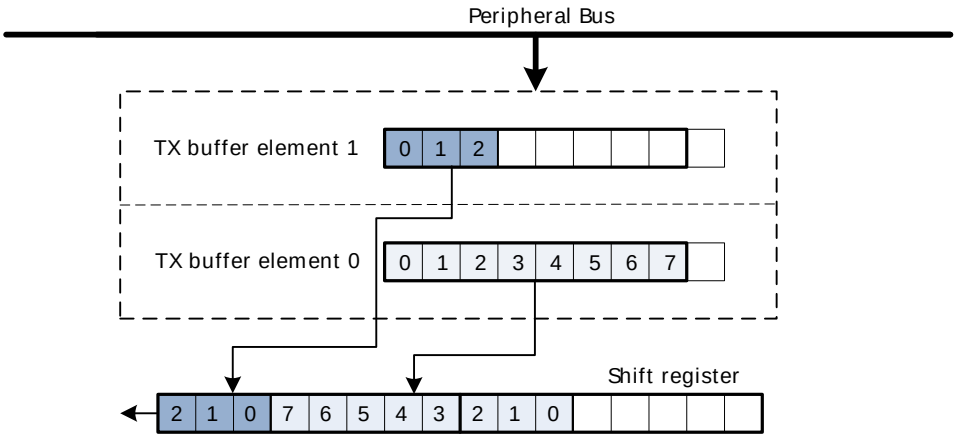


Figure 16.10 (p. 220) illustrates the order of the transmitted bits when an 11 bit frame is transmitted with MSBF set. If MSBF is set and the frame is smaller than 10 bits, only the contents of transmit buffer 0 will be transmitted.

When receiving a large frame, BYTESWAP in USARTn_CTRL determines the order the way the large frame is split into the two buffer elements. If BYTESWAP is cleared, the least significant 8 bits of the received frame are loaded into the first element of the receive buffer, and the remaining bits are loaded into the second element, as shown in Figure 16.11 (p. 221) . The first byte read from the buffer thus contains the 8 least significant bits. Set BYTESWAP to reverse the order.

The status bits are loaded into both elements of the receive buffer. The frame is not moved from the receive shift register before there are two free spaces in the receive buffer.

Bit	Name	Reset	Access	Description
7:4	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
3:0	DATABITS	0x5	RW	**Data-Bit Mode**

This register sets the number of data bits in a USART frame.

Value	Mode	Description
1	FOUR	Each frame contains 4 data bits
2	FIVE	Each frame contains 5 data bits
3	SIX	Each frame contains 6 data bits
4	SEVEN	Each frame contains 7 data bits
5	EIGHT	Each frame contains 8 data bits
6	NINE	Each frame contains 9 data bits
7	TEN	Each frame contains 10 data bits
8	ELEVEN	Each frame contains 11 data bits
9	TWELVE	Each frame contains 12 data bits
10	THIRTEEN	Each frame contains 13 data bits
11	FOURTEEN	Each frame contains 14 data bits
12	FIFTEEN	Each frame contains 15 data bits
13	SIXTEEN	Each frame contains 16 data bits

16.5.3 USARTn_TRIGCTRL - USART Trigger Control register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0	0			0x0	
Access																											RW	RW			RW	
Name																											TXTEN	RXTEN			TSEL	

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
5	TXTEN	0	RW	**Transmit Trigger Enable**

When set, the PRS channel selected by TSEL sets TXEN, enabling the transmitter on positive trigger edges.

4	RXTEN	0	RW	**Receive Trigger Enable**

When set, the PRS channel selected by TSEL sets RXEN, enabling the receiver on positive trigger edges.

3	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
2:0	TSEL	0x0	RW	**Trigger PRS Channel Select**

Select USART PRS trigger channel. The PRS signal can enable RX and/or TX, depending on the setting of RXTEN and TXTEN.

Value	Mode	Description
0	PRSCH0	PRS Channel 0 selected
1	PRSCH1	PRS Channel 1 selected
2	PRSCH2	PRS Channel 2 selected
3	PRSCH3	PRS Channel 3 selected
4	PRSCH4	PRS Channel 4 selected
5	PRSCH5	PRS Channel 5 selected
6	PRSCH6	PRS Channel 6 selected
7	PRSCH7	PRS Channel 7 selected

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x00							
Access																									W							
Name																									TXDATA							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
7:0	TXDATA	0x00	W	**TX Data**
	This frame will be added to the transmit buffer. Only 8 LSB can be written using this register. 9th bit and control bits will be cleared.			

18.5.12 LEUARTn_IF - Interrupt Flag Register

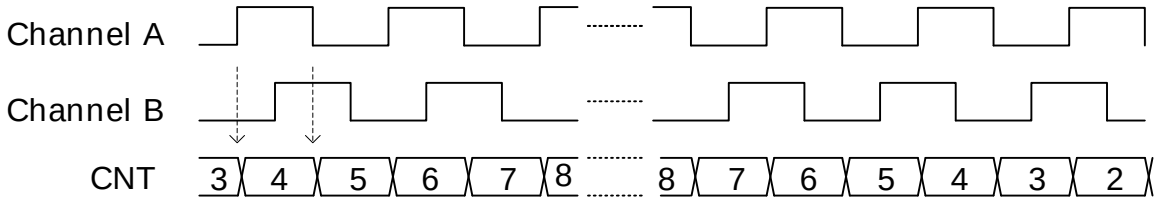
Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																						0	0	0	0	0	0	0	0	0	1	0
Access																						R	R	R	R	R	R	R	R	R	R	R
Name																						SIGF	STARTF	MPAF	FERR	PERR	TXOF	RXUF	RXOF	RXDATAV	TXBL	TXC

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
10	SIGF	0	R	**Signal Frame Interrupt Flag**
	Set when a signal frame is detected.			
9	STARTF	0	R	**Start Frame Interrupt Flag**
	Set when a start frame is detected.			
8	MPAF	0	R	**Multi-Processor Address Frame Interrupt Flag**
	Set when a multi-processor address frame is detected.			
7	FERR	0	R	**Framing Error Interrupt Flag**
	Set when a frame with a framing error is received while RXBLOCK is cleared.			
6	PERR	0	R	**Parity Error Interrupt Flag**
	Set when a frame with a parity error is received while RXBLOCK is cleared.			
5	TXOF	0	R	**TX Overflow Interrupt Flag**
	Set when a write is done to the transmit buffer while it is full. The data already in the transmit buffer is preserved.			
4	RXUF	0	R	**RX Underflow Interrupt Flag**
	Set when trying to read from the receive buffer when it is empty.			
3	RXOF	0	R	**RX Overflow Interrupt Flag**
	Set when data is incoming while the receive shift register is full. The data previously in shift register is overwritten by the new data.			
2	RXDATAV	0	R	**RX Data Valid Interrupt Flag**
	Set when data becomes available in the receive buffer.			
1	TXBL	1	R	**TX Buffer Level Interrupt Flag**
	Set when space becomes available in the transmit buffer for a new frame.			

Table 19.1. TIMER Counter Response in X2 Decoding Mode

Channel B	Channel A	
	Rising	Falling
0	Increment	Decrement
1	Decrement	Increment

Figure 19.8. TIMER X2 Decoding Mode



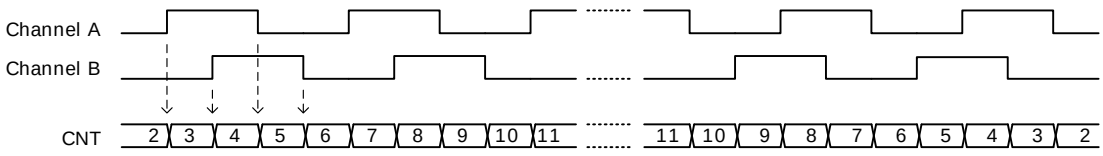
19.3.1.6.2 X4 Decoding Mode

In X4 Decoding mode, the counter increments or decrements on every edge of Channel A and Channel B, see Figure 19.9 (p. 280) and Table 19.2 (p. 280) .

Table 19.2. TIMER Counter Response in X4 Decoding Mode

Opposite Channel	Channel A		Channel B	
	Rising	Falling	Rising	Falling
Channel A = 0			Decrement	Increment
Channel A = 1			Increment	Decrement
Channel B = 0	Increment	Decrement		
Channel B = 1	Decrement	Increment		

Figure 19.9. TIMER X4 Decoding Mode



19.3.1.6.3 TIMER Rotational Position

To calculate a position Equation 19.1 (p. 280) can be used.

TIMER Rotational Position Equation

$$pos° = (CNT/X \times N) \times 360° \quad (19.1)$$

where X = Encoding type and N = Number of pulses per revolution.

19.3.2 Compare/Capture Channels

The Timer contains 3 Compare/Capture channels, which can be configured in the following modes:

19.5 Register Description

19.5.1 TIMERn_CTRL - Control Register

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0										0x0						0x0		0x0		0	0	0	0	0		0x0	
Access					RW										RW						RW		RW		RW	RW	RW	RW	RW		RW	
Name					PRESC										CLKSEL						FALLA		RISEA		DMACLRACT	DEBUGRUN	QDM	OSMEN	SYNC		MODE	

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
27:24	PRESC	0x0	RW	**Prescaler Setting**

These bits select the prescaling factor.

Value	Mode	Description
0	DIV1	The HFPERCLK is undivided
1	DIV2	The HFPERCLK is divided by 2
2	DIV4	The HFPERCLK is divided by 4
3	DIV8	The HFPERCLK is divided by 8
4	DIV16	The HFPERCLK is divided by 16
5	DIV32	The HFPERCLK is divided by 32
6	DIV64	The HFPERCLK is divided by 64
7	DIV128	The HFPERCLK is divided by 128
8	DIV256	The HFPERCLK is divided by 256
9	DIV512	The HFPERCLK is divided by 512
10	DIV1024	The HFPERCLK is divided by 1024

23:18	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
17:16	CLKSEL	0x0	RW	**Clock Source Select**

These bits select the clock source for the timer.

Value	Mode	Description
0	PRESCHFPERCLK	Prescaled HFPERCLK
1	CC1	Compare/Capture Channel 1 Input
2	TIMEROUF	Timer is clocked by underflow(down-count) or overflow(up-count) in the lower numbered neighbor Timer

15:12	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
11:10	FALLA	0x0	RW	**Timer Falling Input Edge Action**

These bits select the action taken in the counter when a falling edge occurs on the input.

Value	Mode	Description
0	NONE	No action
1	START	Start counter without reload
2	STOP	Stop counter without reload
3	RELOADSTART	Reload and start counter

9:8	RISEA	0x0	RW	**Timer Rising Input Edge Action**

These bits select the action taken in the counter when a rising edge occurs on the input.

Value	Mode	Description
0	NONE	No action
1	START	Start counter without reload
2	STOP	Stop counter without reload

Bit	Name	Reset	Access	Description
1	DTPRS1FC	0	W1	**DTI PRS1 Fault Clear**
	Write 1 to this bit to clear PRS 1 fault.			
0	DTPRS0FC	0	W1	**DTI PRS0 Fault Clear**
	Write 1 to this bit to clear PRS 0 fault.			

19.5.22 TIMERn_DTLOCK - DTI Configuration Lock Register

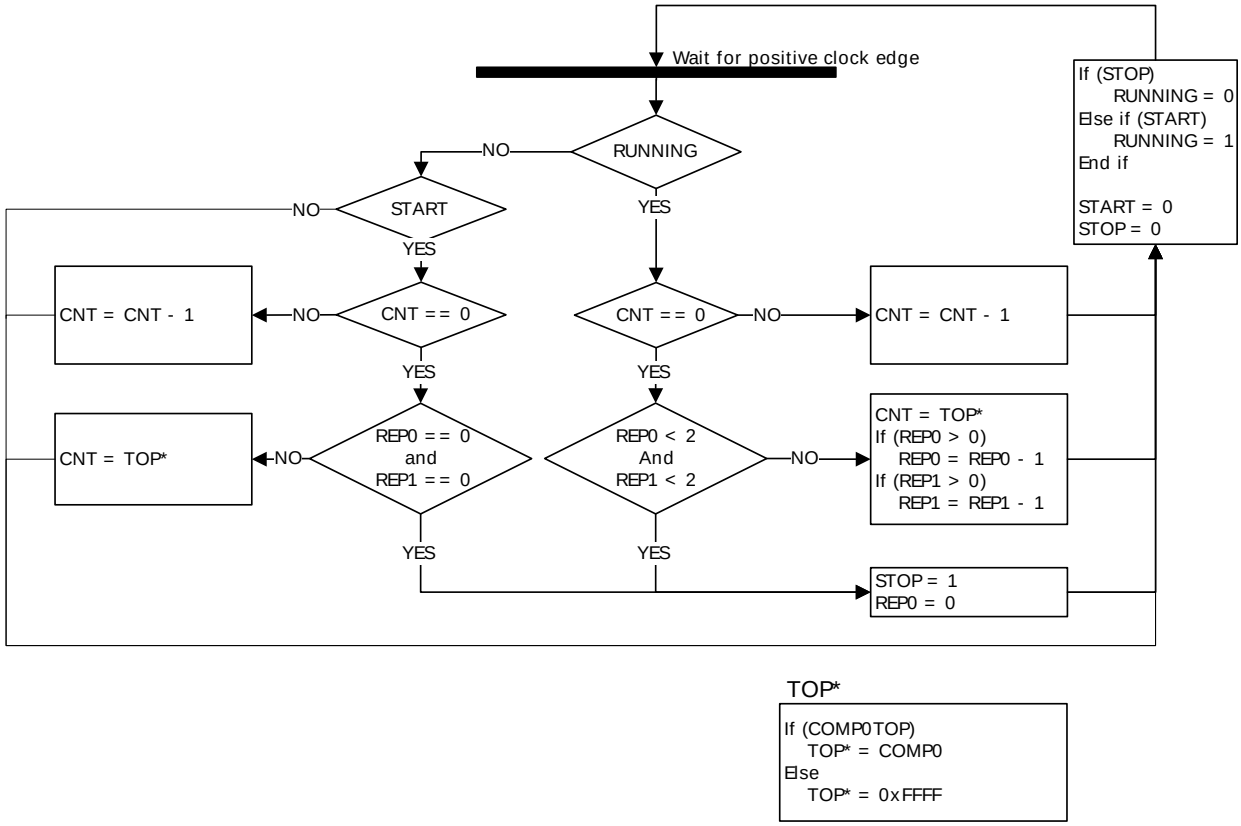
Offset	Bit Position																													
0x088	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0000															
Access																	RW															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
15:0	LOCKKEY	0x0000	RW	**DTI Lock Key**

Write any other value than the unlock code to lock TIMER0_ROUTE, TIMER0_DTCTRL, TIMER0_DTTIME and TIMER0_DTFC from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled.

Mode	Value	Description
Read Operation		
UNLOCKED	0	TIMER DTI registers are unlocked
LOCKED	1	TIMER DTI registers are locked
Write Operation		
LOCK	0	Lock TIMER DTI registers
UNLOCK	0xCE80	Unlock TIMER DTI registers

Figure 21.5. LETIMER Double Repeat State Machine



21.3.3.3 Clock Source

The LETIMER clock source and its prescaler value are defined in the Clock Management Unit (CMU). The $LFACLK_{LETIMERn}$ has a frequency given by Equation 21.1 (p. 325) .

LETIMER Clock Frequency

$$f_{LFACKL\_LETIMERn} = 32.768/2^{LETIMERn} \quad (21.1)$$

where the exponent LETIMERn is a 4 bit value in the CMU_LFAPRESC0 register.

To use this module, the LE interface clock must be enabled in CMU_HFCORECLKEN0, in addition to the module clock.

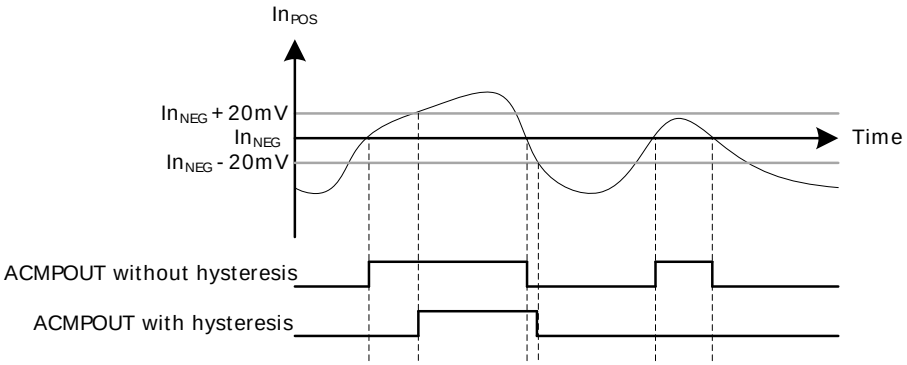
21.3.3.4 RTC Trigger

The LETIMER can be configured to start on compare match events from the Real Time Counter (RTC). If RTCC0TEN in LETIMERn_CTRL is set, the LETIMER will start on a compare match on RTC compare channel 0. In the same way, RTCC1TEN in LETIMERn_CTRL enables the LETIMER to start on a compare match with RTC compare channel 1.

Note

The LETIMER can only use compare match events from the RTC if the LETIMER runs at a higher than or equal frequency than the RTC. Also, if the LETIMER runs at twice the frequency of the RTC, a compare match event in the RTC will trigger the LETIMER twice. Four times the frequency gives four consecutive triggers, etc. The LETIMER will only

Figure 23.2. 20 mV Hysteresis Selected



23.3.4 Input Selection

The POSSEL and NEGSEL fields in ACMPn_INPUTSEL controls which signals are connected to the two inputs of the comparator. 8 external pins are available for both the negative and positive input. For the negative input, 3 additional internal reference sources are available; 1.25 V bandgap, 2.5V bandgap and V_{DD}. The V_{DD} reference can be scaled by a configurable factor, which is set in VDDLEVEL (in ACMPn_INPUTSEL) according to the following formula:

V_{DD} Scaled

$$V_{DD\_SCALED} = V_{DD} \times VDDLEVEL/63 \quad (23.1)$$

A low power reference mode can be enabled by setting the LPREF bit in ACMPn_INPUTSEL. In this mode, the power consumption in the reference buffer (V_{DD} and bandgap) is lowered at the cost of accuracy. Low power mode will only save power if V_{DD} with VDDLEVEL higher than 0 or a bandgap reference is selected.

Normally the analog comparator input mux is disabled when the EN (in ACMPn_CTRL) bit is set low. However if the MUXEN bit in ACMPn_CTRL is set, the mux is enabled regardless of the EN bit. This will minimize kickback noise on the mux inputs when the EN bit is toggled.

23.3.5 Capacitive Sense Mode

The analog comparator includes specialized hardware for capacitive sensing of passive push buttons. Such buttons are traces on PCB laid out in a way that creates a parasitic capacitor between the button and the ground node. Because a human finger will have a small intrinsic capacitance to ground, the capacitance of the button will increase when the button is touched. The capacitance is measured by including the capacitor in a free-running RC oscillator (see Figure 23.3 (p. 358)). The frequency produced will decrease when the button is touched compared to when it is not touched. By measuring the output frequency with a timer (e.g. through PRS), the change in capacitance can be calculated.

The analog comparator contains a complete feedback loop including an optional internal resistor. This resistor is enabled by setting the CSRESEN bit in ACMPn_INPUTSEL. The resistance can be set to one of four values by configuring the CSRESSEL bits in ACMPn_INPUTSEL. If the internal resistor is not enabled, the circuit will be open. The capacitive sense mode is enabled by setting the NEGSEL field in ACMPn_INPUTSEL to CAPSENSE. The input pin is selected through the POSSEL bits in ACMPn_INPUTSEL. The scaled V_{DD} in Figure 23.3 (p. 358) can be altered by configuring the VDDLEVEL in ACMPn_INPUTSEL. It is recommended to set the hysteresis (HYSTSEL in ACMPn_CTRL) higher than the lowest level when using the analog comparator in capacitive sense mode.

25.5.7 ADCn_IF - Interrupt Flag Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0	0							0	0
Access																							R	R							R	R
Name																							SCANOF	SINGLEOF							SCAN	SINGLE

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
9	SCANOF	0	R	**Scan Result Overflow Interrupt Flag**
	Indicates scan result overflow when this bit is set.			
8	SINGLEOF	0	R	**Single Result Overflow Interrupt Flag**
	Indicates single result overflow when this bit is set.			
7:2	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
1	SCAN	0	R	**Scan Conversion Complete Interrupt Flag**
	Indicates scan conversion complete when this bit is set.			
0	SINGLE	0	R	**Single Conversion Complete Interrupt Flag**
	Indicates single conversion complete when this bit is set.			

25.5.8 ADCn_IFS - Interrupt Flag Set Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0	0							0	0
Access																							W1	W1							W1	W1
Name																							SCANOF	SINGLEOF							SCAN	SINGLE

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
9	SCANOF	0	W1	**Scan Result Overflow Interrupt Flag Set**
	Write to 1 to set scan result overflow interrupt flag			
8	SINGLEOF	0	W1	**Single Result Overflow Interrupt Flag Set**
	Write to 1 to set single result overflow interrupt flag.			
7:2	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
1	SCAN	0	W1	**Scan Conversion Complete Interrupt Flag Set**
	Write to 1 to set scan conversion complete interrupt flag.			
0	SINGLE	0	W1	**Single Conversion Complete Interrupt Flag Set**
	Write to 1 to set single conversion complete interrupt flag.			

26.5.5 DACn_IEN - Interrupt Enable Register

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0	0			0	0
Access																											RW	RW			RW	RW
Name																											CH1UF	CH0UF			CH1	CH0

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
5	CH1UF	0	RW	**Channel 1 Conversion Data Underflow Interrupt Enable**
	Enable/disable channel 1 data underflow interrupt.			
4	CH0UF	0	RW	**Channel 0 Conversion Data Underflow Interrupt Enable**
	Enable/disable channel 0 data underflow interrupt.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
1	CH1	0	RW	**Channel 1 Conversion Complete Interrupt Enable**
	Enable/disable channel 1 conversion complete interrupt.			
0	CH0	0	RW	**Channel 0 Conversion Complete Interrupt Enable**
	Enable/disable channel 0 conversion complete interrupt.			

26.5.6 DACn_IF - Interrupt Flag Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0	0			0	0
Access																											R	R			R	R
Name																											CH1UF	CH0UF			CH1	CH0

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
5	CH1UF	0	R	**Channel 1 Data Underflow Interrupt Flag**
	Indicates channel 1 data underflow.			
4	CH0UF	0	R	**Channel 0 Data Underflow Interrupt Flag**
	Indicates channel 0 data underflow.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
1	CH1	0	R	**Channel 1 Conversion Complete Interrupt Flag**
	Indicates channel 1 conversion complete and that new data can be written to the data register.			
0	CH0	0	R	**Channel 0 Conversion Complete Interrupt Flag**
	Indicates channel 0 conversion complete and that new data can be written to the data register.			

Bit	Name	Reset	Access	Description
31:0	XORDATA	0x00000000	RW	**XOR Data Access**
	Access data with XOR function through this register.			

27.5.10 AES_KEYLA - KEY Low Register

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Access	RW																															
Name	KEYLA																															

Bit	Name	Reset	Access	Description
31:0	KEYLA	0x00000000	RW	**Key Low Access A**
	Access the low key words through this register.			

27.5.11 AES_KEYLB - KEY Low Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Access	RW																															
Name	KEYLB																															

Bit	Name	Reset	Access	Description
31:0	KEYLB	0x00000000	RW	**Key Low Access B**
	Access the low key words through this register.			

Abbreviation	Description
LEUART	Low Energy Universal Asynchronous Receiver Transmitter
LFRCO	Low Frequency RC Oscillator
LFXO	Low Frequency Crystal Oscillator
LS	Low-speed
MAC	Media Access Controller
NVIC	Nested Vector Interrupt Controller
OSR	Oversampling Ratio
OTG	On-the-go
PCNT	Pulse Counter
PHY	Physical Layer
PRS	Peripheral Reflex System
PWM	Pulse Width Modulation
RC	Resistance and Capacitance
RMU	Reset Management Unit
RTC	Real Time Clock
SAR	Successive Approximation Register
SOF	Start of Frame
SPI	Serial Peripheral Interface
SW	Software
UART	Universal Asynchronous Receiver Transmitter
USART	Universal Synchronous Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCMP	Voltage supply Comparator
WDOG	Watchdog timer
XTAL	Crystal