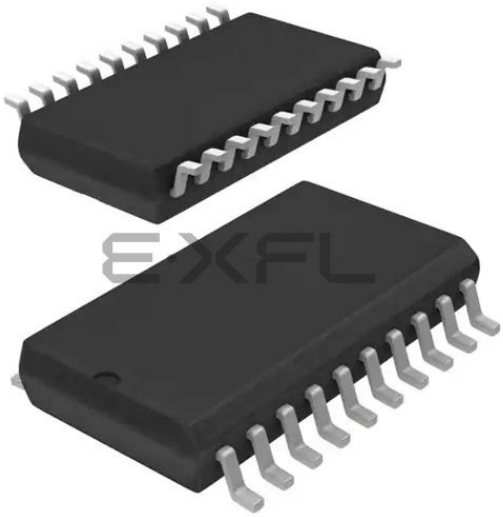

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903f3m3tr

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Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals or to synchronize with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break
-

4.11 TIM5 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM6

4.12 TIM6 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM5.

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complementary outputs	Ext. trigger	Timer synchronization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	Yes
TIM5	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM6	8	Any power of 2 from 1 to 128	Up	0	0	No	

5.3 TSSOP20, SO20 and UFQFPN20 pin descriptions

Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions

TSSOP20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext.	High sink(1)	Speed	OD	PP			
4	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 52 channel 3	SPI master/ slave select [AFR1]/ UART1 data transmit [AFR1:0]
11	8	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)		**Port B5**	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)		**Port B4**	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3/TLI/ [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
14	11	PC4/ TIM1_CH4/ CLK_CCO/AIN2/ [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7]
15	12	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	15	PD1/ SWIM(4)	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.1 Alternate function remapping bits

Table 13. STM8S903K3 alternate function remapping bits [7:2] for 32-pin packages

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate functions.(2) 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N. **AFR6** Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port D7 alternate function = TIM1_CH4. **AFR5** Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = CLK_CCO. **AFR4** Alternate function remapping option 4 0: AFR4 remapping option inactive: Default alternate functions.(2) 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. **AFR3** Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function.(2) 1: Port C3 alternate function = TLI. **AFR2** Alternate function remapping option 2 0: AFR2 remapping option inactive: Default alternate functions.(2) 1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3; port D4 alternate function = UART1_CK

1. Do not use more than one remapping option in the same port.

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

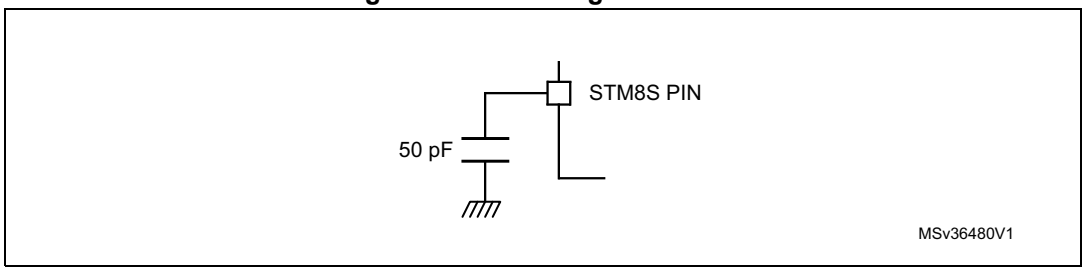
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

Figure 8. Pin loading conditions



10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 14. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz

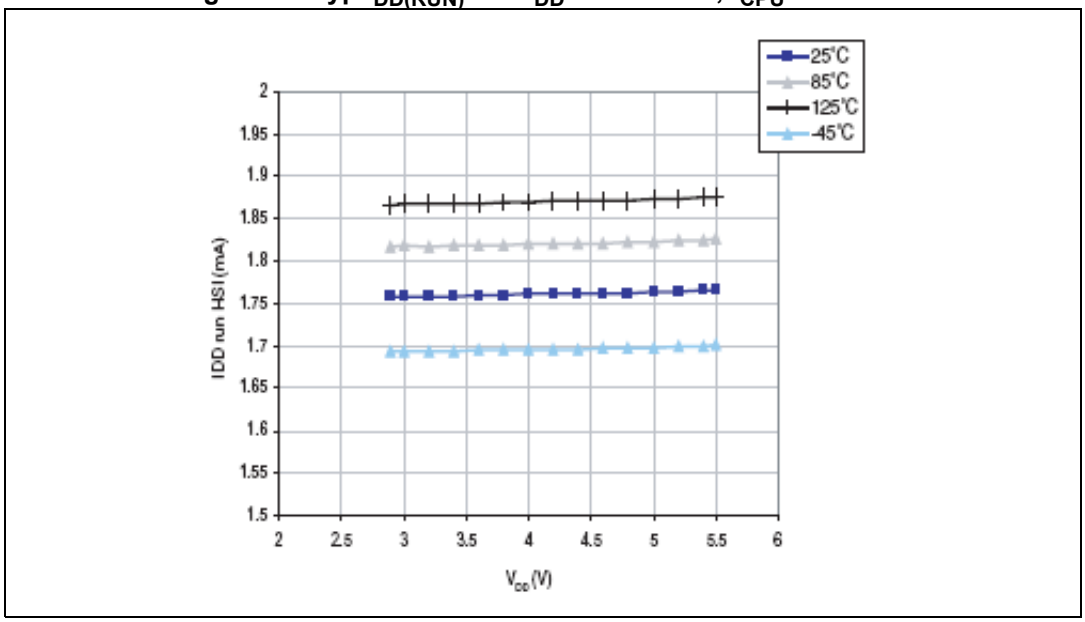


Figure 15. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE external clock, f_{CPU} = 16 MHz

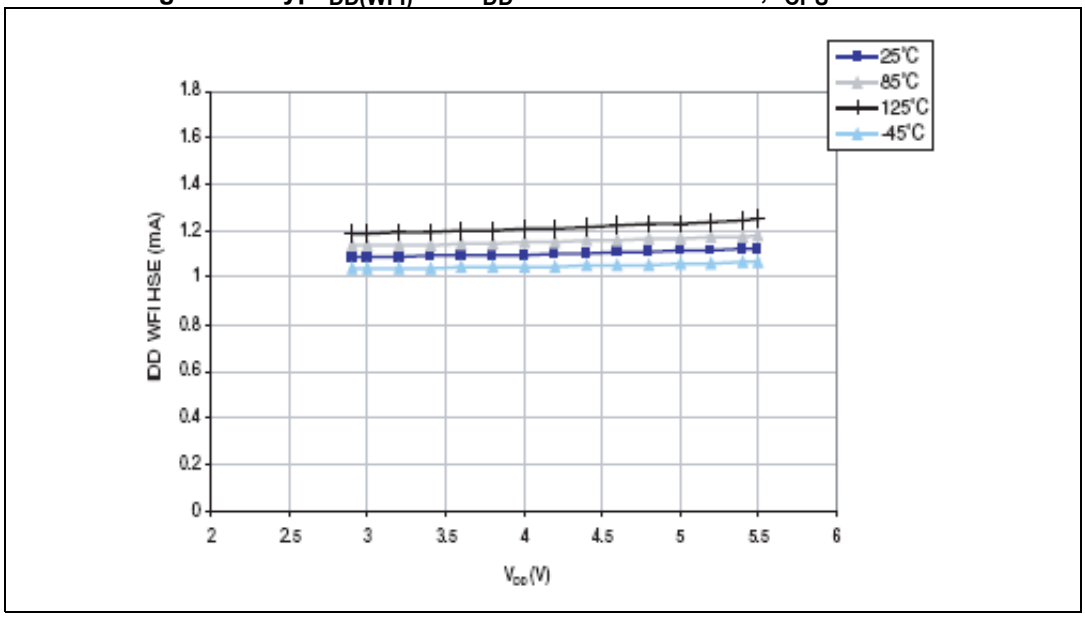
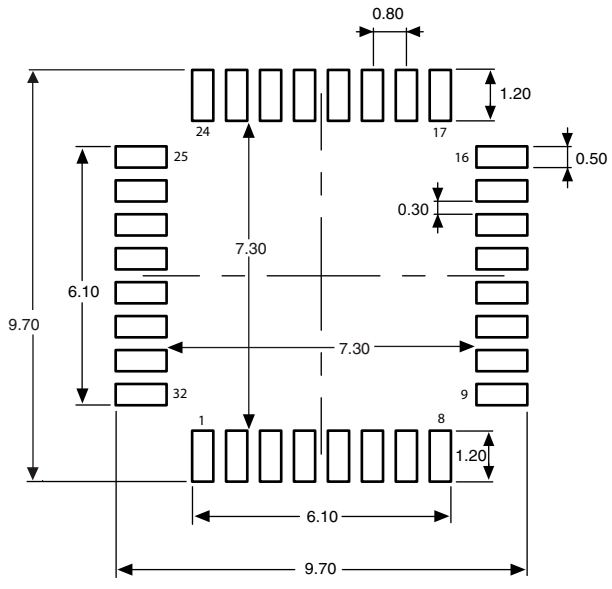


Table 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

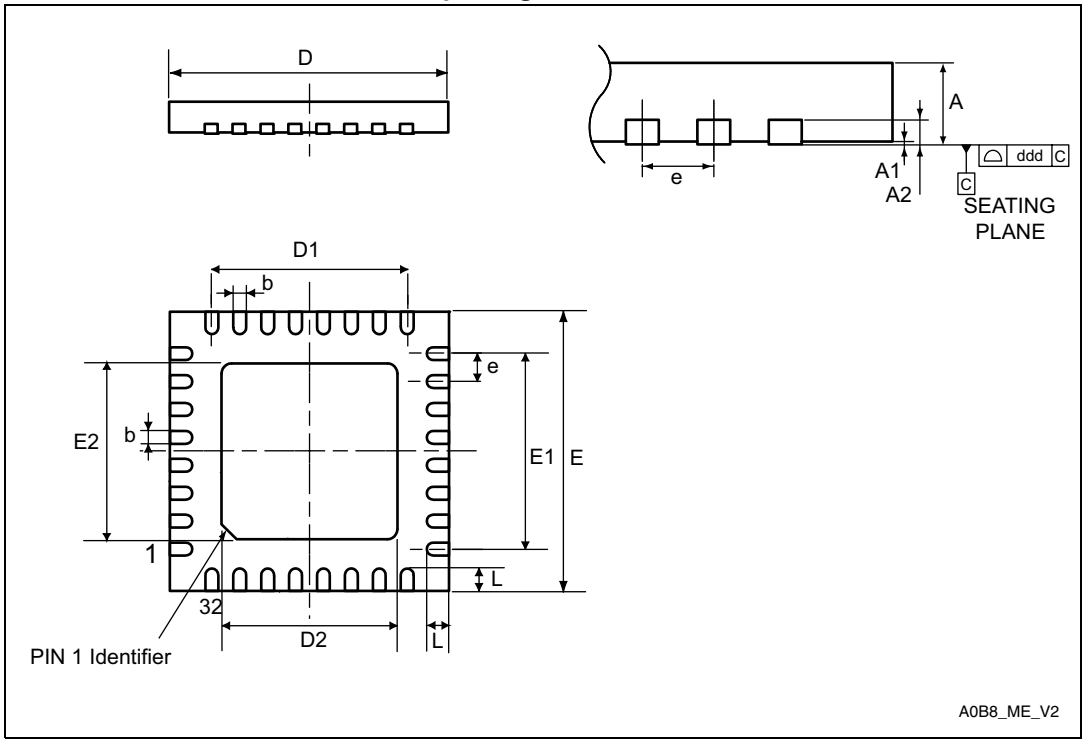
Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.2 UFQFPN32 package information

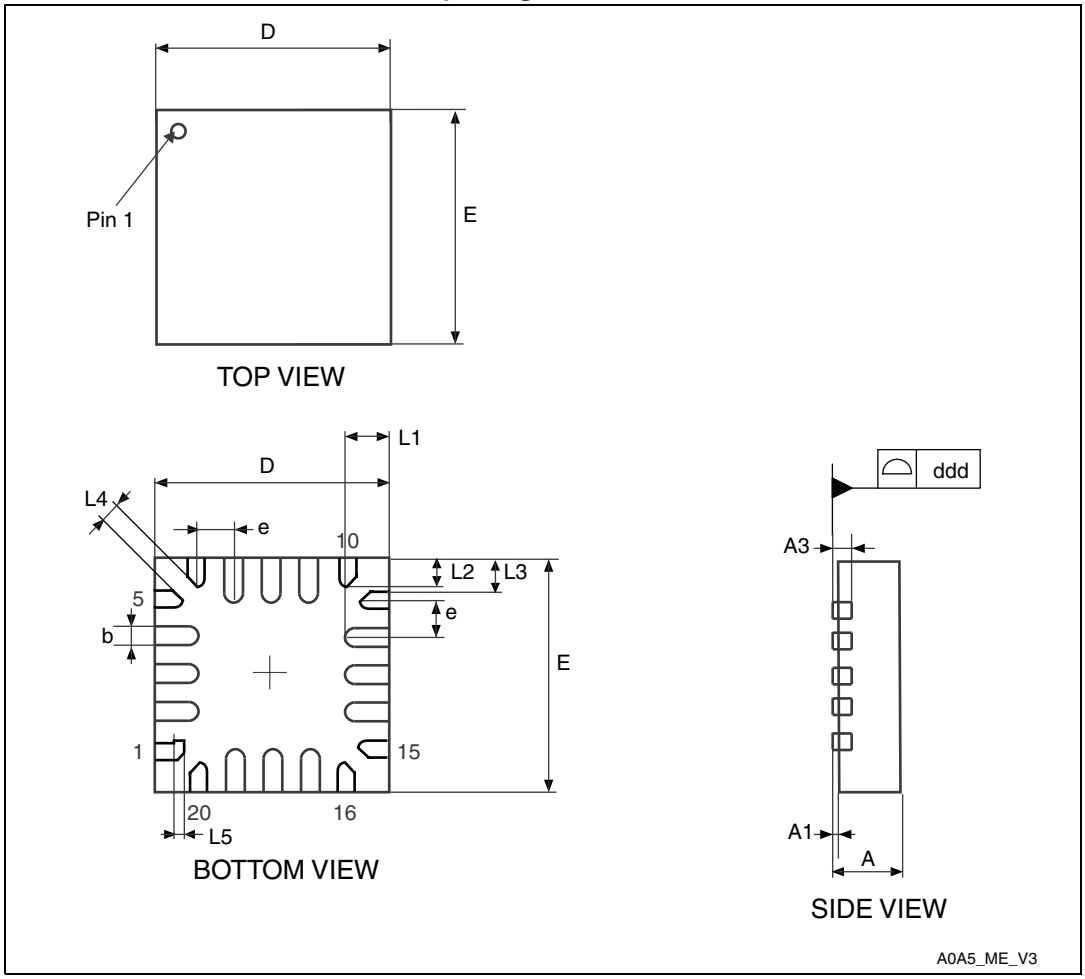
Figure 48. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

11.3 UFQFPN20 package information

Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

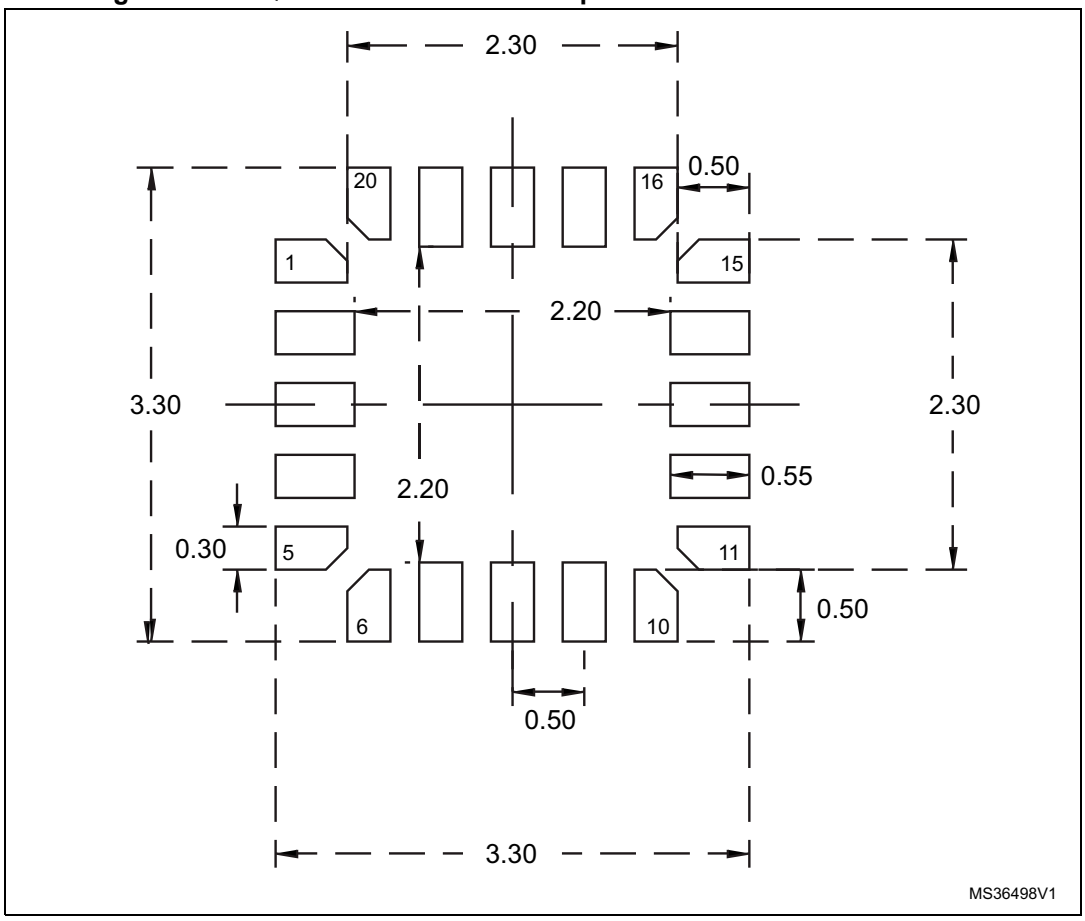


1. Drawing is not to scale.

Table 56. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

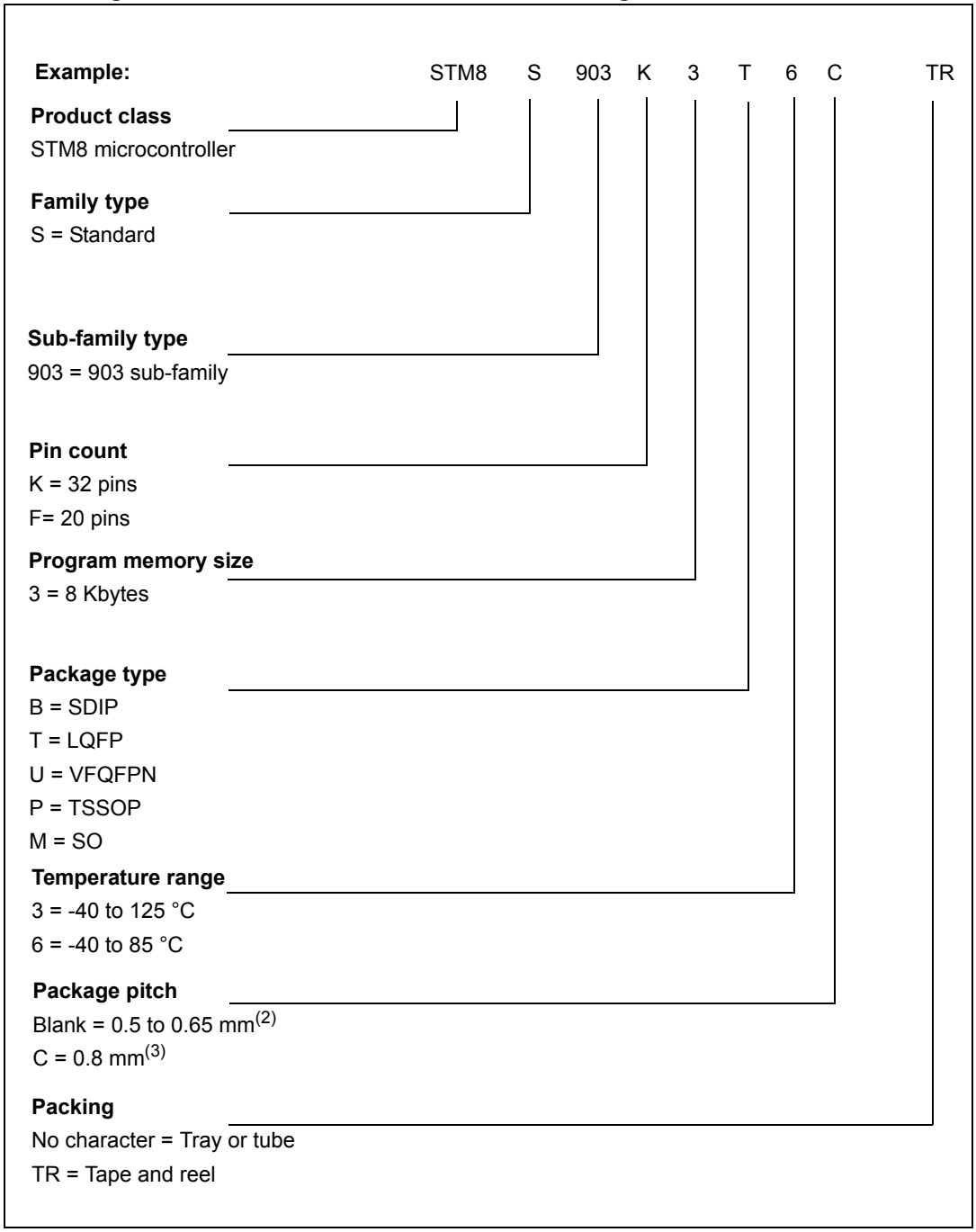
Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

Figure 62. UFQFPN recommended footprint without on-board emulation



13 Ordering information

Figure 63. STM8S903K3/F3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP903K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

13.1 STM8S903K3/F3 FASTROM microcontroller option list

(last update: April 2010)

Customer	.....
Address	.....
Contact	.....
Phone number	.....
FASTROM code reference(1)	.....

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .Hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Device type/memory size/package (check only one option)

FASTROM device	8 Kbyte
TSSOP20	[ ] STM8S903F3
SO20W	[ ] STM8S903F3
UFQFPN20	[ ] STM8S903F3
LQFP32	[ ] STM8S903K3
UFQFPN32	[ ] STM8S903K3

Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

LQFP32: 2 lines of 7 characters max: "_ _ _ _ _ _ _" and "_ _ _ _ _ _ _"
TSSOP20: 1 line of 10 characters max: "_ _ _ _ _ _ _ _ _ _"
SO20: 1 line of 13 characters max: "_ _ _ _ _ _ _ _ _ _ _ _ _"
UFQFPN32: 1 line of 7 characters max: "_ _ _ _ _ _ _"
UFQFPN20: 1 line of 4 characters max: "_ _ _ _"

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for the STM8 programming.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

15 Revision history

Table 61. Document revision history

Date	Revision	Changes
30-Apr-2009	1	Initial release.
03-Jun-2009	2	– Added bullet point concerning unique identifier to *Features* section on cover page. – Highlighted internal reference voltage in *Section 4.13: Analog-to-digital converter (ADC1)*. – Updated wpu and PP status of PB5/12C_SDA[TIM1_BKIN] and PB4/12C_SCL[ADC_ETR] pins in *Section 5: Pinouts and pin descriptions*. – Updated *Section 6.1: Memory map*. – Added *Section 9: Unique ID*. – Added TBD values to *Table 45: SPI characteristics*. – Added max values to *Table 48: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 49: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*.

Table 61. Document revision history (continued)

Date	Revision	Changes
08-Sep-2010	5	Removed VFQFPN32 package. Updated the definition for reset state in *Table 4: Legend/abbreviations for pinout tables* Updated pins 13/25/20, 14/26/21, 19/32/27, 1/2/29, 2/3/30, and 3/4/31; added footnote to PD1/SWIM pin in *Table 6: STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions*. Standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Changed the caption of *Table 13: STM8S903K3 alternate function remapping bits [7:2] for 32-pin packages*. Added *Table 14: STM8S903F3 alternate function remapping bits [7:2] for 20-pin packages*. Changed the caption of *Table 15: STM8S903K3 alternate function remapping bits [1:0] for 32-pin packages*. Added *Table 16: STM8S903F3 alternate function remapping bits [1:0] for 20-pin packages*. Replaced 0.01 µF with 0.1 µF in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram*. Updated footnote 1 in *Table 48: ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V* and *Table 49: ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V*. Updated existing footnote and added three additional footnotes to *Table 55: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*. Updated the special marking and OPT2 alternate function remapping sections in *Section 13.1: STM8S903K3/F3 FASTROM microcontroller option list*.

Table 61. Document revision history (continued)

Date	Revision	Changes
23-Feb-2015	9	Updated: – *Section 11.5: TSSOP20 package information* – *Section 11.3: UFQFPN20 package information*. Added: – Figure 46: LQFP32 recommended footprint – *Figure 47: LQFP32 marking example (package top view)* – *Figure 50: UFQFPN32 marking example (package top view)* – *Figure 53: UFQFPN20 marking example (package top view)* – *Figure 55: SDIP32 marking example (package top view)* – *Figure 57: TSSOP20 recommended package footprint* – *Figure 58: TSSOP20 marking example (package top view)* – *Figure 60: SO20 marking example (package top view)*

Table 61. Document revision history (continued)

Date	Revision	Changes
26-Mar-2015	10	Corrected the values for “b” dimensions in *Table 55: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.
13-Feb-2017	11	Updated: – Analog to digital converter (ADC) features on *Section : Features* – *Section 10.2: Absolute maximum ratings* – *Table 5: TSSOP20/SO20/UFQFPN20 pin descriptions* – *Table 19: Current characteristics* – *Table 33: Peripheral current consumption* – *Table 47: ADC characteristics* – *Table 56: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data* – *Figure 18: HSE external clock source* – *Figure 19: HSE oscillator circuit diagram* – *Figure 40: SPI timing diagram where slave mode and CPHA = 1* – *Figure 41: SPI timing diagram - master mode* – *Figure 44: Typical application with ADC* – *Section : Electromagnetic interference (EMI)* – All “Device marking” sections on *Section 11: Package information* – Footnotes on the tables of *Section 10: Electrical characteristics* and of *Figure 48: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline* – Title of *Table 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data* and *Table 56: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data* – Title of *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*, *Figure 46: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* Added: – *Figure 52: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*