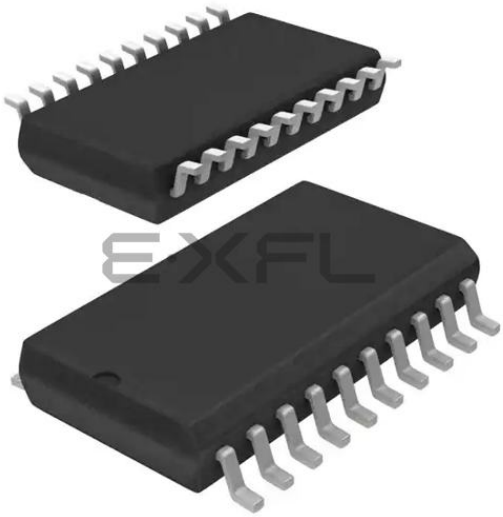

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903f3m6

List of tables

2 Description

The STM8S903K3/F3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

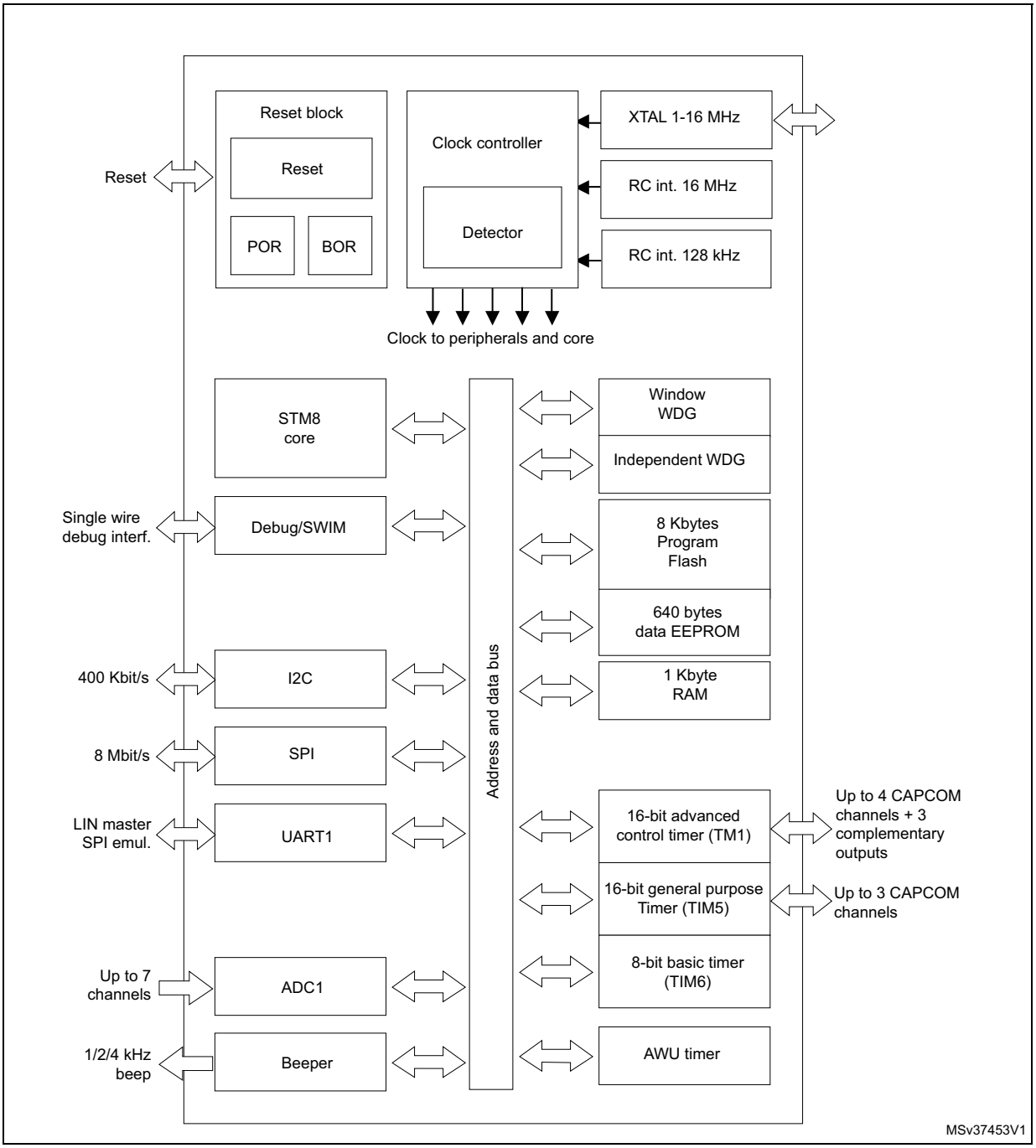
Table 1. STM8S903K3/F3 access line features

Device	STM8S903K3	STM8S903F3
Pin count	32	20
Maximum number of GPIOs (I/Os)	28(1)	16(2)
Ext. interrupt pins	28	16
Timer CAPCOM channels	7	
Timer complementary outputs	3	2
A/D converter channels	7	5
High sink I/Os	21	12
Low density Flash program memory (bytes)	8K	
Data EEPROM (bytes)	640(3)	
RAM (bytes)	1K	
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM5), 8-bit timer (TIM6)	

1. Including 21 high-sink outputs
2. Including 12 high-sink outputs
3. No read-while-write (RWW) capability.

3 Block diagram

Figure 1. STM8S903K3/F3 block diagram



4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels,
- 32 interrupt vectors with hardware priority,
- Up to 28 external interrupts on 7 vectors including TLI,
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 8 Kbyte of Flash program single voltage Flash memory,
- 640 byte true data EEPROM,
- User option byte area.

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (fCPU/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (fCPU/16)

LIN master mode

- Emission: Generates 13-bit synch. break frame
- Reception: Detects 11-bit break frame

4.14.2 SPI

- Maximum speed: 8 Mbit/s (fMASTER/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.3 I^2C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

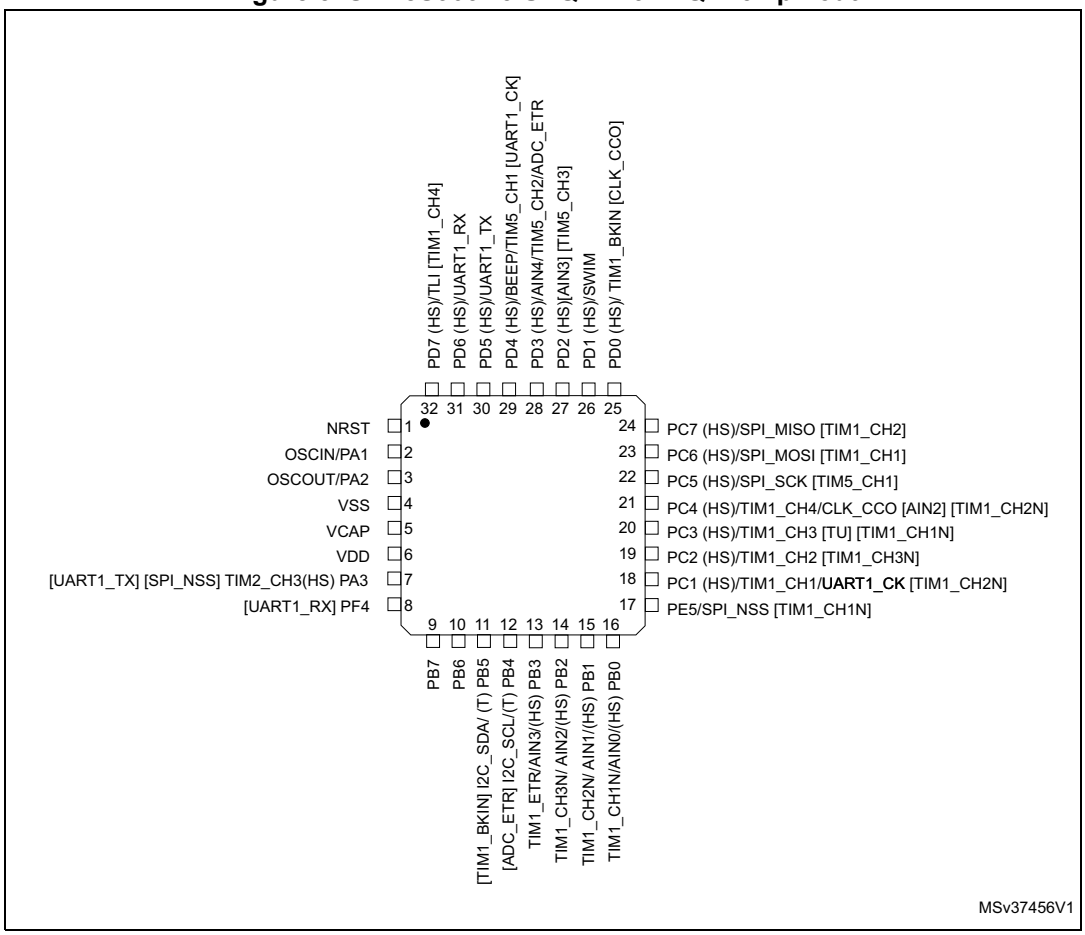
5.3 TSSOP20, SO20 and UFQFPN20 pin descriptions

Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions

TSSOP20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext.	High sink(1)	Speed	OD	PP			
4	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 52 channel 3	SPI master/ slave select [AFR1]/ UART1 data transmit [AFR1:0]
11	8	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)		**Port B5**	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)		**Port B4**	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3/TLI/ [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
14	11	PC4/ TIM1_CH4/ CLK_CCO/AIN2/ [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7]
15	12	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	15	PD1/ SWIM(4)	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-

5.4 STM8S903K3 UFQFPN32/LQFP32 and SDIP32 pinouts

Figure 5. STM8S903K3 UFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
4	31	PD6/ AIN6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
5	32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10: Electrical characteristics*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Total current consumption in wait mode

Table 25. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 26. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption in halt mode

Table 29. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20	55	

1. Guaranteed by characterization results.

Table 30. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low power mode wakeup times

Table 31. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See note(3)	µs
$t_{WU(WFI)}$	Wakeup time from run mode(2)	f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	3(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	48(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in power-down mode(5)	HSI (after wakeup)	50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in power-down mode(5)			54	-	

1. Guaranteed by characterization results.

Figure 12. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

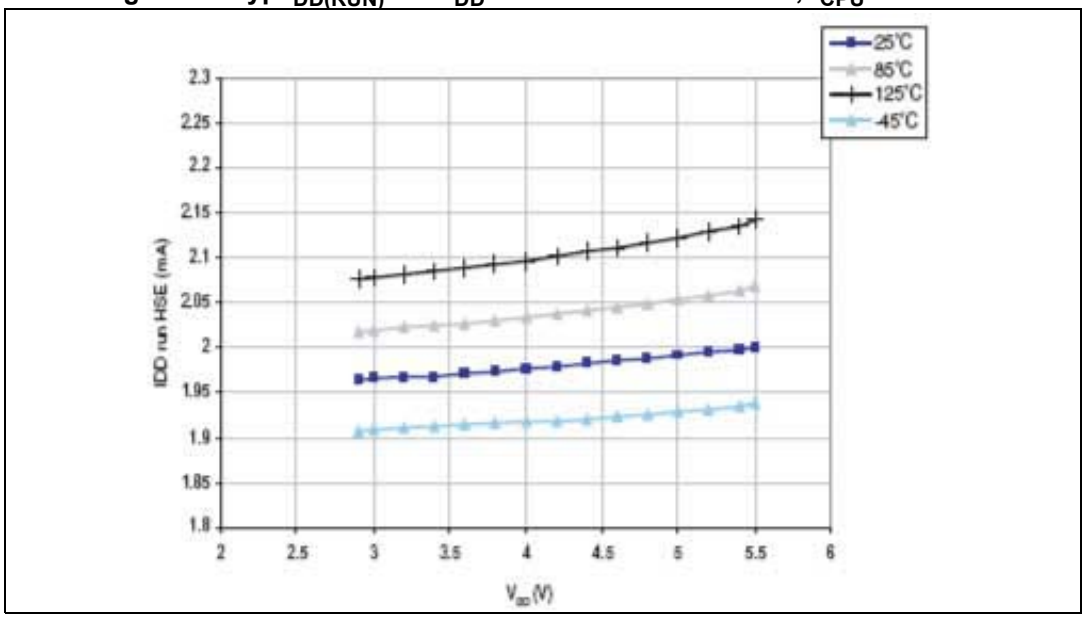


Figure 13. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

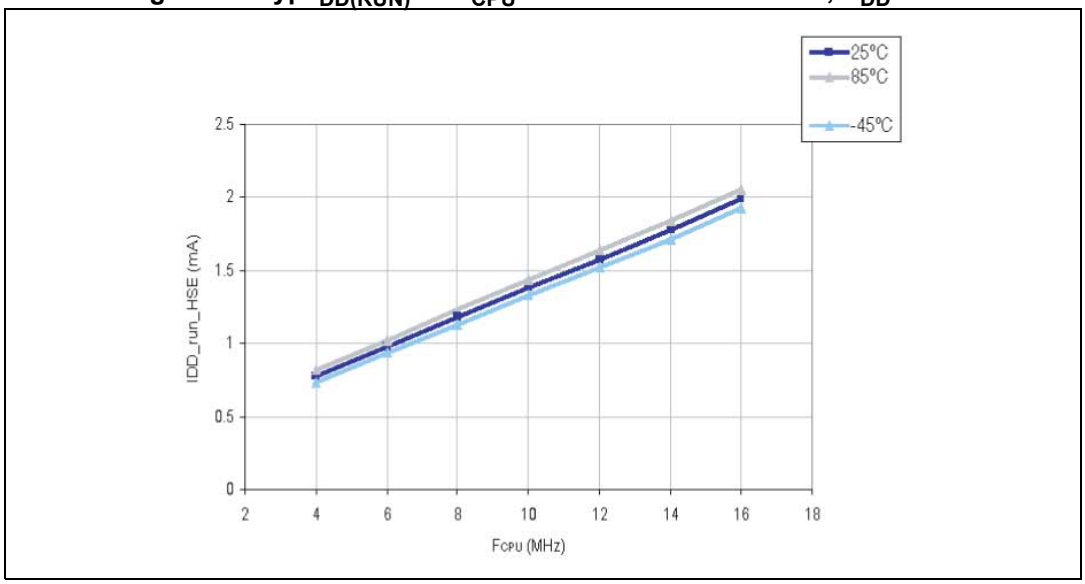


Figure 16. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, V_{DD} = 5 V

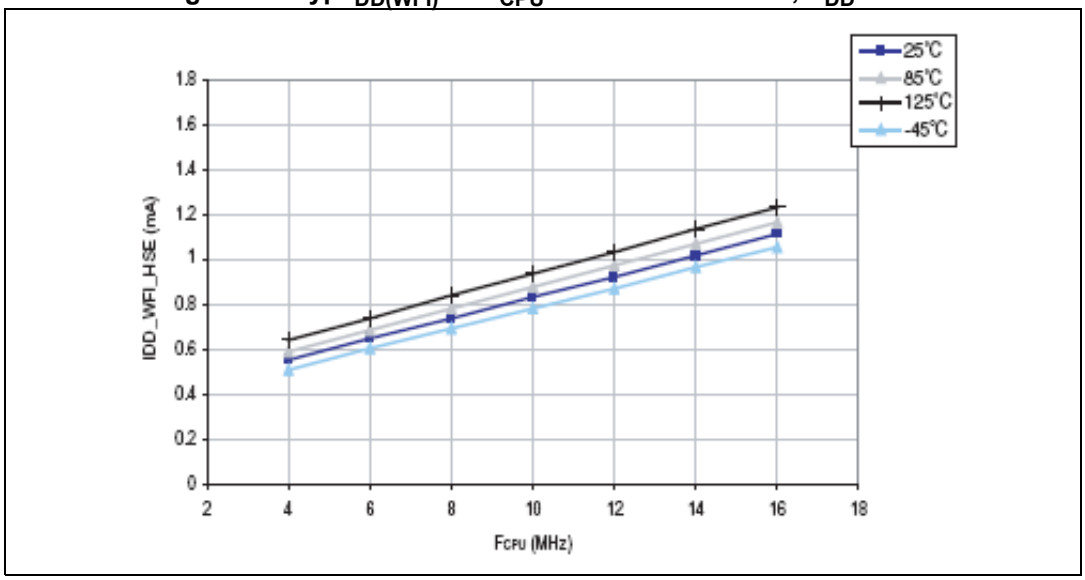
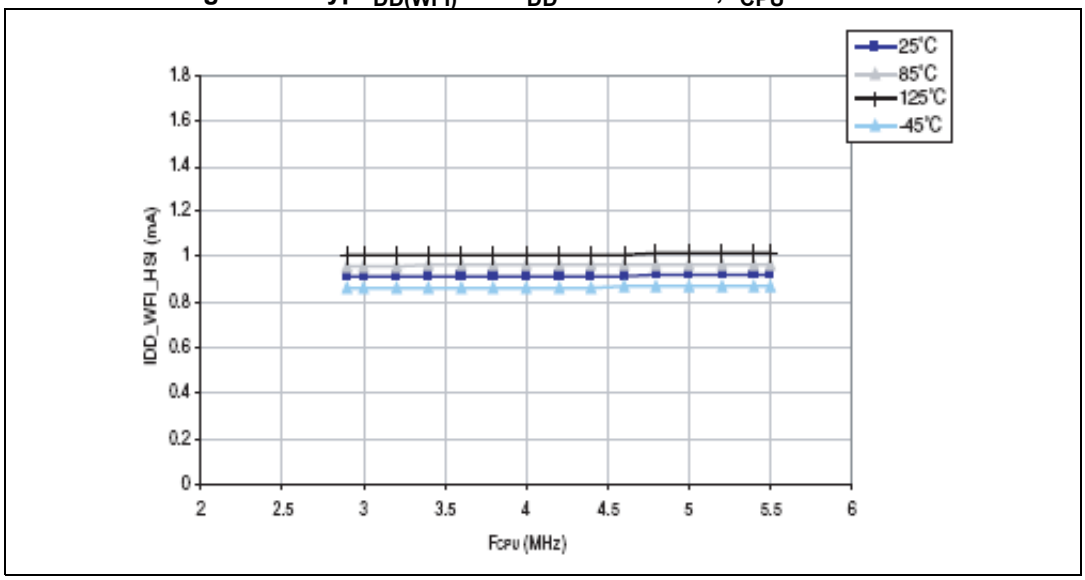


Figure 17. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



10.3.3 External clock sources and timing characteristics

HSE user external clock

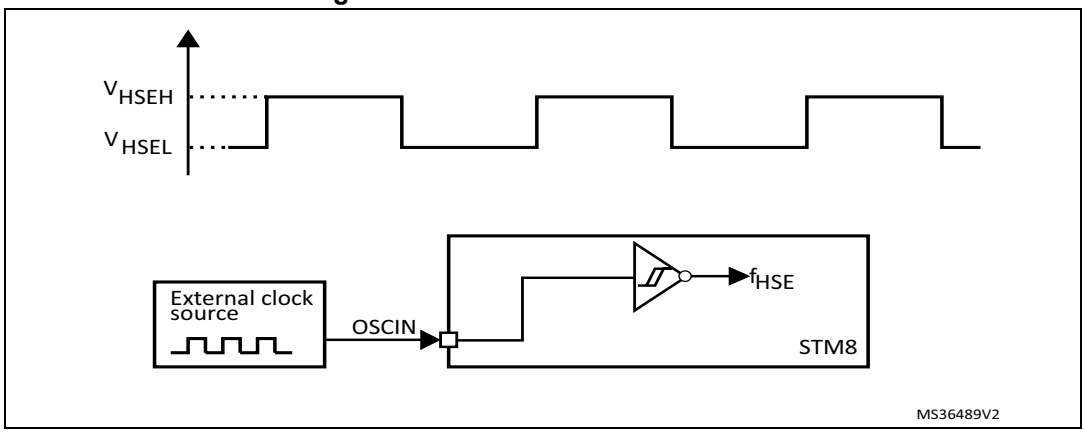
Subject to general operating conditions for V_{DD} and T_A.

Table 34. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 35. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)(3)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

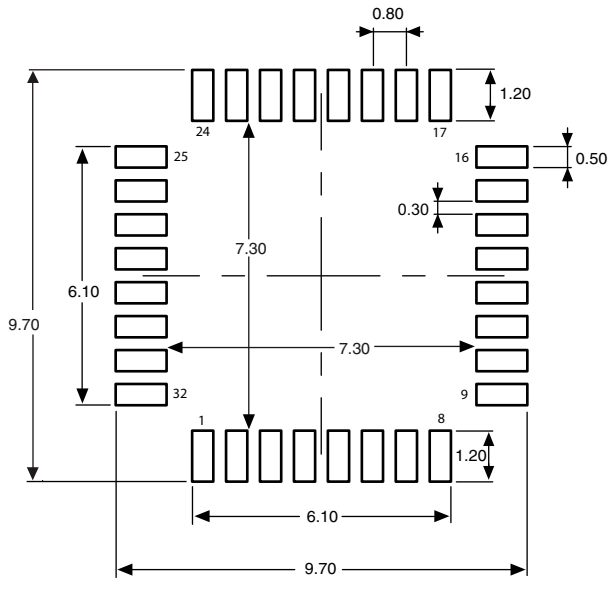
1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Table 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 21: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 60. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4.4mm	110	°C/W
	Thermal resistance junction-ambient SO20W (300 mils)	20	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	101	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm	38	
	Thermal resistance junction-ambient SDIP32 - 400 mils	60	

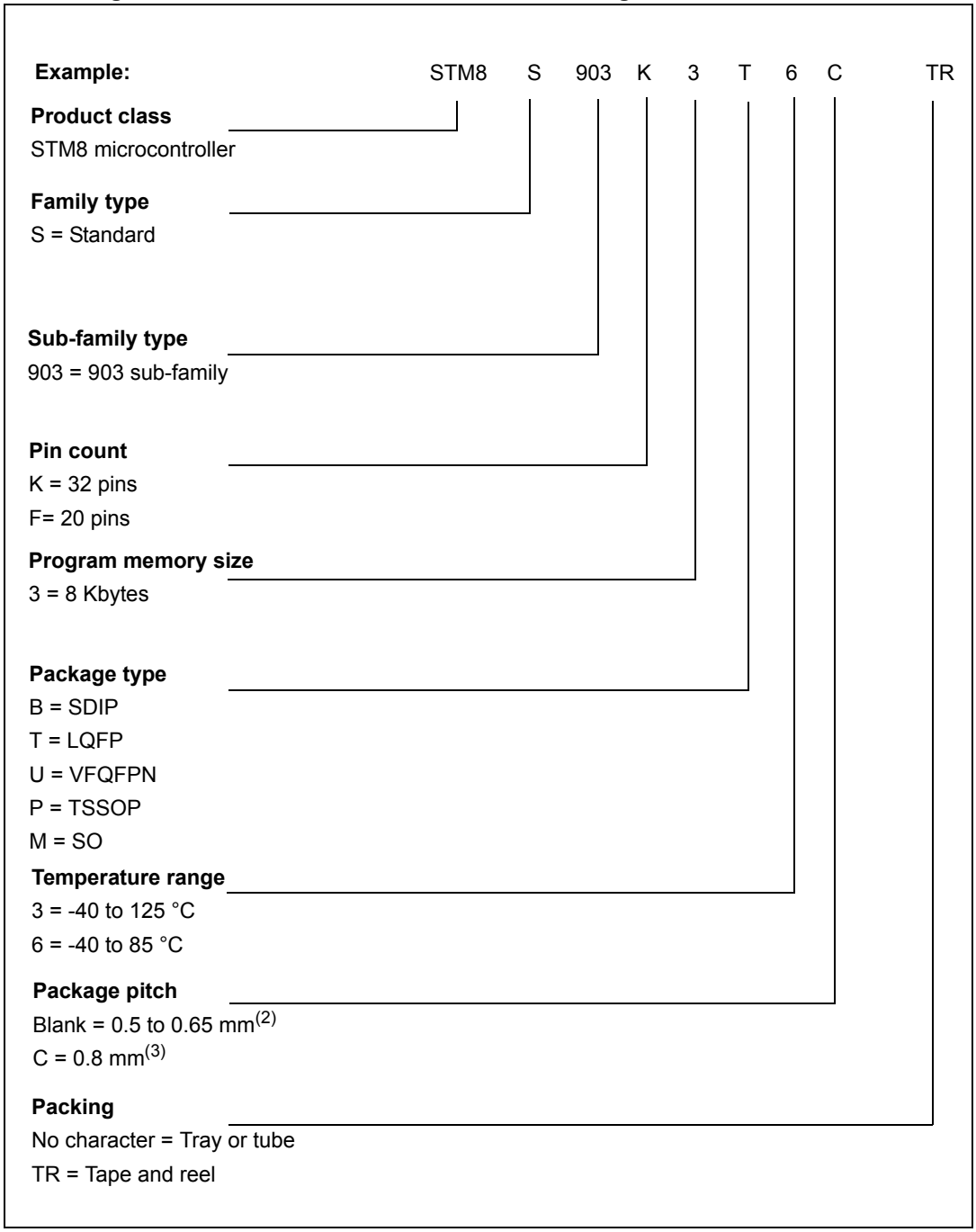
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

13 Ordering information

Figure 63. STM8S903K3/F3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP903K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

15 Revision history

Table 61. Document revision history

Date	Revision	Changes
30-Apr-2009	1	Initial release.
03-Jun-2009	2	– Added bullet point concerning unique identifier to *Features* section on cover page. – Highlighted internal reference voltage in *Section 4.13: Analog-to-digital converter (ADC1)*. – Updated wpu and PP status of PB5/12C_SDA[TIM1_BKIN] and PB4/12C_SCL[ADC_ETR] pins in *Section 5: Pinouts and pin descriptions*. – Updated *Section 6.1: Memory map*. – Added *Section 9: Unique ID*. – Added TBD values to *Table 45: SPI characteristics*. – Added max values to *Table 48: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 49: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*.