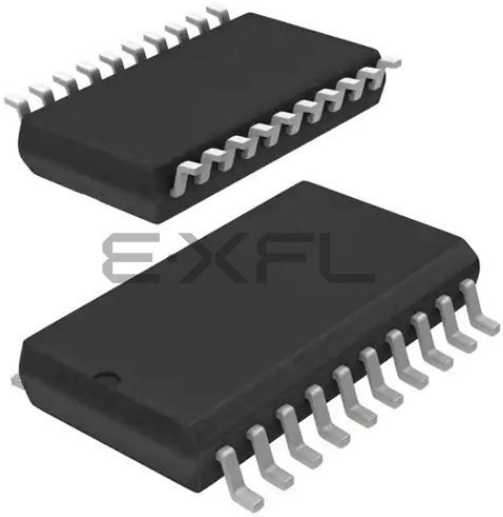


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903f3m6tr

4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM5	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	Reserved	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM6	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

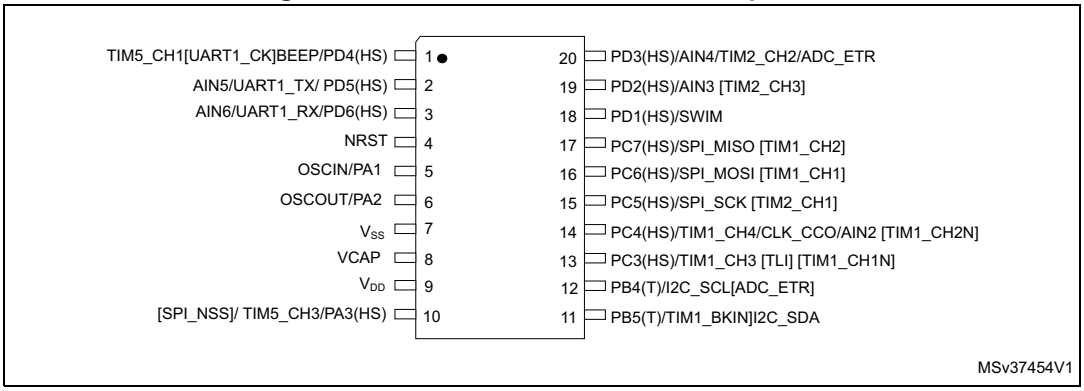
5 Pinouts and pin descriptions

Table 4. Legend/abbreviations for pinout tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

5.1 STM8S903F3 TSSOP20/SO20 pinout

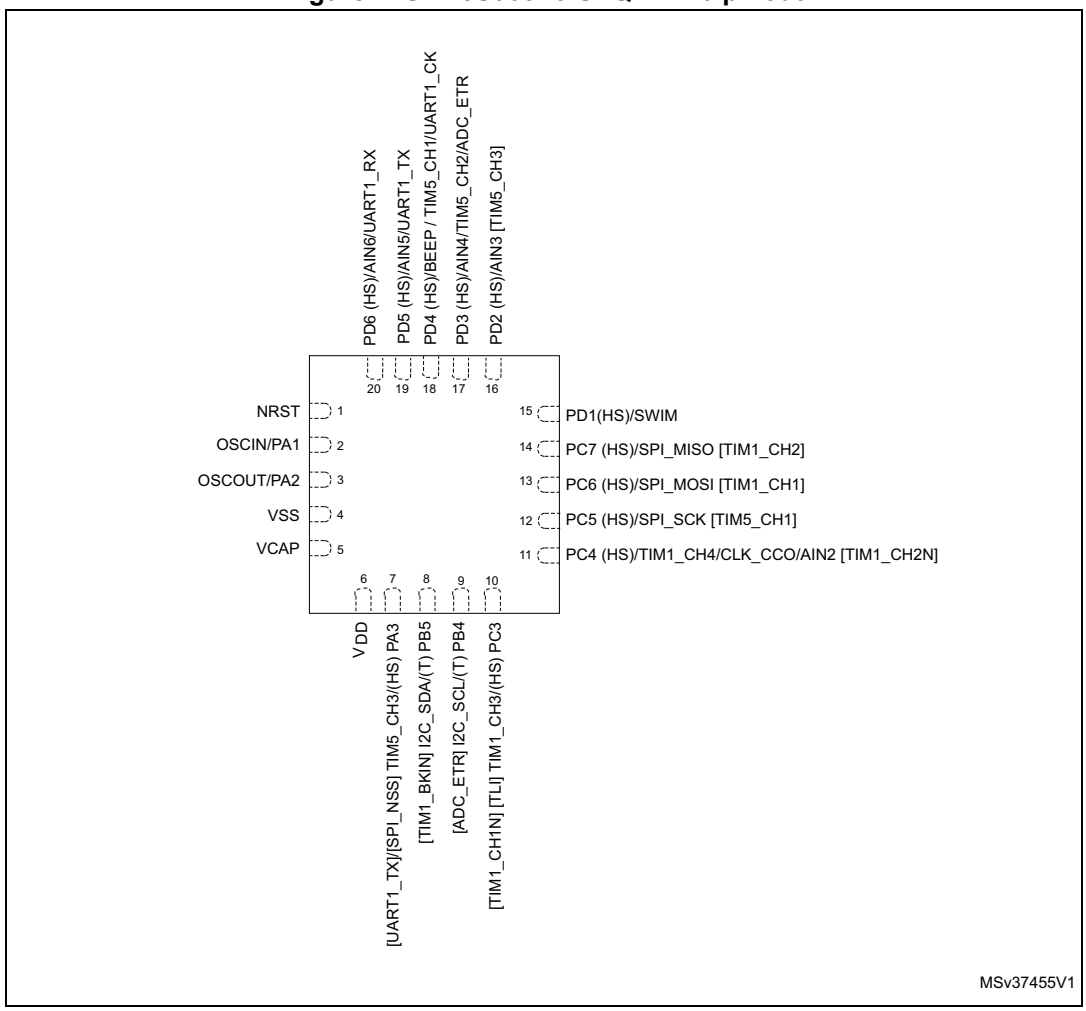
Figure 3. STM8S903F3 TSSOP20/SO20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function)

5.2 STM8S903F3 UFQFPN20 pinout

Figure 4. STM8S903F3 UFQFPN20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	EXTI5	Port F external interrupts	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM5	TIM5 update/ overflow/trigger	-	-	0x00 803C
14	TIM5	TIM5 capture/ compare	-	-	0x00 8040
15	Reserved	-	-	-	0x00 8044
16	Reserved	-	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

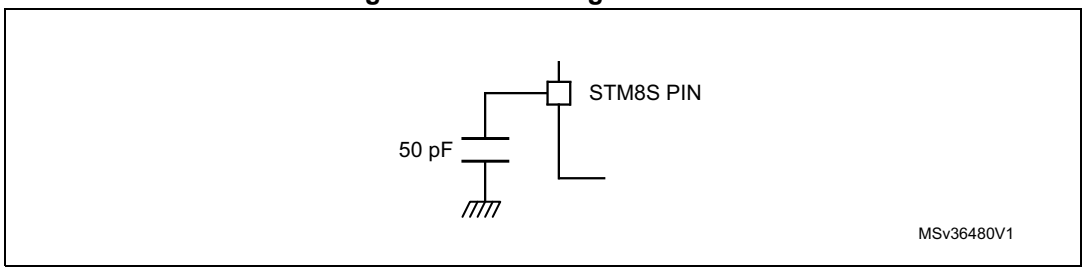
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

Figure 8. Pin loading conditions



10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 22. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 34. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source

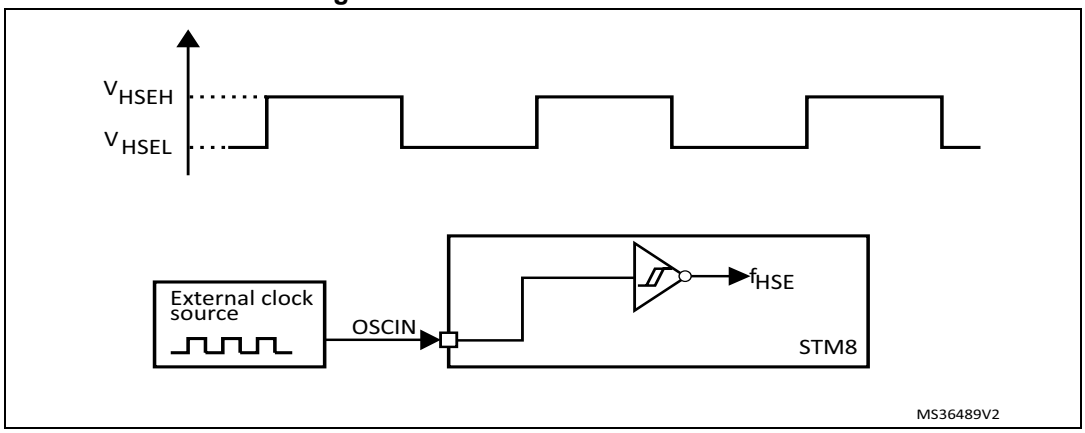
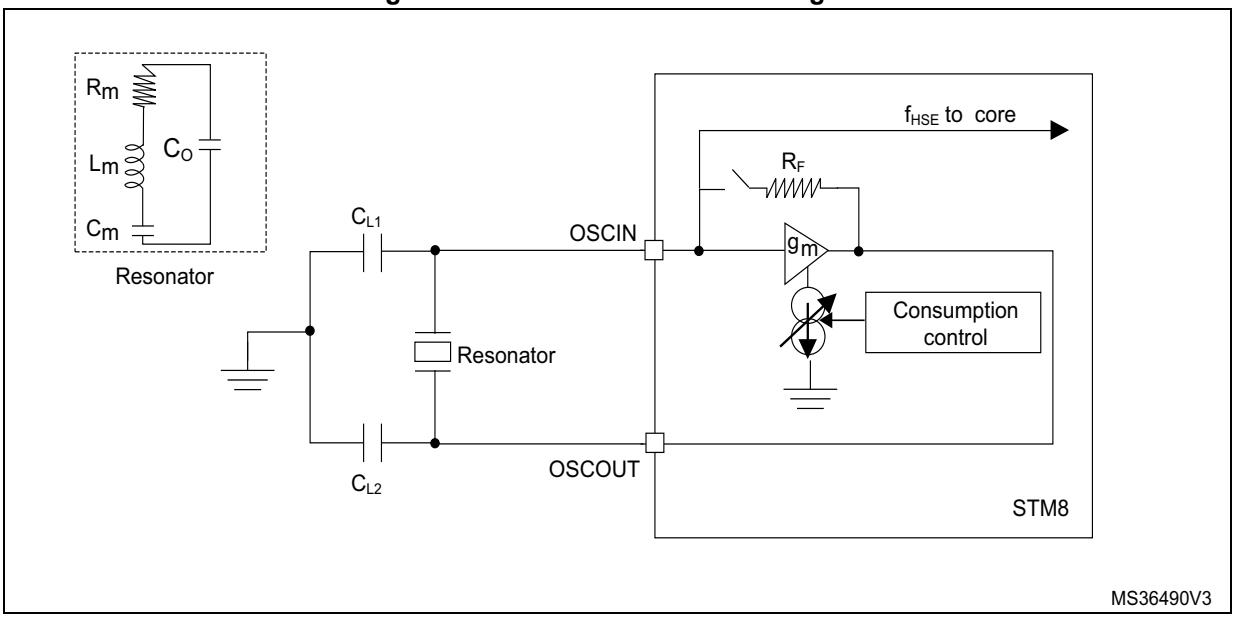


Figure 19. HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

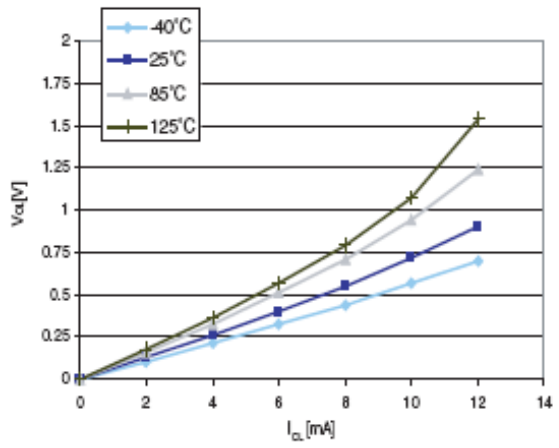


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

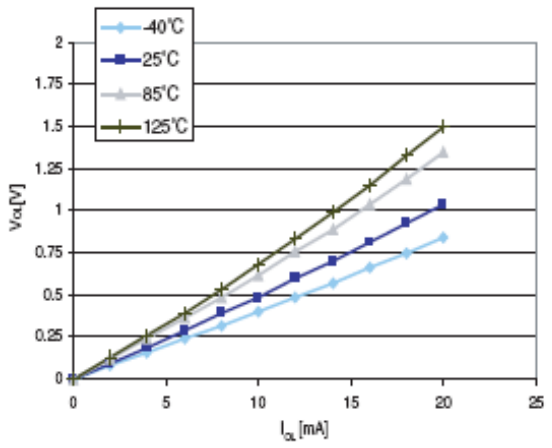


Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

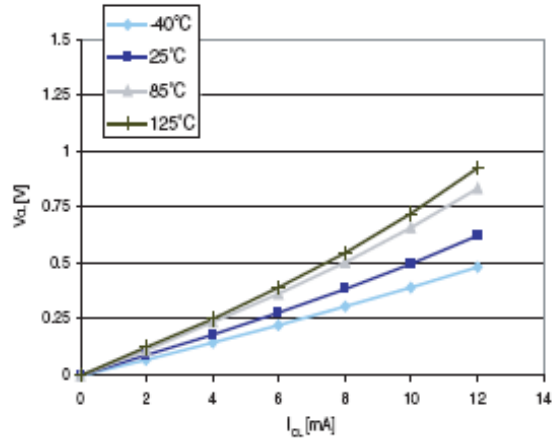
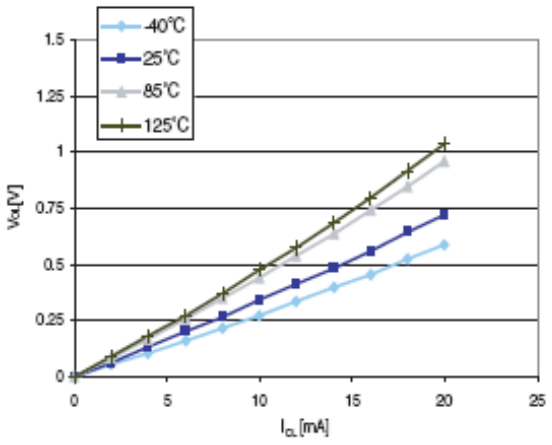


Figure 30. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)



Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 51. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		EMI level	2.5	2.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 52. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

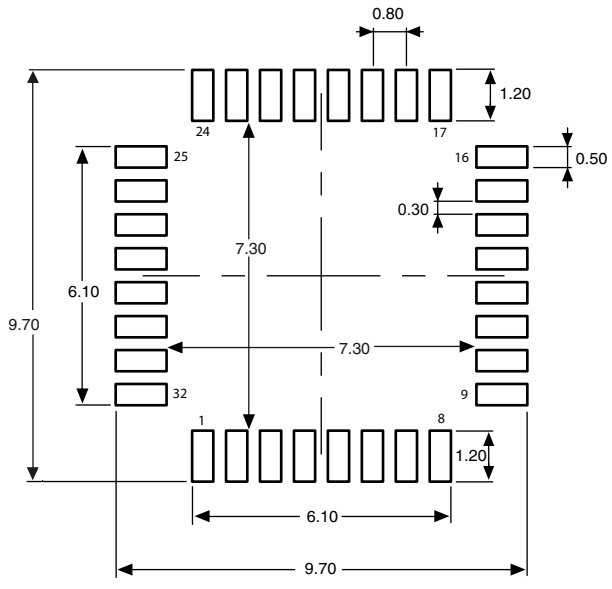
- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

Table 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

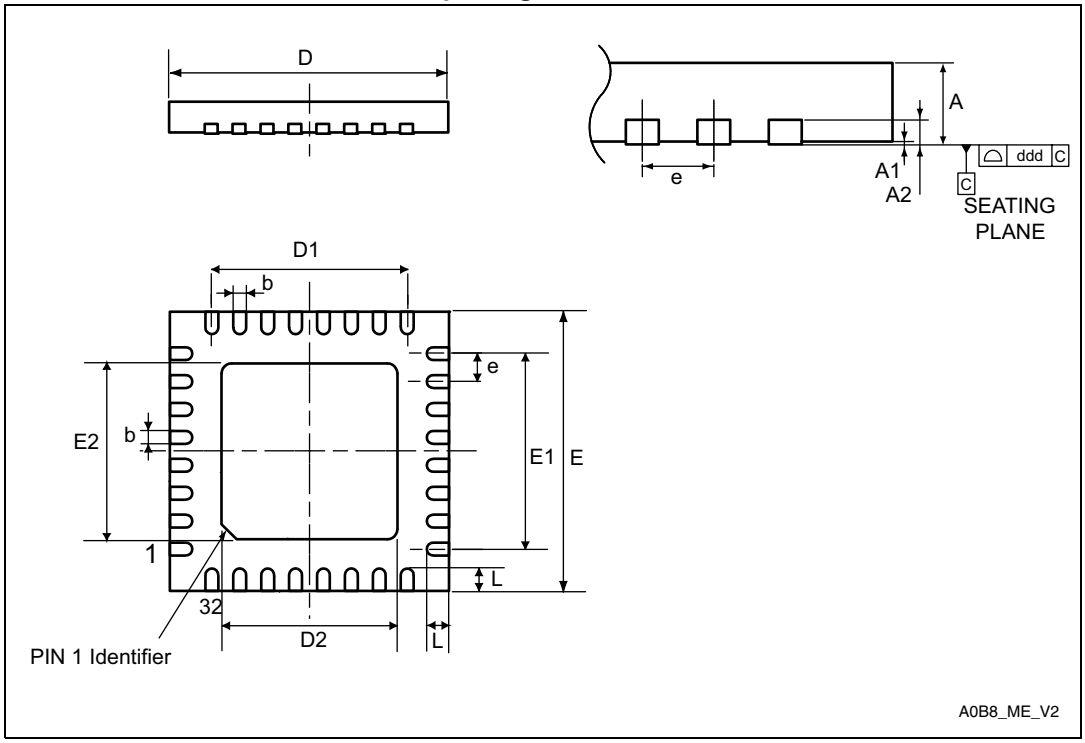
Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.2 UFQFPN32 package information

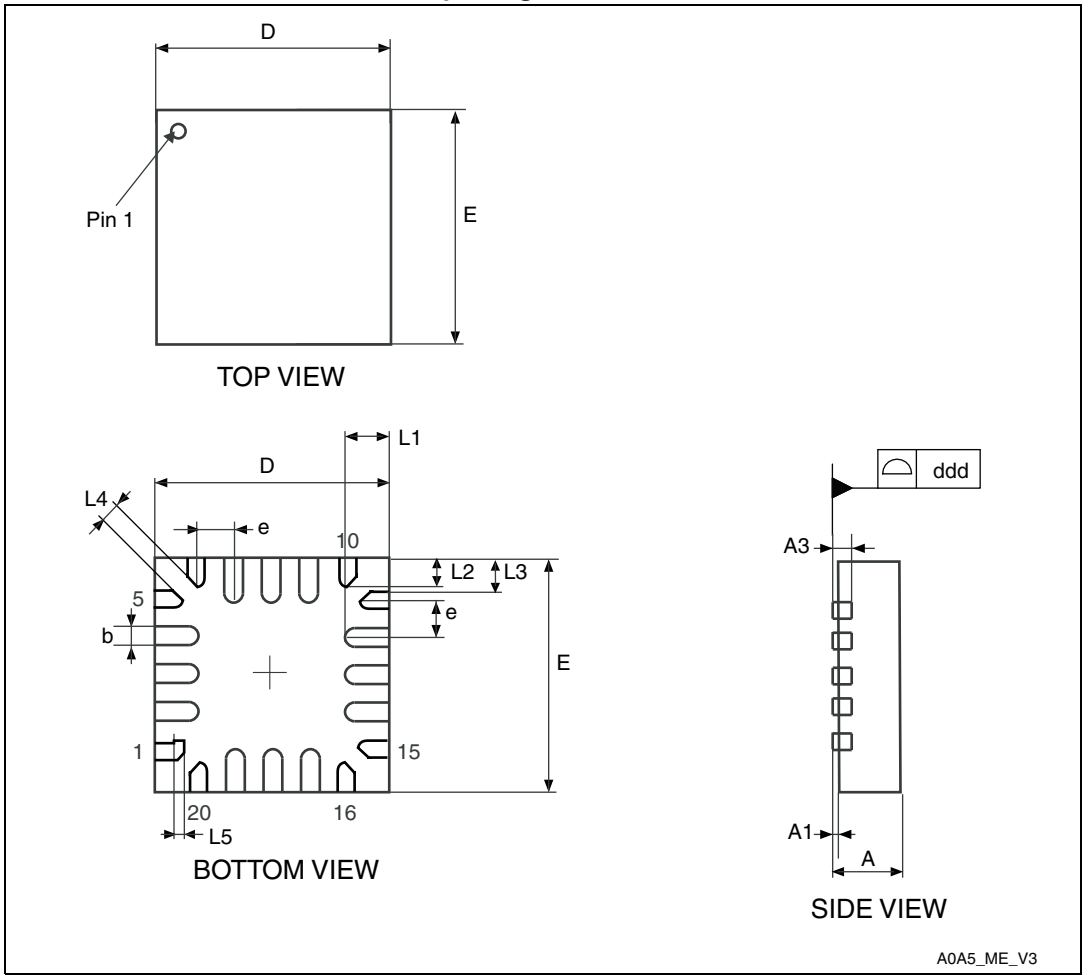
Figure 48. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

11.3 UFQFPN20 package information

Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 56. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

Table 57. SDIP32 package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eB	-	-	12.700	-	-	0.5000
L	2.540	3.048	3.810	0.1000	0.1200	0.1500

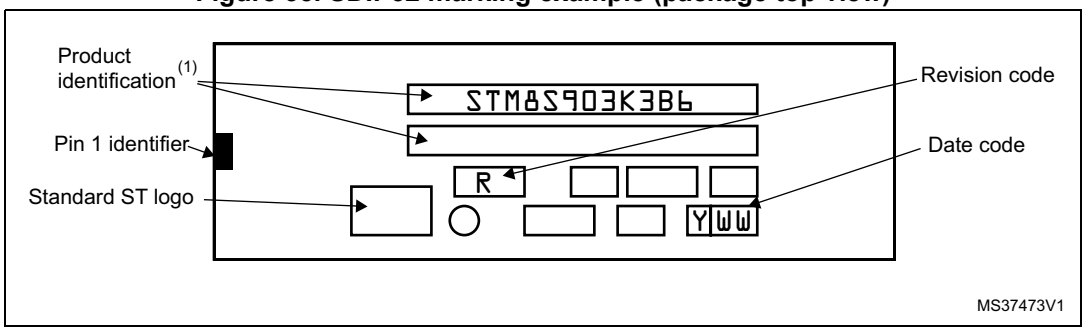
1. Values in inches are converted from mm and rounded to 4 decimal digits

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 55. SDIP32 marking example (package top view)



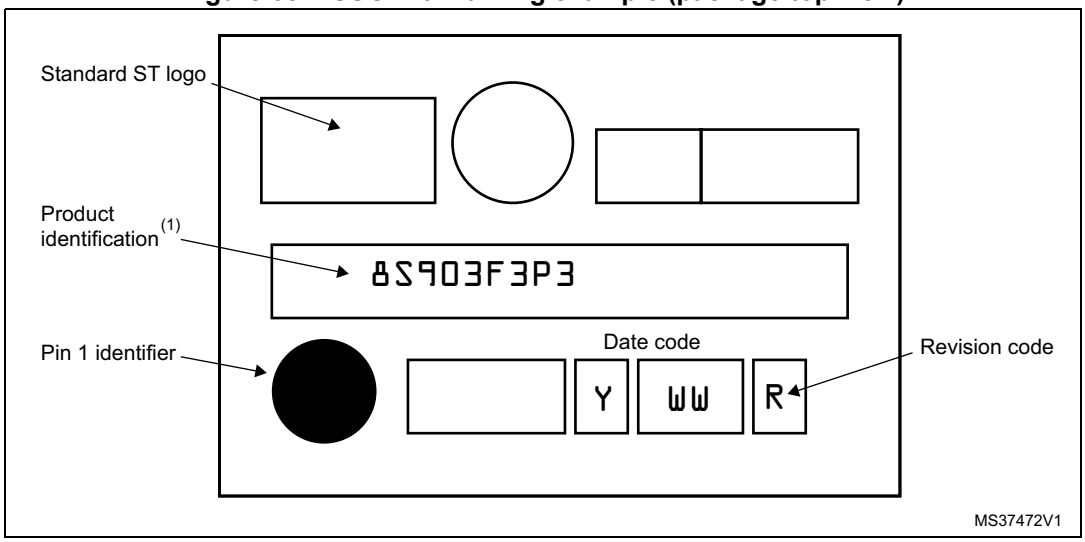
1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 58. TSSOP20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.6 SO20 package information

Figure 59. SO20 package outline

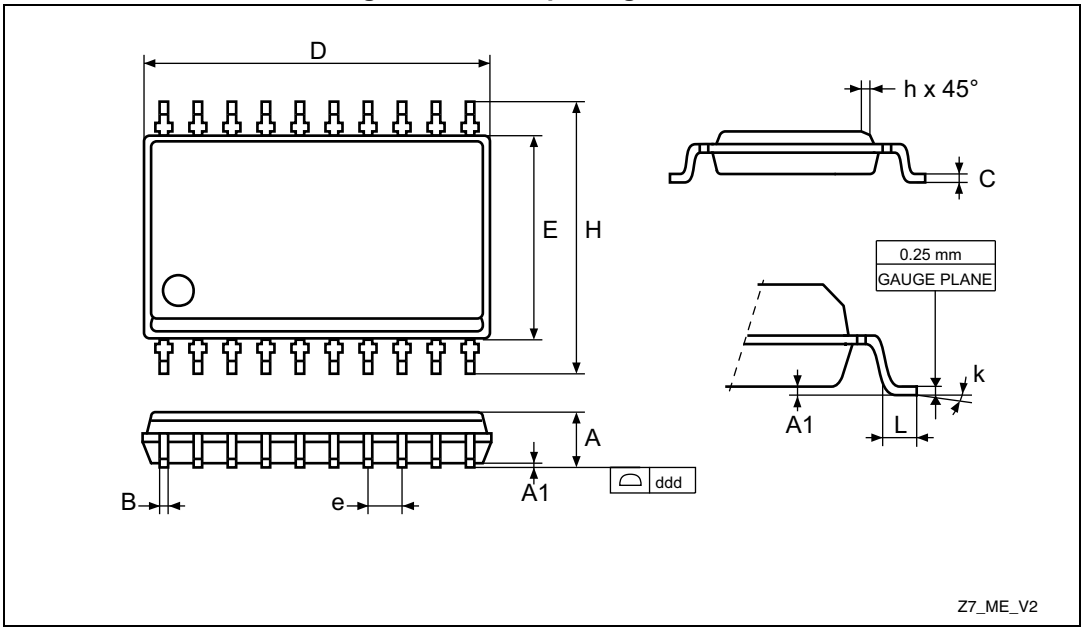


Table 59. SO20 mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	2.350	-	2.650	0.0925	-	0.1043
A1	0.100	-	0.300	0.0039	-	0.0118
B	0.330	-	0.510	0.013	-	0.0201
C	0.230	-	0.320	0.0091	-	0.0126
D	12.600	-	13.000	0.4961	-	0.5118
E	7.400	-	7.600	0.2913	-	0.2992
e	-	1.270	-	-	0.0500	-
H	10.000	-	10.650	0.3937	-	0.4193
h	0.250	-	0.750	0.0098	-	0.0295
L	0.400	-	1.270	0.0157	-	0.0500
k	0.0°	-	8.0°	0.0°	-	8.0°
ddd	-	-	0.100	-	-	0.0039

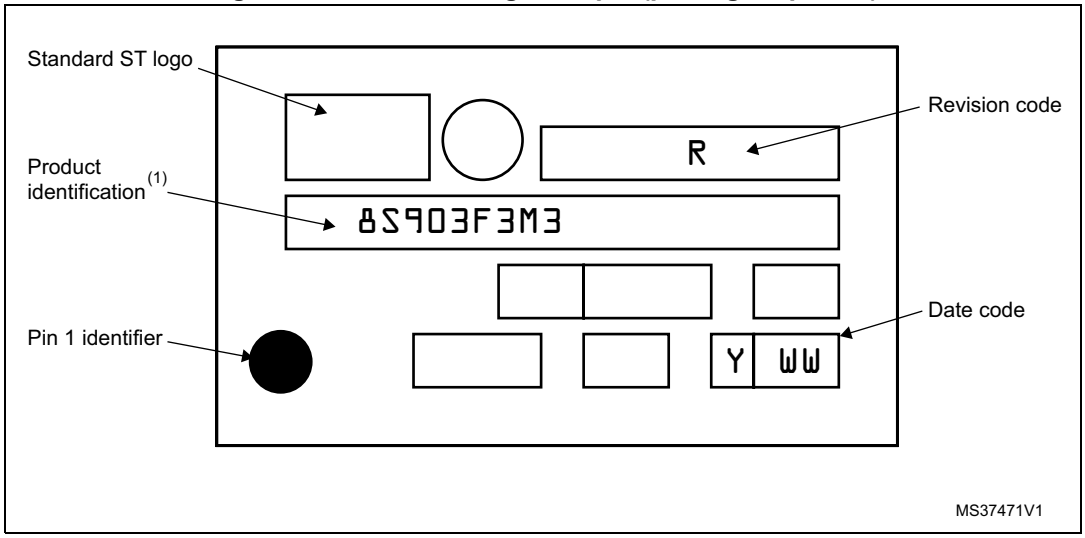
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

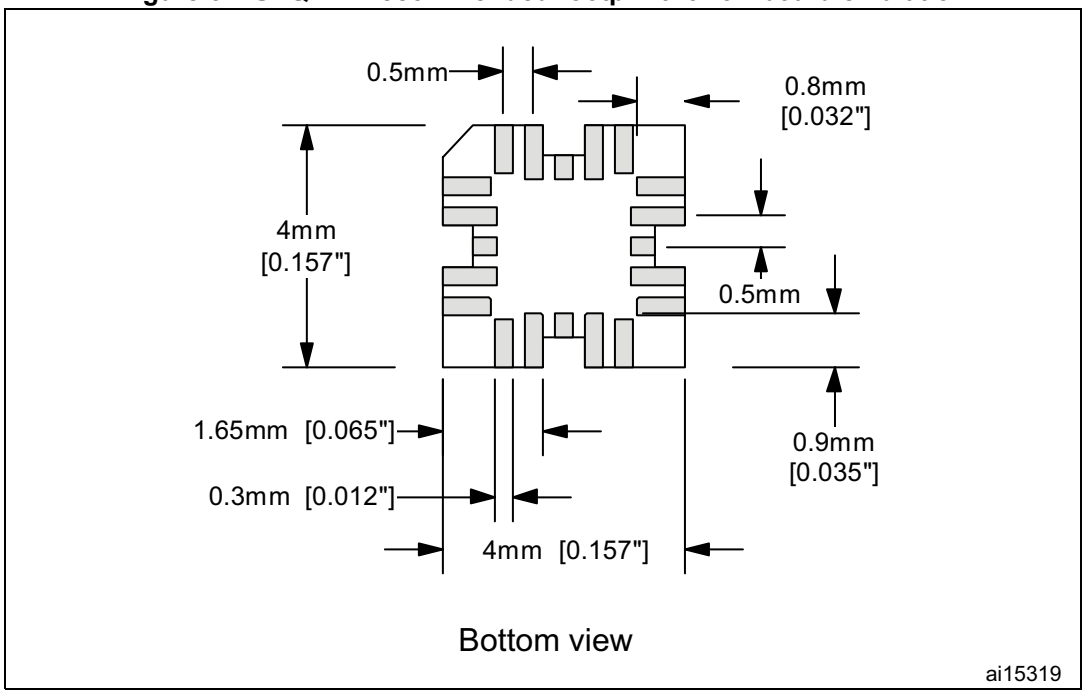
Figure 60. SO20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.7 UFQFPN recommended footprint

Figure 61. UFQFPN recommended footprint for on-board emulation



12.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 13: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 75°C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with

I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 8 mA x 5 V= 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

P_{Dmax} = 400 mW + 64 mW

Thus: P_{Dmax} = 464 mW.

Using the values obtained in *Table 60: Thermal characteristics on page 107* T_{Jmax} is calculated as follows:

For LQFP32 60 °C/W

T_{Jmax} = 75 °C + (60 °C/W x 464 mW) = 75 °C + 27.8 °C = 102.8 °C

This is within the range of the suffix 6 version parts (-40 < T_J < 105 °C).

Parts must be ordered at least with the temperature range suffix 6.

OPT4 watchdog

PRSC (check only one option)	[ ] for 16 MHz to 128 kHz prescaler [ ] for 8 MHz to 128 kHz prescaler [ ] for 4 MHz to 128 kHz prescaler
CKAWUSEL (check only one option)	[ ] LSI clock source selected for AWU [ ] HSE clock with prescaler selected as clock source for AWU
EXTCLK (check only one option)	[ ] External crystal connected to OSCIN/OSCOUT [ ] External signal on OSCIN

OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....

Table 61. Document revision history (continued)

Date	Revision	Changes
26-Mar-2015	10	Corrected the values for “b” dimensions in *Table 55: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.
13-Feb-2017	11	Updated: – Analog to digital converter (ADC) features on *Section : Features* – *Section 10.2: Absolute maximum ratings* – *Table 5: TSSOP20/SO20/UFQFPN20 pin descriptions* – *Table 19: Current characteristics* – *Table 33: Peripheral current consumption* – *Table 47: ADC characteristics* – *Table 56: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data* – *Figure 18: HSE external clock source* – *Figure 19: HSE oscillator circuit diagram* – *Figure 40: SPI timing diagram where slave mode and CPHA = 1* – *Figure 41: SPI timing diagram - master mode* – *Figure 44: Typical application with ADC* – *Section : Electromagnetic interference (EMI)* – All “Device marking” sections on *Section 11: Package information* – Footnotes on the tables of *Section 10: Electrical characteristics* and of *Figure 48: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline* – Title of *Table 54: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data* and *Table 56: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data* – Title of *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*, *Figure 46: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* Added: – *Figure 52: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*