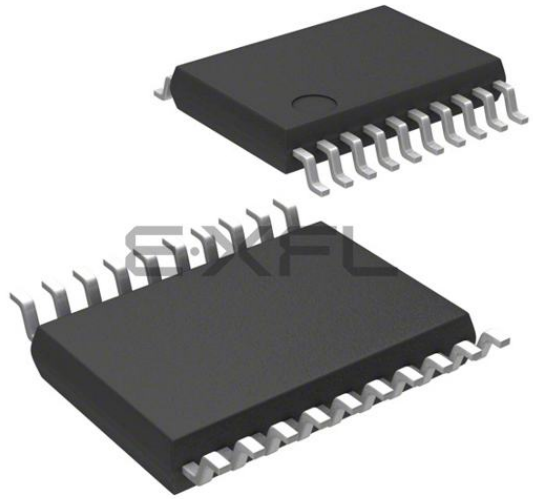

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903f3p6tr

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5.3 TSSOP20, SO20 and UFQFPN20 pin descriptions

Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions

TSSOP20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext.	High sink(1)	Speed	OD	PP			
4	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 52 channel 3	SPI master/ slave select [AFR1]/ UART1 data transmit [AFR1:0]
11	8	PB5/ I2C_SDA [TIM1_BKIN]	I/O	**X**	-	X	-	O1	T(3)		**Port B5**	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_SCL [ADC_ETR]	I/O	**X**	-	X	-	O1	T(3)		**Port B4**	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3/TLI/ [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7]
14	11	PC4/ TIM1_CH4/ CLK_CCO/AIN2/ [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7]
15	12	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 5 channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	PI master out/slave in	Timer 1 channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 channel 2[AFR0]
18	15	PD1/ SWIM(4)	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-

Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions (continued)

TSSOP20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext.	High sink(1)	Speed	OD	PP			
19	16	PD2/AIN3/ [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4 Timer 52 - channel 2/ADC external trigger	-
1	18	PD4/ TIM5_CH1/ BEEP [UART1_CK]	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 5 - channel 1/BEEP output	UART clock [AFR2]
2	19	PD5/ AIN5/ UART1_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ UART1 data transmit	-
3	20	PD6/ AIN6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, ‘T’ defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
4	31	PD6/ AIN6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
5	32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10: Electrical characteristics*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF
0x00 5349 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC_DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			

Table 23. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 24. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	mA
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Figure 14. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz

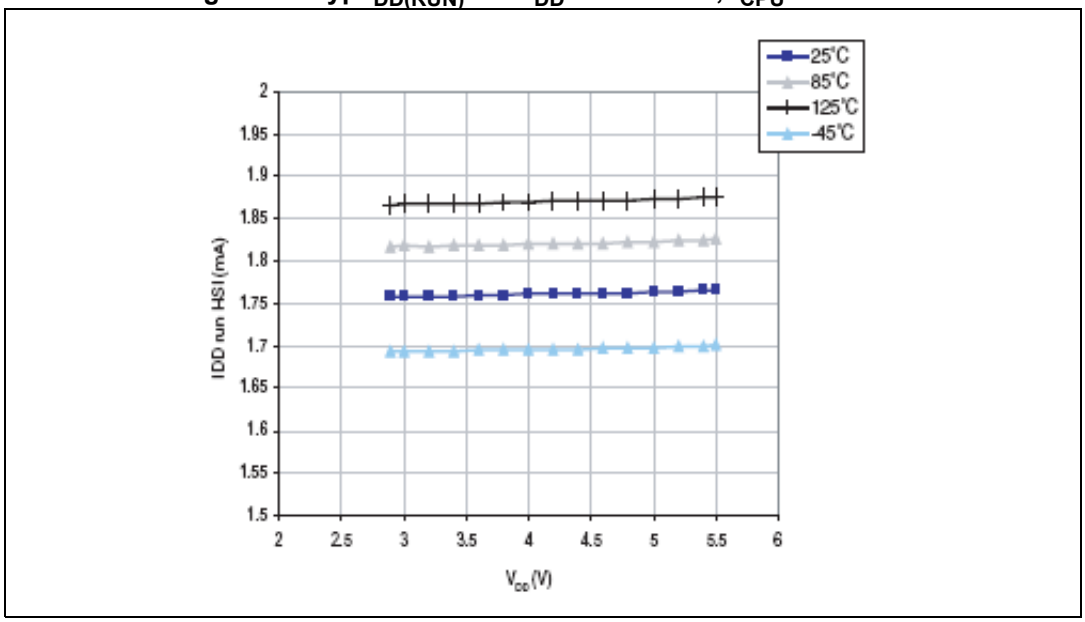
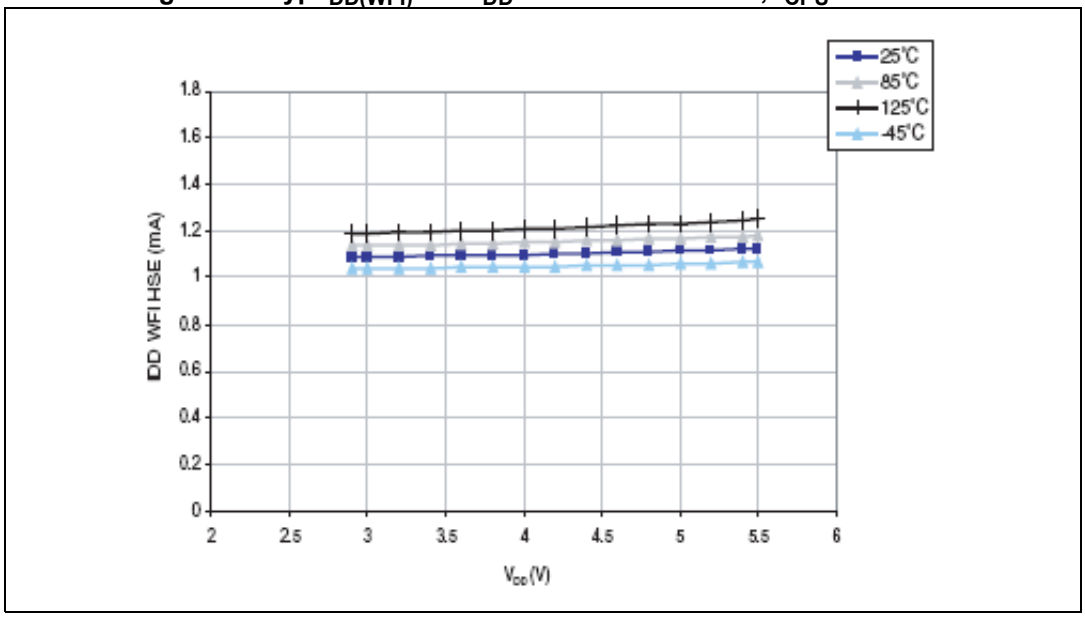


Figure 15. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE external clock, f_{CPU} = 16 MHz



10.3.3 External clock sources and timing characteristics

HSE user external clock

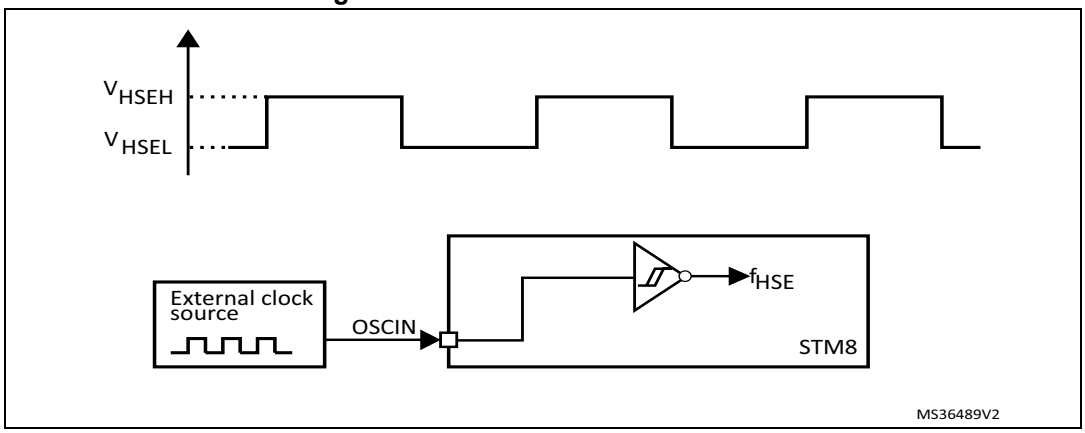
Subject to general operating conditions for V_{DD} and T_A.

Table 34. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source



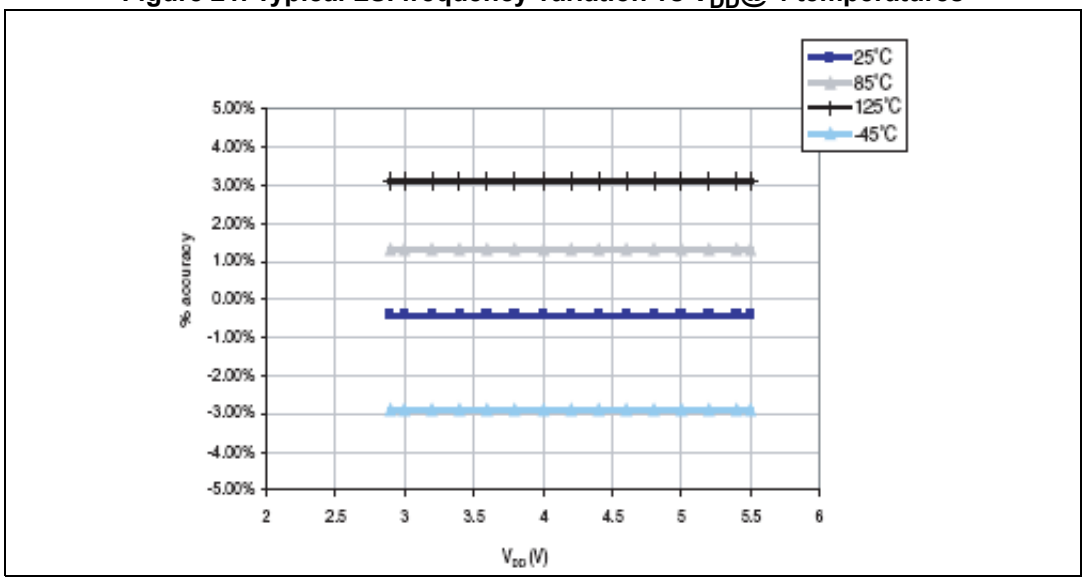
Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 37. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110	128	150	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
IDD(LSI)	LSI oscillator power consumption	-	-	5	-	µA

Figure 21. Typical LSI frequency variation vs V_{DD}@ 4 temperatures



10.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 47. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD}= 2.95 to 5.5 V	1	-	4	MHz
		V_{DD}= 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 2.95 to 5.5 V	1.19	1.22	1.25	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4 MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
		-	14			$1/f_{ADC}$

1. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 53. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	

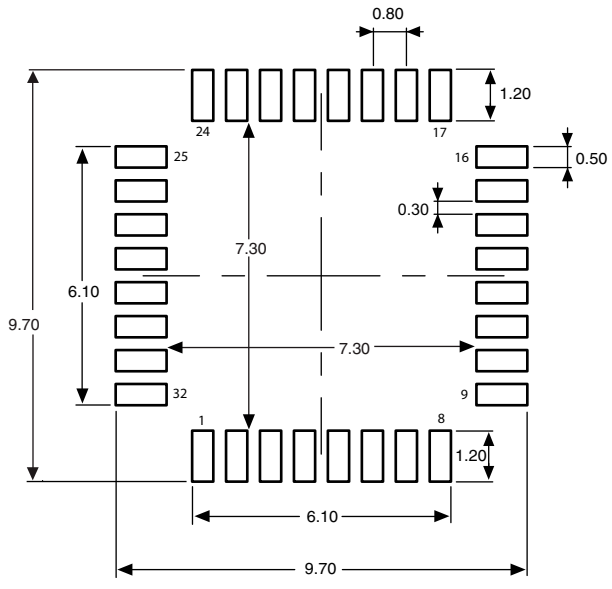
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

Table 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

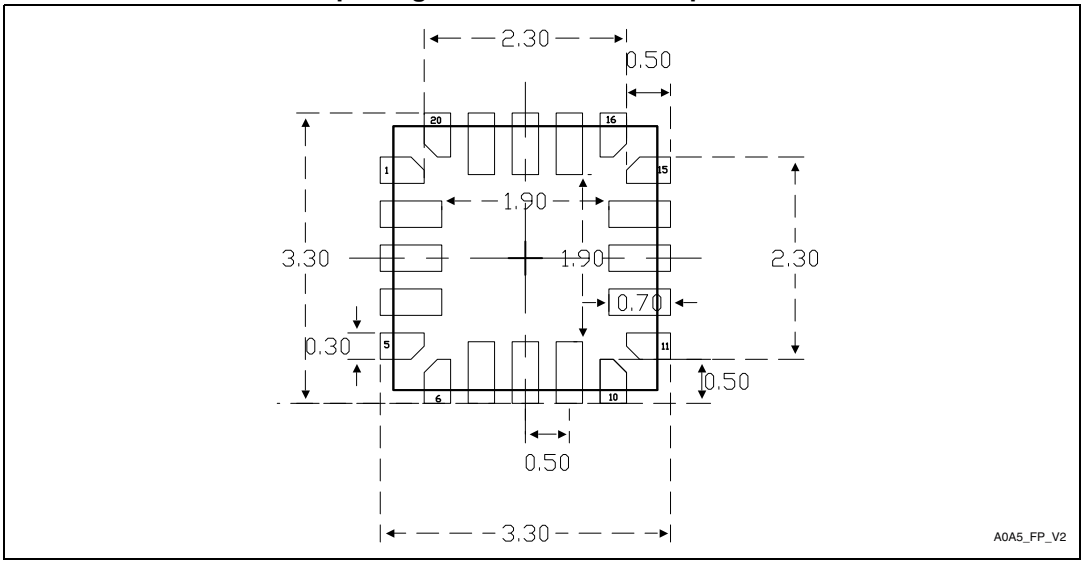
Table 56. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits

Section 11.7: UFQFPN recommended footprint shows the recommended footprints for UFQFPN with and without on-board emulation.

Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

11.5 TSSOP20 package information

Figure 56. TSSOP20 package outline

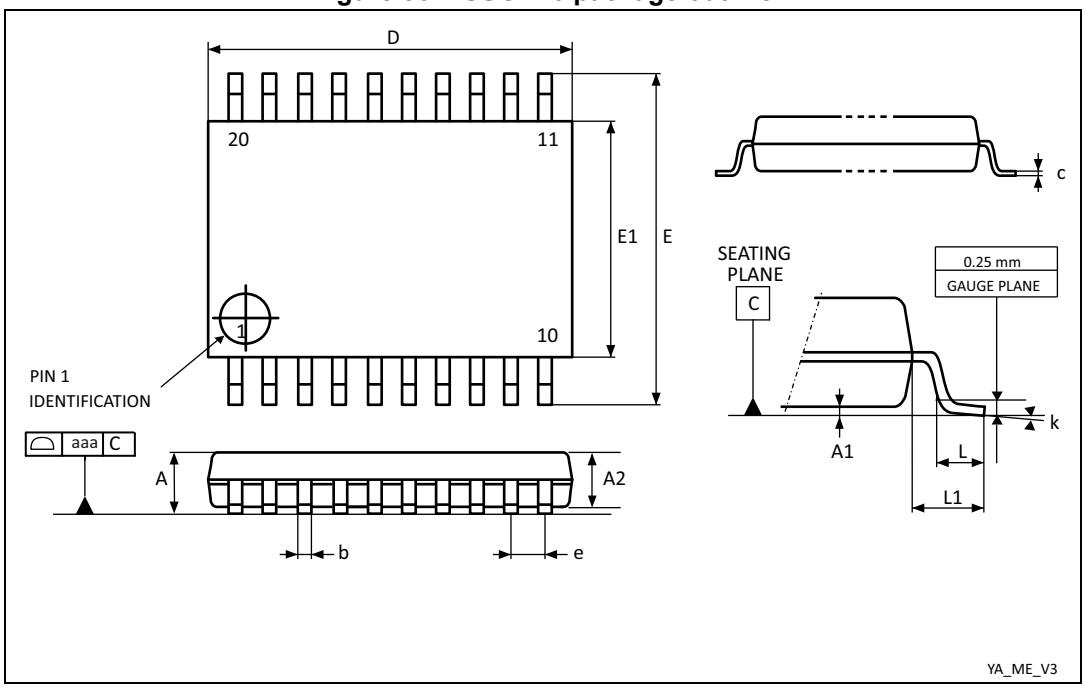


Table 58. TSSOP20 package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

OTP2 alternate function remapping for STM8S903K3

Do not use more than one remapping option in the same port.

AFR1, AFR0 (check only one option)	[ ] 00: Remapping options inactive. Default alternate functions used. Refer to pinout description. [ ] 01: Port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, and port C7 alternate function = TIM1_CH2. [ ] 10: Port A3 alternate function = SPI_NSS and port D2 alternate function = TIM5_CH3. [ ] 11: Port D2 alternate function = TIM5_CH3, port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, port C7 alternate function = TIM1_CH2, port C2 alternate function = TIM1_CH3N, port C1 alternate function = TIM1_CH2N, port E5 alternate function = TIM1_CH1N, port A3 alternate function = UART1_TX, and port F4 alternate function = UART1_RX.
AFR2 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port C4 alternate function = AIN2, port D2 alternate function = AIN3, port D4 alternate function = UART1_CK.
AFR3 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port C3 alternate function = TLI.
AFR4 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port B4 alternate function = ADC_ETR, port B5 alternate function = TIM1_BKIN.
AFR5 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port D0 alternate function = CLK_CCO.
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port D7 alternate function = TIM1_CH4.
AFR7 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. [ ] 1: Port C3 alternate function = TIM1_CH1N, port C4 alternate function = TIM1_CH2N.

Table 61. Document revision history (continued)

Date	Revision	Changes
08-Sep-2010	5	Removed VFQFPN32 package. Updated the definition for reset state in *Table 4: Legend/abbreviations for pinout tables* Updated pins 13/25/20, 14/26/21, 19/32/27, 1/2/29, 2/3/30, and 3/4/31; added footnote to PD1/SWIM pin in *Table 6: STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions*. Standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Changed the caption of *Table 13: STM8S903K3 alternate function remapping bits [7:2] for 32-pin packages*. Added *Table 14: STM8S903F3 alternate function remapping bits [7:2] for 20-pin packages*. Changed the caption of *Table 15: STM8S903K3 alternate function remapping bits [1:0] for 32-pin packages*. Added *Table 16: STM8S903F3 alternate function remapping bits [1:0] for 20-pin packages*. Replaced 0.01 µF with 0.1 µF in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram*. Updated footnote 1 in *Table 48: ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V* and *Table 49: ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V*. Updated existing footnote and added three additional footnotes to *Table 55: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*. Updated the special marking and OPT2 alternate function remapping sections in *Section 13.1: STM8S903K3/F3 FASTROM microcontroller option list*.