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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903k3t3c

11.2	UFQFPN32 package information	93
11.3	UFQFPN20 package information	96
11.4	SDIP32 package information	99
11.5	TSSOP20 package information	101
11.6	SO20 package information	104
11.7	UFQFPN recommended footprint	105
12	Thermal characteristics	107
12.1	Reference document	107
12.2	Selecting the product temperature range	108
13	Ordering information	109
13.1	STM8S903K3/F3 FASTROM microcontroller option list	110
14	STM8 development tools	115
14.1	Emulation and in-circuit debugging tools	115
14.1.1	STice key features	115
14.2	Software tools	116
14.2.1	STM8 toolset	116
14.2.2	C and assembly toolchains	116
14.3	Programming tools	117
15	Revision history	118

4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)

SDIP32	LQFP/UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink ⁽¹⁾	Speed	OD	PP			
12	7	PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX]	I/O	X	X	X	HS	O3	X	X	Port A3	Timer 5 channel 3	SPI master/ slave select [AFR1] /UART1 data transmit [AFR 1:0]
13	8	PF4 [UART1_RX]	I/O	X	X	-	-	O1	X	X	Port F4	-	UART1 data receive [AFR1:0]
14	9	PB7	I/O	X	X	X	-	O1	X	X	Port B7	-	-
15	10	PB6	I/O	X	X	X	-	O1	X	X	Port B6	-	-
16	11	PB5/ I2C_SDA [TIM1_BKIN]	I/O	X	-	X	-	O1	T ₍₃₎	-	Port B5	I2C data	Timer 1 - break input [AFR4]
17	12	PB4/ I2C_SCL [ADC_ETR]	I/O	X	-	X	-	O1	T	-	Port B4	I2C clock	ADC external trigger [AFR4]
18	13	PB3/ AIN3/TIM1_ETR	I/O	X	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
19	14	PB2/ AIN2/ TIM1_CH3N	I/O	X	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
20	15	PB1/ AIN1/ TIM1_CH2N	I/O	X	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
21	16	PB0/ AIN0/ TIM1_CH1N	I/O	X	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-
22	17	PE5/ SPI_NSS [TIM1_CH1N]	I/O	X	X	X	HS	O3	X	X	Port E5	SPI master/slave select	Timer 1 - inverted channel 1 [AFR1:0]
23	18	PC1/ TIM1_CH1/ UART1_CK [TIM1_CH2N]	I/O	X	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	Timer 1 - inverted channel 2 [AFR1:0]

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xFF ⁽¹⁾
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xFF ⁽¹⁾
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xFF ⁽¹⁾
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xFF ⁽¹⁾
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xFF ⁽¹⁾
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xFF ⁽¹⁾
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	EXTCLK: External clock selection 0: External crystal connected to OSCIN/OSCOU 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	HSECNT[7:0]: HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

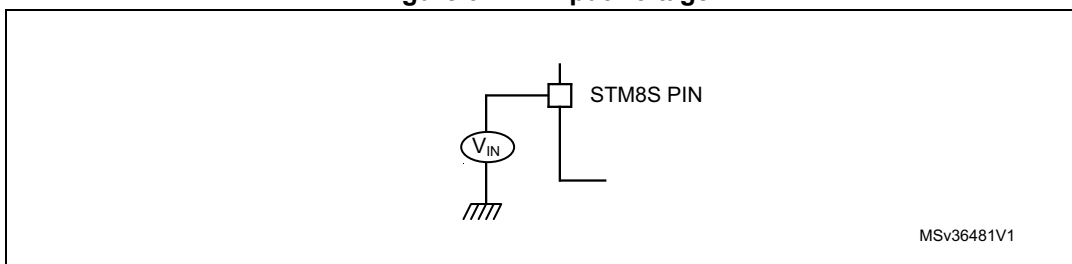
8.1 Alternate function remapping bits

Table 13. STM8S903K3 alternate function remapping bits [7:2] for 32-pin packages

Option byte no.	Description ⁽¹⁾
OPT2	<p>AFR7 Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate functions.⁽²⁾ 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N.</p> <p>AFR6 Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.⁽²⁾ 1: Port D7 alternate function = TIM1_CH4.</p> <p>AFR5 Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.⁽²⁾ 1: Port D0 alternate function = CLK_CCO.</p> <p>AFR4 Alternate function remapping option 4 0: AFR4 remapping option inactive: Default alternate functions.⁽²⁾ 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.</p> <p>AFR3 Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function.⁽²⁾ 1: Port C3 alternate function = TLI.</p> <p>AFR2 Alternate function remapping option 2 0: AFR2 remapping option inactive: Default alternate functions.⁽²⁾ 1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3; port D4 alternate function = UART1_CK</p>

1. Do not use more than one remapping option in the same port.

Figure 9. Pin input voltage



10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 18: Voltage characteristics](#), [Table 19: Current characteristics](#) and [Table 20: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 Qualification Standard, the extended mission profiles are available on demand.

Table 18. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V _{DDx} - V _{SS}	Supply voltage (including VDDA and VDDIO) ⁽¹⁾	-0.3	6.5	V
V _{IN}	Input voltage on true open drain pins ⁽²⁾	V _{SS} - 0.3	6.5	V
	Input voltage on any other pin ⁽²⁾	V _{SS} - 0.3	V _{DD} + 0.3	
V _{DDx} - V _{DD}	Variations between different power pins	-	50	mV
V _{SSx} - V _{SS}	Variations between all the different ground pins	-	50	
V _{ESD}	Electrostatic discharge voltage	see <i>Absolute maximum ratings (electrical sensitivity) on page 88</i>		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. This pin must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 19. Current characteristics

Symbol	Ratings	Max. ⁽¹⁾	Unit
I_{VDD}	Total current into V_{DD} power lines (source) ⁽²⁾	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	

Total current consumption in wait mode

Table 25. Total current consumption in wait mode at $V_{DD} = 5\text{ V}$

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER} = 16\text{ MHz}$	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER} / 128 = 125\text{ kHz}$	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER} / 8192 = 15.625\text{ kHz}$	HSI RC osc. (16 MHz/8) ⁽²⁾	0.45	0.57	
		$f_{CPU} = f_{MASTER} = 128\text{ kHz}$	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.

2. Default clock configuration measured with all peripherals off.

Table 26. Total current consumption in wait mode at $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER} = 16\text{ MHz}$	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER} / 128 = 125\text{ kHz}$	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER} / 8192 = 15.625\text{ kHz}$	HSI RC osc. (16 MHz/8) ⁽²⁾	0.45	0.57	
		$f_{CPU} = f_{MASTER} = 128\text{ kHz}$	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.

2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 27. Total current consumption in active halt mode at $V_{DD} = 5\text{ V}$

Symbol	Parameter	Conditions			Typ	Max at 85 °C ⁽¹⁾	Max at 85 °C ⁽¹⁾	Unit
		Main voltage regulator (MVR) ⁽²⁾	Flash mode ⁽³⁾	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	μA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

1. Guaranteed by characterization results.

2. Configured by the REGAH bit in the CLK_ICKR register.

3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 28. Total current consumption in active halt mode at $V_{DD} = 3.3\text{ V}$

Symbol	Parameter	Conditions			Typ	Max at 85 °C ⁽¹⁾	Max at 85 °C ⁽¹⁾	Unit
		Main voltage regulator (MVR) ⁽²⁾	Flash mode ⁽³⁾	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	μA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.

2. Configured by the REGAH bit in the CLK_ICKR register.

3. Configured by the AHALT bit in the FLASH_CR1 register.

2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 32. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$I_{DD(R)}$	Supply current in reset state ⁽²⁾	$V_{DD} = 5\text{ V}$	400	-	μA
		$V_{DD} = 3.3\text{ V}$	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	μs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS} .

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A .

HSI internal RC/ $f_{CPU} = f_{MASTER} = 16\text{ MHz}$, $V_{DD} = 5\text{ V}$

Table 33. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current ⁽¹⁾	210	μA
$I_{DD(TIM5)}$	TIM5 supply current ⁽¹⁾	130	
$I_{DD(TIM6)}$	TIM6 supply current ⁽¹⁾	50	
$I_{DD(UART1)}$	UART1 supply current ⁽²⁾	120	
$I_{DD(SPI)}$	SPI supply current ⁽²⁾	45	
$I_{DD(I2C)}$	I2C supply current ⁽²⁾	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting ⁽³⁾	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

10.3.3 External clock sources and timing characteristics

HSE user external clock

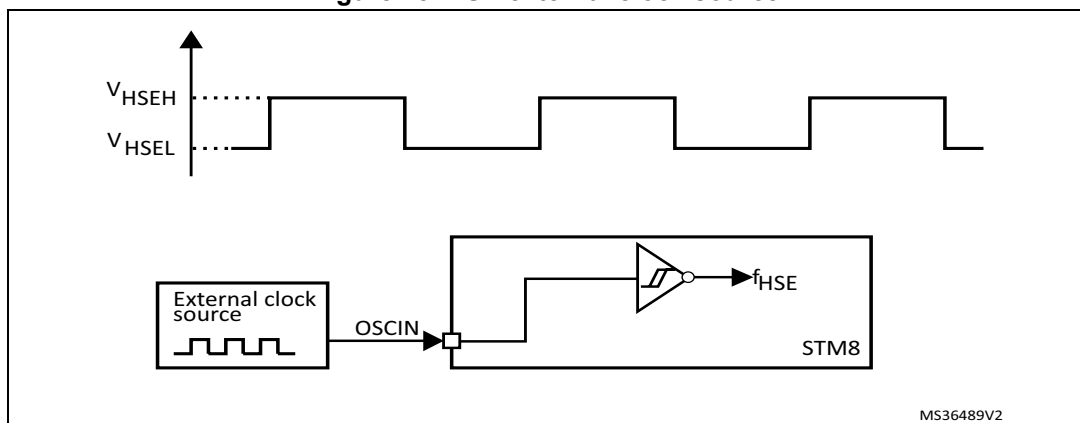
Subject to general operating conditions for V_{DD} and T_A .

Table 34. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
$V_{HSEH}^{(1)}$	OSCIN input pin high level voltage	-	$0.7 \times V_{DD}$	$V_{DD} + 0.3 \text{ V}$	V
$V_{HSEL}^{(1)}$	OSCIN input pin low level voltage	-	V_{SS}	$0.3 \times V_{DD}$	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	μA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 35. HSE oscillator characteristics

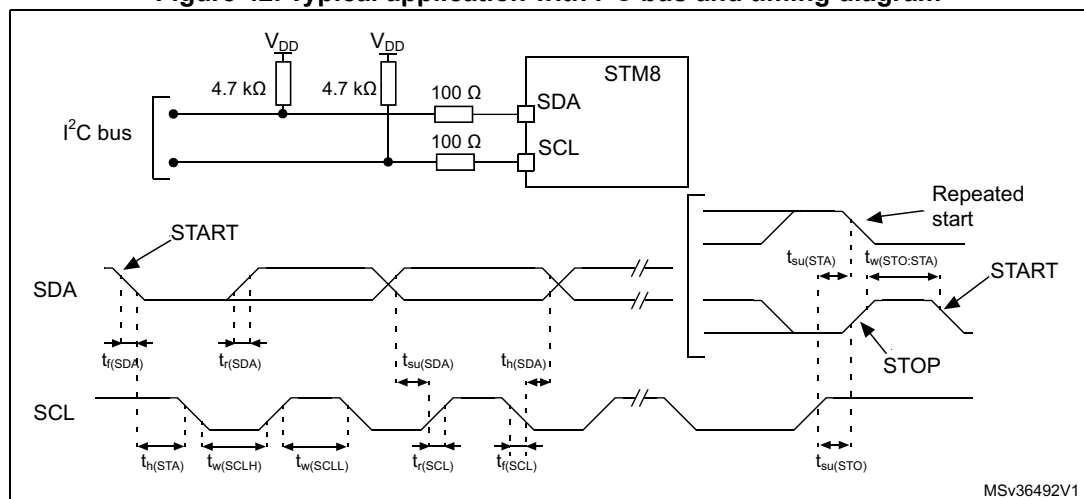
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	k Ω
$C^{(1)}$	Recommended load capacitance ⁽²⁾	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF $f_{OSC} = 16$ MHz	-	-	6 (start up) 1.6 (stabilized) ⁽³⁾	mA
		C = 10 pF $f_{OSC} = 16$ MHz	-	-	6 (start up) 1.2 (stabilized) ⁽³⁾	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

10.3.9 I²C interface characteristicsTable 46. I²C characteristics

Symbol	Parameter	Standard mode I ² C		Fast mode I ² C ⁽¹⁾		Unit
		Min ⁽²⁾	Max ⁽²⁾	Min ⁽²⁾	Max ⁽²⁾	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_h(SDA)$	SDA data hold time	0 ⁽³⁾	-	0 ⁽⁴⁾	900 ⁽³⁾	
$t_r(SDA)$ $t_r(SCL)$	SDA and SCL rise time ($V_{DD} = 3$ to 5.5 V)	-	1000	-	300	
$t_f(SDA)$ $t_f(SCL)$	SDA and SCL fall time ($V_{DD} = 3$ to 5.5 V)	-	300	-	300	
$t_h(STA)$	START condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_w(STO:STA)$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER} must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 42. Typical application with I²C bus and timing diagram

10.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA} , f_{MASTER} , and T_A unless otherwise specified.

Table 47. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	$V_{DD} = 2.95$ to 5.5 V	1	-	4	MHz
		$V_{DD} = 4.5$ to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range ⁽¹⁾	-	V_{SS}	-	V_{DD}	V
V_{BREF}	Internal bandgap reference voltage	$V_{DD} = 2.95$ to 5.5 V	1.19	1.22	1.25	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_S^{(1)}$	Minimum sampling time	$f_{ADC} = 4$ MHz	-	0.75	-	μs
		$f_{ADC} = 6$ MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	μs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	$f_{ADC} = 4$ MHz	3.5			μs
		$f_{ADC} = 6$ MHz	2.33			μs
		-	14			$1/f_{ADC}$

1. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 50. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 61000-4-2	2/B ⁽¹⁾
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 61000-4-4	4/A ⁽¹⁾

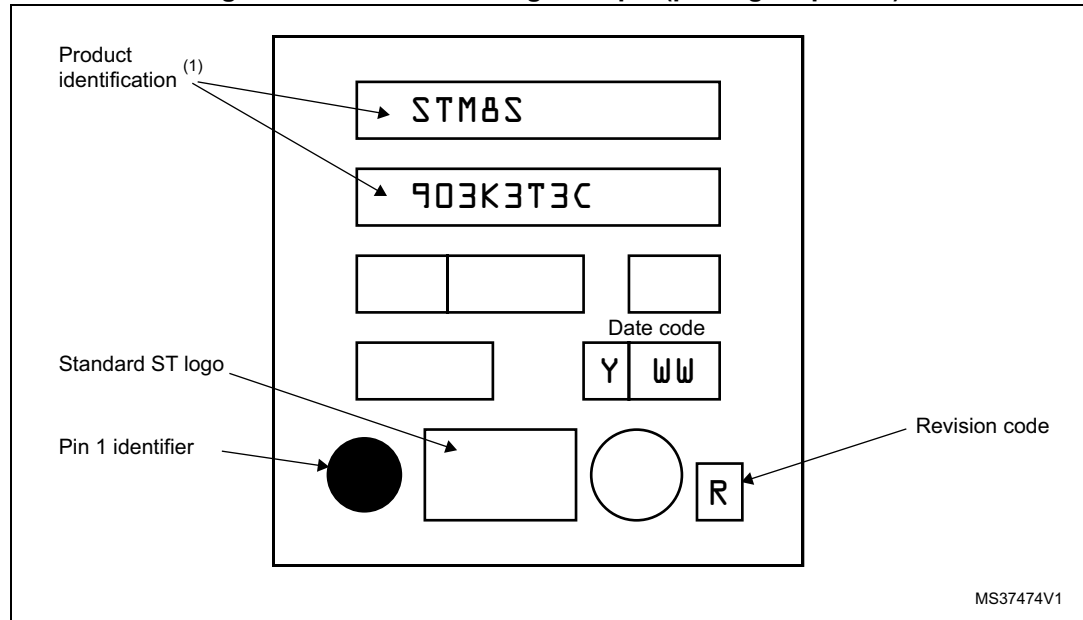
1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP32 marking example (package top view)



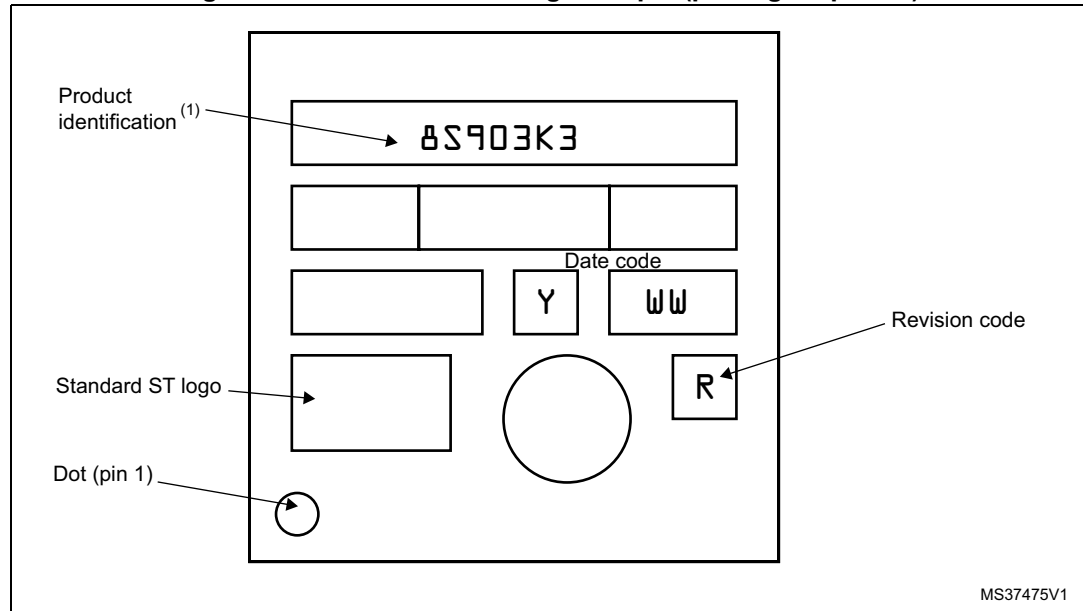
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. UFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.6 SO20 package information

Figure 59. SO20 package outline

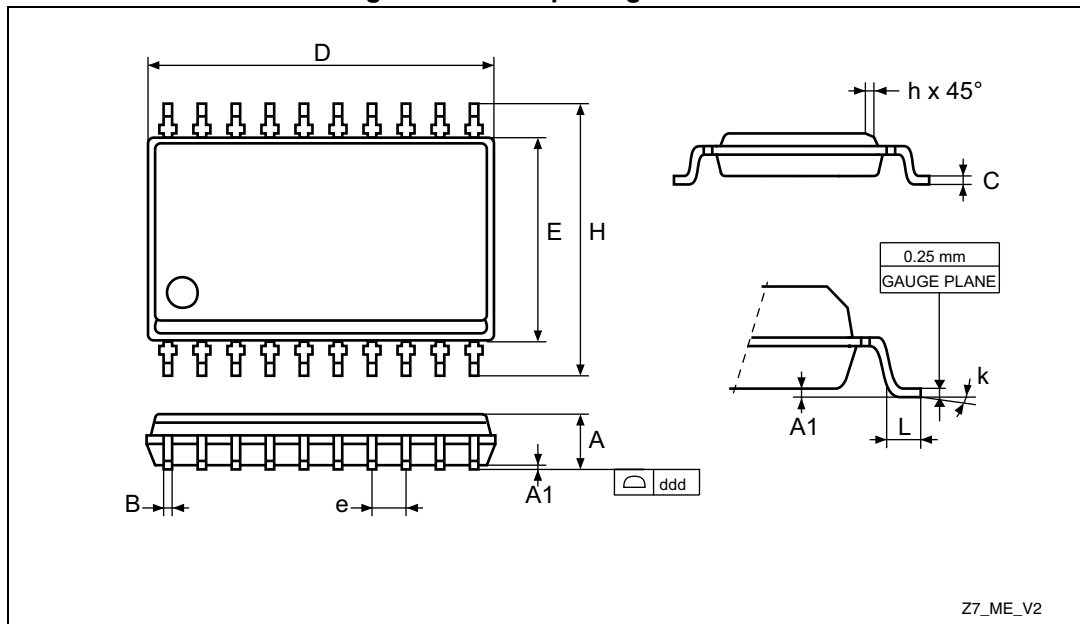


Table 59. SO20 mechanical data

Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	2.350	-	2.650	0.0925	-	0.1043
A1	0.100	-	0.300	0.0039	-	0.0118
B	0.330	-	0.510	0.013	-	0.0201
C	0.230	-	0.320	0.0091	-	0.0126
D	12.600	-	13.000	0.4961	-	0.5118
E	7.400	-	7.600	0.2913	-	0.2992
e	-	1.270	-	-	0.0500	-
H	10.000	-	10.650	0.3937	-	0.4193
h	0.250	-	0.750	0.0098	-	0.0295
L	0.400	-	1.270	0.0157	-	0.0500
k	0.0°	-	8.0°	0.0°	-	8.0°
ddd	-	-	0.100	-	-	0.0039

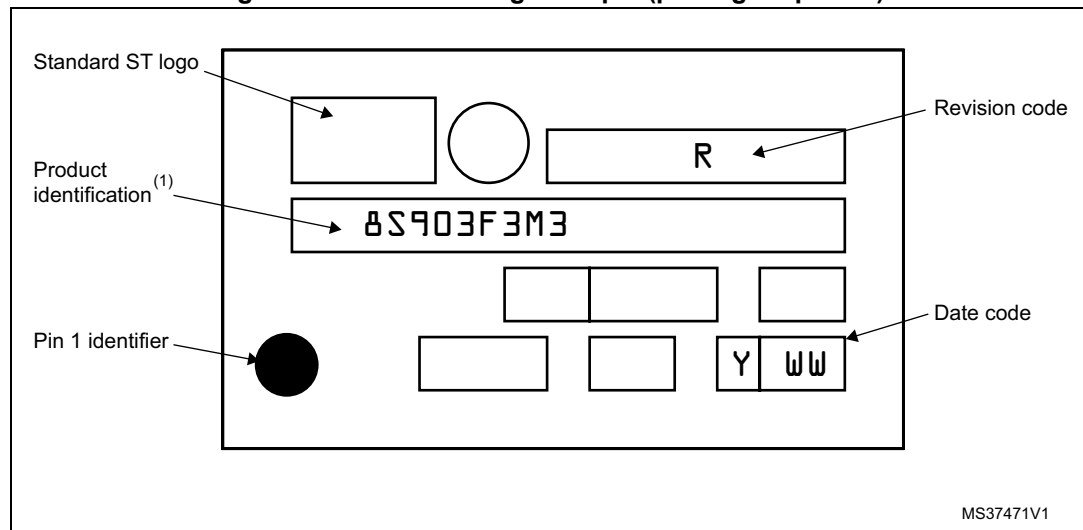
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 60. SO20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.7 UFQFPN recommended footprint

Figure 61. UFQFPN recommended footprint for on-board emulation

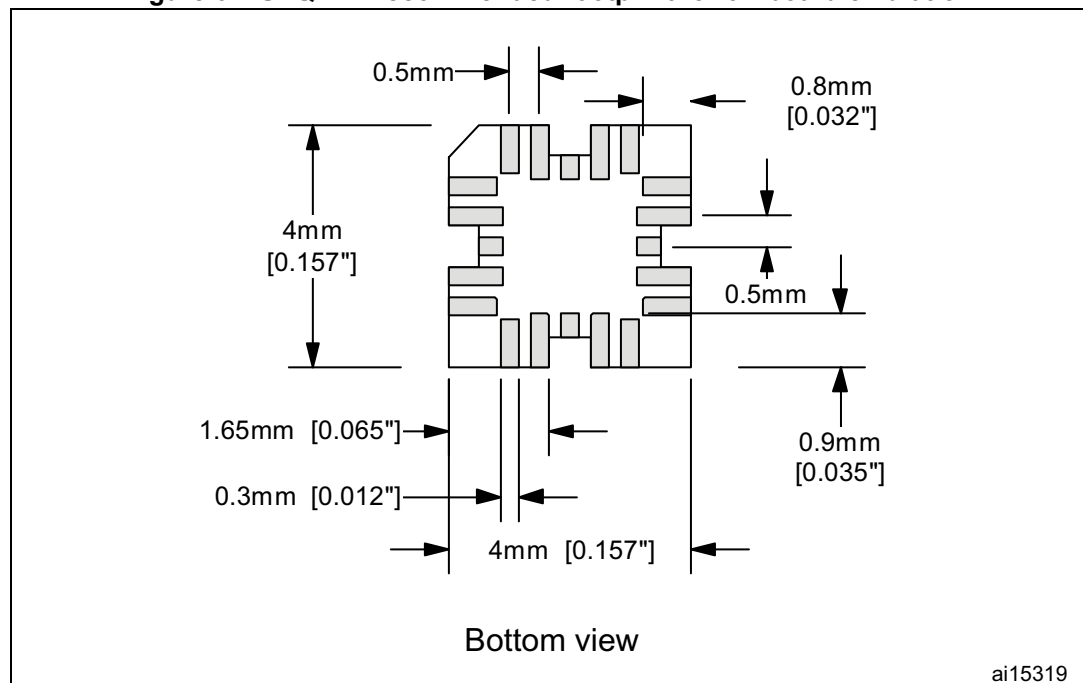


Table 61. Document revision history (continued)

Date	Revision	Changes
22-Apr-2010	3	<p>Added SO20W, TSSOP20, SDIP32, and UFQFPN32 packages.</p> <p>Added STM8S903F3 part number.</p> <p>Updated the document status to full datasheet.</p> <p>Updated the definition of alternate function remapping option in Table 4: Legend/abbreviations for pinout tables.</p> <p>Updated Px_IDR reset value in Table 7: I/O port hardware register map.</p> <p>Removed ESR low limit and update high limit for CEXT conditions in Table 21: General operating conditions.</p> <p>Updated VCAP and ESR low limit, added ESL parameter, as well as PD in Table 21: General operating conditions.</p> <p>Changed ESD to FESD (functional ESD); added name of AN1709; replaced IEC 1000 with IEC 61000 in Table 50: EMS data</p> <p>Replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to Table 51: EMI data.</p> <p>Replaced J 1752/3 with IEC 61967-2 and updated data of Table 51: EMI data.</p> <p>Removed note 3 related to Accuracy of HSI oscillator.</p> <p>Updated Θ_{JA} in Table 13: STM8S903K3 alternate function remapping bits [7:2] for 32-pin packages.</p> <p>Changed Θ_{JA} to 60°C/W in Section 12.2: Selecting the product temperature range.</p> <p>In Section 13: Ordering information, replaced package pitch digit by VFQFPN/UFQFPN package, and added footnote regarding possible future release of a dedicated ordering information scheme. Added SO20W, TSSOP20, SDIP32, and UFQFPN32.</p> <p>Added Section 13.1: STM8S903K3/F3 FASTROM microcontroller option list.</p>
30-Apr-2010	4	<p>Modified PD at TA = 85 °C for SO20W in Table 21: General operating conditions.</p>

Table 61. Document revision history (continued)

Date	Revision	Changes
23-Feb-2015	9	<p>Updated:</p> <ul style="list-style-type: none">– Section 11.5: TSSOP20 package information– Section 11.3: UFQFPN20 package information. <p>Added:</p> <ul style="list-style-type: none">– Figure 46: LQFP32 recommended footprint– Figure 47: LQFP32 marking example (package top view)– Figure 50: UFQFPN32 marking example (package top view)– Figure 53: UFQFPN20 marking example (package top view)– Figure 55: SDIP32 marking example (package top view)– Figure 57: TSSOP20 recommended package footprint– Figure 58: TSSOP20 marking example (package top view)– Figure 60: SO20 marking example (package top view)