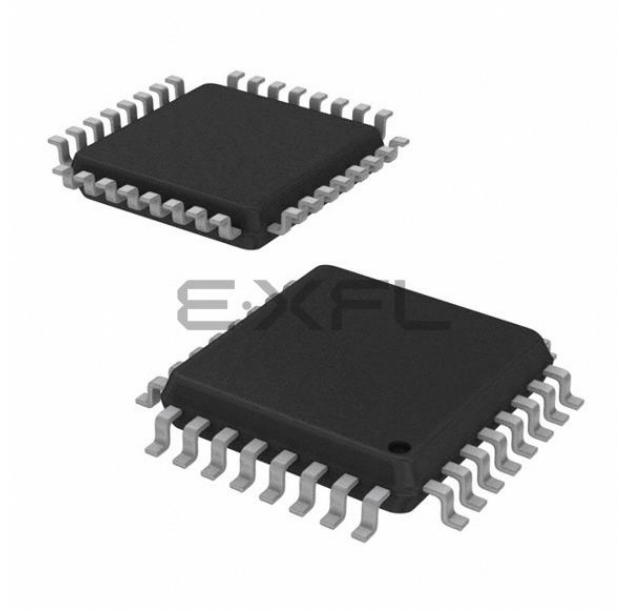

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 640 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.95V ~ 5.5V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903k3t3ctr |

# List of tables

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## 4.11 TIM5 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM6

## 4.12 TIM6 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM5.

**Table 3. TIM timer features**

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complementary outputs | Ext. trigger | Timer synchronization/ chaining |
|---|---|---|---|---|---|---|---|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/down | 4 | 3 | Yes | Yes |
| TIM5 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM6 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

## 5.3 TSSOP20, SO20 and UFQFPN20 pin descriptions

**Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions**

| TSSOP20 | UFQFPN20 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | floating | wpu | Ext. | High sink(1) | Speed | OD | PP | | | |
| 4 | 1 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 5 | 2 | PA1/ OSCIN(2) | I/O | **X** | X | X | - | O1 | X | X | Port A1 | Resonator/ crystal in | - |
| 6 | 3 | PA2/ OSCOUT | I/O | **X** | X | X | - | O1 | X | X | **Port A2** | Resonator/ crystal out | - |
| 7 | 4 | VSS | S | - | - | - | - | - | - | - | Digital ground | | - |
| 8 | 5 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 9 | 6 | VDD | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 10 | 7 | PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX] | I/O | **X** | X | X | HS | O3 | X | X | **Port A3** | Timer 52 channel 3 | SPI master/ slave select [AFR1]/ UART1 data transmit [AFR1:0] |
| 11 | 8 | PB5/ I2C_SDA [TIM1_BKIN] | I/O | **X** | - | X | - | O1 | T(3) | | **Port B5** | I2C data | Timer 1 - break input [AFR4] |
| 12 | 9 | PB4/ I2C_SCL [ADC_ETR] | I/O | **X** | - | X | - | O1 | T(3) | | **Port B4** | I2C clock | ADC external trigger [AFR4] |
| 13 | 10 | PC3/ TIM1_CH3/TLI/ [TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7] |
| 14 | 11 | PC4/ TIM1_CH4/ CLK_CCO/AIN2/ [TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C4 | Timer 1 - channel 4 /configurable clock output | Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7] |
| 15 | 12 | PC5/SPI_SCK [TIM5_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 5 channel 1 [AFR0] |
| 16 | 13 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C6 | PI master out/slave in | Timer 1 channel 1 [AFR0] |
| 17 | 14 | PC7/ SPI_MISO [TIM1_CH2] | I/O | **X** | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | Timer 1 channel 2[AFR0] |
| 18 | 15 | PD1/ SWIM(4) | I/O | X | X | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |

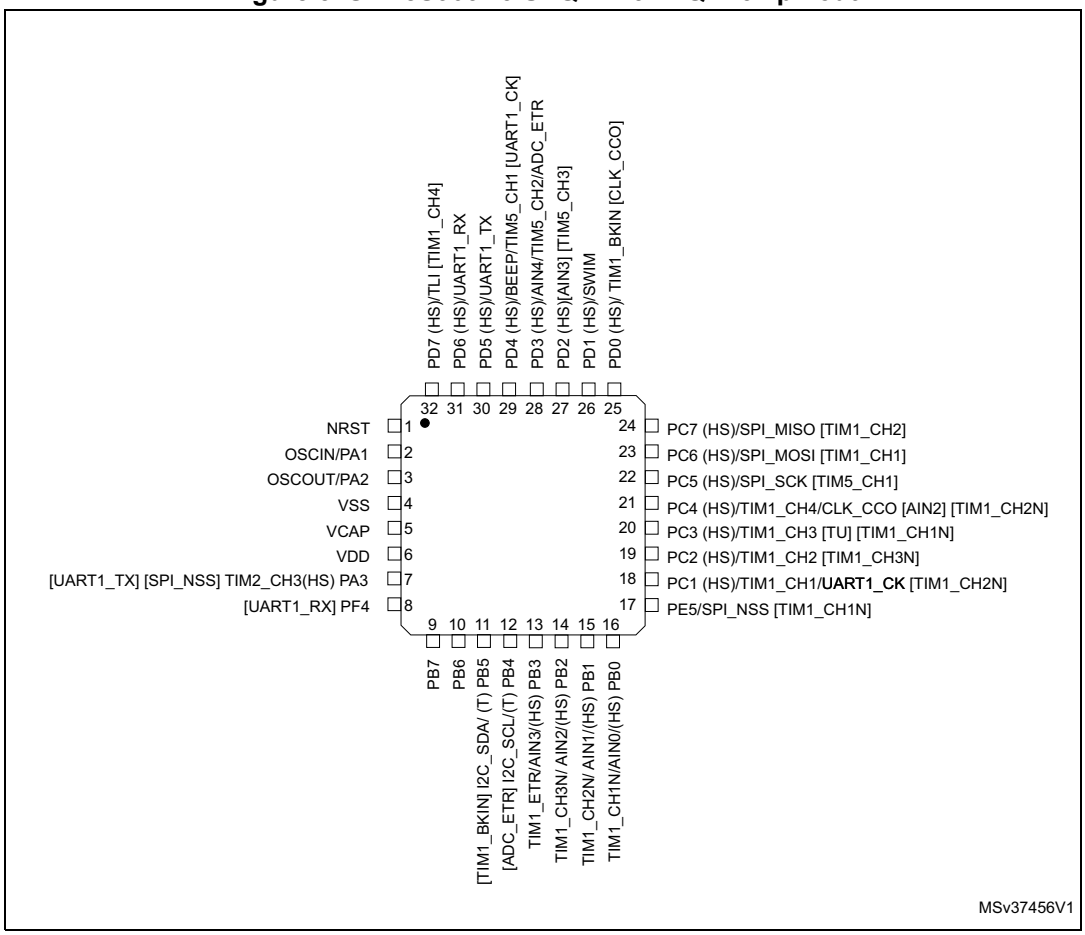
**Table 5. TSSOP20/SO20/UFQFPN20 pin descriptions (continued)**

| TSSOP20 | UFQFPN20 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | floating | wpu | Ext. | High sink(1) | Speed | OD | PP | | | |
| 19 | 16 | PD2/AIN3/ [TIM5_CH3] | I/O | **X** | X | X | HS | O3 | X | X | Port D2 | - | Analog input 3 [AFR2] Timer 52 - channel 3 [AFR1] |
| 20 | 17 | PD3/ AIN4/ TIM5_CH2/ ADC_ETR | I/O | **X** | X | X | HS | O3 | X | X | Port D3 | Analog input 4 Timer 52 - channel 2/ADC external trigger | - |
| 1 | 18 | PD4/ TIM5_CH1/ BEEP [UART1_CK] | I/O | **X** | X | X | HS | O3 | X | X | Port D4 | Timer 5 - channel 1/BEEP output | UART clock [AFR2] |
| 2 | 19 | PD5/ AIN5/ UART1_TX | I/O | **X** | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ UART1 data transmit | - |
| 3 | 20 | PD6/ AIN6/ UART1_RX | I/O | **X** | X | X | HS | O3 | X | X | Port D6 | Analog input 6/ UART1 data receive | - |

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10.2: Absolute maximum ratings*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, ‘T’ defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented)
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

## 5.4 STM8S903K3 UFQFPN32/LQFP32 and SDIP32 pinouts

**Figure 5. STM8S903K3 UFQFPN32/LQFP32 pinout**




1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to $V_{DD}$ not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

**Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)**

| SDIP32 | LQFP/ UFQFP32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 12 | 7 | PA3/ TIM5_CH3 [SPI_NSS] [UART1_TX] | I/O | **X** | X | X | HS | O3 | X | X | **Port A3** | Timer 5 channel 3 | SPI master/ slave select [AFR1] /UART1 data transmit [AFR 1:0] |
| 13 | 8 | PF4 [UART1_RX] | I/O | **X** | X | - | - | O1 | X | X | **Port F4** | - | UART1 data receive [AFR1:0] |
| 14 | 9 | PB7 | I/O | **X** | X | X | - | O1 | X | X | **Port B7** | - | - |
| 15 | 10 | PB6 | I/O | **X** | X | X | - | O1 | X | X | **Port B6** | - | - |
| 16 | 11 | PB5/ I2C_SDA [TIM1_BKIN] | I/O | **X** | - | X | - | O1 | T (3) | - | **Port B5** | I2C data | Timer 1 - break input [AFR4] |
| 17 | 12 | PB4/ I2C_SCL [ADC_ETR] | I/O | **X** | - | X | - | O1 | T | - | **Port B4** | I2C clock | ADC external trigger [AFR4] |
| 18 | 13 | PB3/ AIN3/TIM1_ETR | I/O | **X** | X | X | HS | O3 | X | X | **Port B3** | Analog input 3/ Timer 1 external trigger | - |
| 19 | 14 | PB2/ AIN2/ TIM1_CH3N | I/O | **X** | X | X | HS | O3 | X | X | **Port B2** | Analog input 2/ Timer 1 - inverted channel 3 | - |
| 20 | 15 | PB1/ AIN1/ TIM1_CH2N | I/O | **X** | X | X | HS | O3 | X | X | **Port B1** | Analog input 1/ Timer 1 - inverted channel 2 | - |
| 21 | 16 | PB0/ AIN0/ TIM1_CH1N | I/O | **X** | X | X | HS | O3 | X | X | **Port B0** | Analog input 0/ Timer 1 - inverted channel 1 | - |
| 22 | 17 | PE5/ SPI_NSS [TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port E5 | SPI master/slave select | Timer 1 - inverted channel 1 [AFR1:0] |
| 23 | 18 | PC1/ TIM1_CH1/ UART1_CK [TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C1 | Timer 1 - channel 1 UART1 clock | Timer 1 - inverted channel 2 [AFR1:0] |

**Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)**

| SDIP32 | LQFP/ UFQFP32 | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | floating | wpu | Ext. interrupt | High sink(1) | Speed | OD | PP | | | |
| 24 | 19 | PC2/ TIM1_CH2 [TIM1_CH3N] | I/O | **X** | X | X | HS | O3 | X | X | Port C2 | Timer 1 - channel 2 | Timer 1 - inverted channel 3 [AFR1:0] |
| 25 | 20 | PC3/ TIM1_CH3/TLI/ [TIM1_CH1N] | I/O | **X** | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | Top level interrupt [AFR3] Timer 1 inverted channel 1 [AFR7] |
| 26 | 21 | PC4/ TIM1_CH4/ CLK_CCO/AIN2/ [TIM1_CH2N] | I/O | **X** | X | X | HS | O3 | X | X | Port C4 | Timer 1 - channel 4 /configurable clock output | Analog input 2 [AFR2]Timer 1 inverted channel 2 [AFR7] |
| 27 | 22 | PC5/SPI_SCK [TIM5_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 5 channel 1 [AFR0] |
| 28 | 23 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | **X** | X | X | HS | O3 | X | X | Port C6 | SPI master out/slave in | Timer 1 channel 1 [AFR0] |
| 29 | 24 | PC7/ SPI_MISO [TIM1_CH2] | I/O | **X** | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | Timer 1 channel 2[AFR0] |
| 30 | 25 | PD0/ TIM1_BKIN [CLK_CCO] | I/O | **X** | X | X | HS | O3 | X | X | Port D0 | Timer 1 - break input | Configurable clock output [AFR5] |
| 31 | 26 | PD1/ SWIM(4) | I/O | **X** | X | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |
| 32 | 27 | PD2/AIN3/ [TIM5_CH3] | I/O | **X** | X | X | HS | O3 | X | X | Port D2 | - | Analog input 3 [AFR2] Timer 5 - channel 3 [AFR1] |
| 1 | 28 | PD3/ AIN4/ TIM5_CH2/ ADC_ETR | I/O | **X** | X | X | HS | O3 | X | X | Port D3 | Analog input 4 Timer 5 - channel 2/ADC external trigger | - |
| 2 | 29 | PD4/ TIM5_CH1/ BEEP [UART1_CK] | I/O | **X** | X | X | HS | O3 | X | X | Port D4 | Timer 5 - channel 1/BEEP output | UART clock [AFR2] |
| 3 | 30 | PD5/ AIN5/ UART1_TX | I/O | **X** | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ UART1 data transmit | - |

2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

### Total current consumption and timing in forced reset state

**Table 32. Total current consumption and timing in forced reset state**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD(R)}$ | Supply current in reset state(2) | $V_{DD}$ = 5 V | 400 | - | µA |
| | | $V_{DD}$ = 3.3 V | 300 | - | |
| $t_{RESETBL}$ | Reset pin release to vector fetch | - | - | 150 | µs |

1. Guaranteed by design.
2. Characterized with all I/Os tied to $V_{SS}$.

### Current consumption of on-chip peripherals

Subject to general operating conditions for $V_{DD}$ and $T_A$.

HSI internal RC/$f_{CPU}$= $f_{MASTER}$ = 16 MHz, $V_{DD}$ = 5 V

**Table 33. Peripheral current consumption**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $I_{DD(TIM1)}$ | TIM1 supply current(1) | 210 | µA |
| $I_{DD(TIM5)}$ | TIM5 supply current(1) | 130 | |
| $I_{DD(TIM6)}$ | TIM6 supply current(1) | 50 | |
| $I_{DD(UART1)}$ | UART1 supply current (2) | 120 | |
| $I_{DD(SPI)}$ | SPI supply current (2) | 45 | |
| $I_{DD(I2C)}$ | I2C supply current(2) | 65 | |
| $I_{DD(ADC1)}$ | ADC1 supply current when converting(3) | 1000 | |

1. Data based on a differential $I_{DD}$ measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

### Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

### HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Table 35. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | External high speed oscillator frequency | - | 1 | - | 16 | MHz |
| $R_F$ | Feedback resistor | - | - | 220 | - | kΩ |
| $C^{(1)}$ | Recommended load capacitance(2) | - | - | - | 20 | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF $f_{OSC}$ = 16 MHz | - | - | 6 (start up) 1.6 (stabilized)(3) | mA |
| | | C = 10 pF $f_{OSC}$ = 16 MHz | - | - | 6 (start up) 1.2 (stabilized)(3) | |
| $g_m$ | Oscillator transconductance | - | 5 | - | - | mA/V |
| $t_{SU(HSE)}^{(4)}$ | Startup time | $V_{DD}$ is stabilized | - | 1 | - | ms |

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

## 10.3.6 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 40. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | $V_{DD}$ = 5 V | -0.3 V | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage | | 0.7 x $V_{DD}$ | - | $V_{DD}$ + 0.3 V | |
| $V_{hys}$ | Hysteresis(1) | | - | 700 | - | mV |
| $R_{pu}$ | Pull-up resistor | $V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$ | 30 | 55 | 80 | kΩ |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 35(2) | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125(2) | |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 20 pF | - | - | 20(2) | ns |
| | | Standard and high sink I/Os Load = 20 pF | - | - | 50(2) | |
| $I_{lkg}$ | Digital input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1(3) | µA |
| $I_{lkg\ ana}$ | Analog input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±250(3) | nA |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O | Injection current ±4 mA | - | - | ±1(3) | µA |

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Guaranteed by characterization results

**Table 42. Output driving current (true open drain ports)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level with 2 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | - | 1.0 | V |
| | Output low level with 2 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 3.3 V | - | 1.5(1) | |
| $V_{OH}$ | Output high level with 2 pins sourced | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | - | 2.0(1) | |

1. Guaranteed by characterization results

**Table 43. Output driving current (high sink ports)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level with 8 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | - | 0.8 | V |
| | Output low level with 4 pins sunk | $I_{IO}$= 10 mA, $V_{DD}$ = 3.3 V | - | 1.0(1) | |
| | | $I_{IO}$= 20 mA, $V_{DD}$ = 5 V | - | 1.5(1) | |
| $V_{OH}$ | Output high level with 8 pins sourced | $I_{IO}$= 10 mA, $V_{DD}$ = 5 V | 4.0 | - | |
| | Output high level with 4 pins sourced | $I_{IO}$= 10 mA, $V_{DD}$ = 3.3 V | 2.1(1) | - | |
| | | $I_{IO}$= 20 mA, $V_{DD}$ = 5 V | 3.3(1) | - | |

1. Guaranteed by characterization results.

**Figure 25. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (standard ports)**

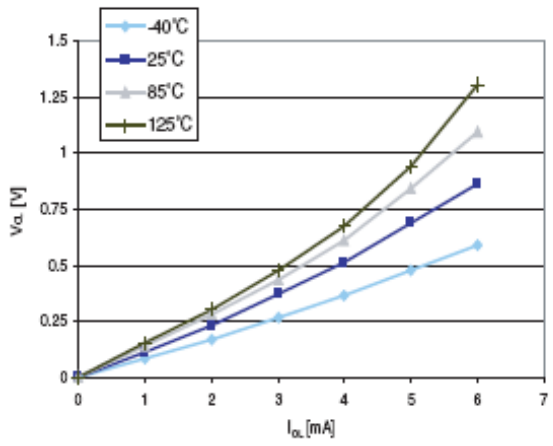



**Figure 26. Typ. $V_{OL}$ @ $V_{DD}$ = 5.0 V (standard ports)**

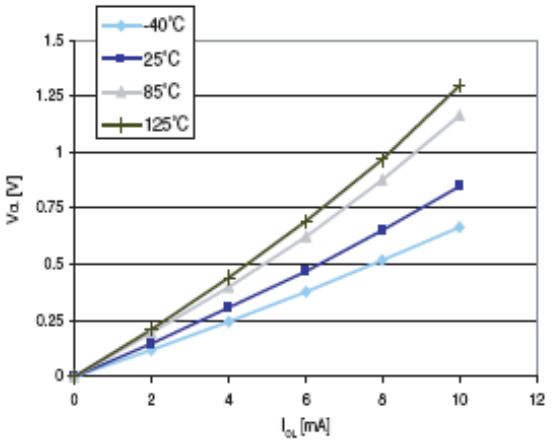
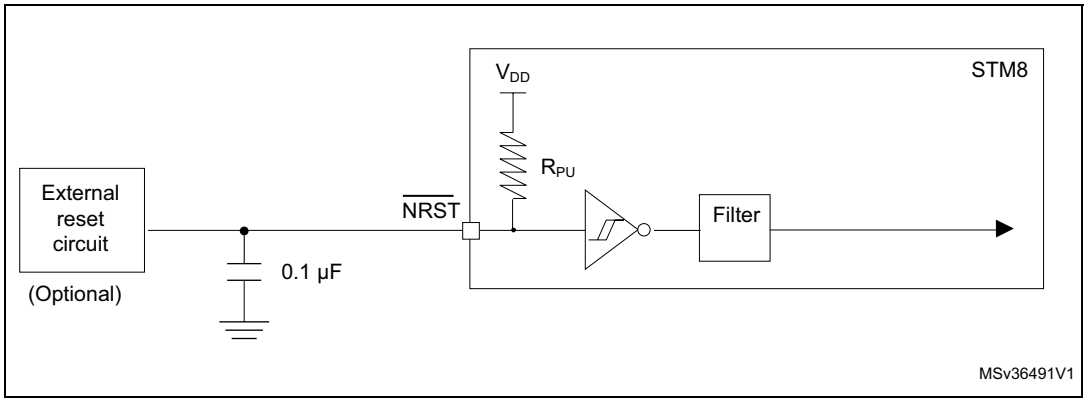


**Figure 38. Recommended reset pin protection**




## 10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 45. SPI characteristics**

| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 7 | |

**Table 45. SPI characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 25 | ns |
| $t_{su(NSS)}$[2] | NSS setup time | Slave mode | 4 * $t_{MASTER}$ | - | |
| $t_{h(NSS)}$[2] | NSS hold time | Slave mode | 70 | - | |
| $t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2] | SCK high and low time | Master mode | $t_{SCK}/2$ - 15 | $t_{SCK}/2$ + 15 | |
| $t_{su(MI)}$[2] $t_{su(SI)}$[2] | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$[2] $t_{h(SI)}$[2] | Data input hold time | Master mode | 7 | - | |
| | | Slave mode | 10 | - | |
| $t_{a(SO)}$[2][3] | Data output access time | Slave mode | - | 3* $t_{MASTER}$ | |
| $t_{dis(SO)}$[2][4] | Data output disable time | Slave mode | 25 | - | |
| $t_{v(SO)}$[2] | Data output valid time | Slave mode (after enable edge) | - | 65 | |
| $t_{v(MO)}$[2] | Data output valid time | Master mode (after enable edge) | - | 30 | |
| $t_{h(SO)}$[2] | Data output hold time | Slave mode (after enable edge) | 27 | - | |
| $t_{h(MO)}$[2] | | Master mode (after enable edge) | 11 | - | |

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

**Table 48. ADC accuracy with $R_{AIN}$< 10 kΩ, $V_{DD}$= 5 V**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $\|E_T\|$ | Total unadjusted error(2) | $f_{ADC}$ = 2 MHz | 1.6 | 3.5 | LSB |
| | | $f_{ADC}$ = 4 MHz | 2.2 | 4 | |
| | | $f_{ADC}$ = 6 MHz | 2.4 | 4.5 | |
| $\|E_O\|$ | Offset error(2) | $f_{ADC}$ = 2 MHz | 1.1 | 2.5 | |
| | | $f_{ADC}$ = 4 MHz | 1.5 | 3 | |
| | | $f_{ADC}$ = 6 MHz | 1.8 | 3 | |
| $\|E_G\|$ | Gain error(2) | $f_{ADC}$ = 2 MHz | 1.5 | 3 | |
| | | $f_{ADC}$ = 4 MHz | 2.1 | 3 | |
| | | $f_{ADC}$ = 6 MHz | 2.2 | 4 | |
| $\|E_D\|$ | Differential linearity error(2) | $f_{ADC}$ = 2 MHz | 0.7 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.7 | 1.5 | |
| | | $f_{ADC}$ = 6 MHz | 0.7 | 1.5 | |
| $\|E_L\|$ | Integral linearity error(2) | $f_{ADC}$ = 2 MHz | 0.6 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.8 | 2 | |
| | | $f_{ADC}$ = 6 MHz | 0.8 | 2 | |

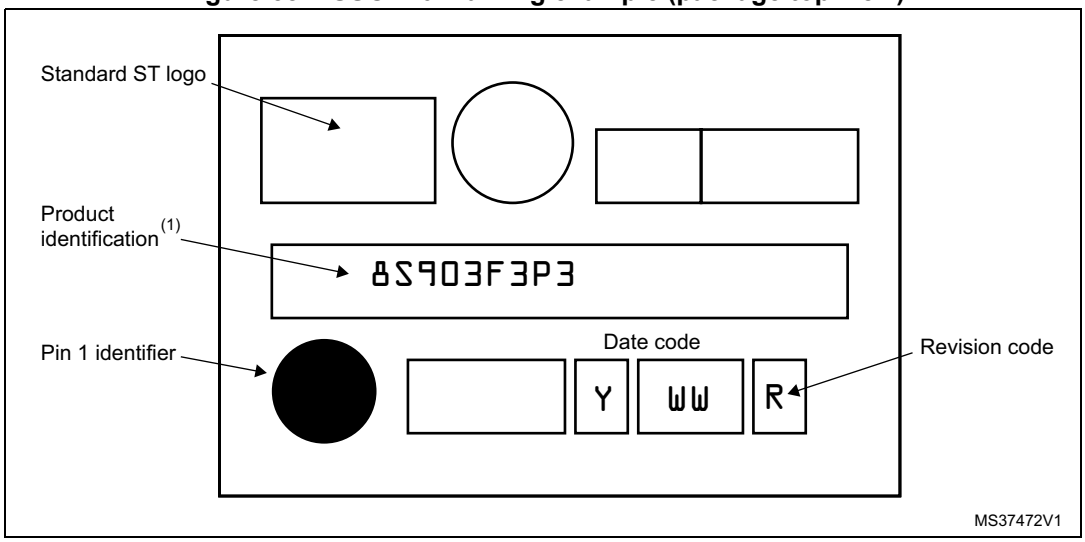
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 58. TSSOP20 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Three characters are reserved for code identification.

### Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

### Padding value for unused program memory (check only one option)

| | |
|---|---|
| [ ] 0xFF | Fixed value |
| [ ] 0x83 | TRAP instruction code |
| [ ] 0x75 | Illegal opcode (causes a reset when executed) |

### OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

### OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

| | |
|---|---|
| UBC, bit0 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit1 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit2 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit3 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit4 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit5 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit6 | [ ] 0: Reset<br>[ ] 1: Set |
| UBC, bit7 | [ ] 0: Reset<br>[ ] 1: Set |

*Note: If the UBC area is not used, please select all bits at reset states.*

### OTP2 alternate function remapping for STM8S903K3

Do not use more than one remapping option in the same port.

| | |
|---|---|
| AFR1, AFR0<br>(check only one option) | [ ] 00: Remapping options inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 01: Port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, and port C7 alternate function = TIM1_CH2.<br>[ ] 10: Port A3 alternate function = SPI_NSS and port D2 alternate function = TIM5_CH3.<br>[ ] 11: Port D2 alternate function = TIM5_CH3, port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, port C7 alternate function = TIM1_CH2, port C2 alternate function = TIM1_CH3N, port C1 alternate function = TIM1_CH2N, port E5 alternate function = TIM1_CH1N, port A3 alternate function = UART1_TX, and port F4 alternate function = UART1_RX. |
| AFR2<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port C4 alternate function = AIN2, port D2 alternate function = AIN3, port D4 alternate function = UART1_CK. |
| AFR3<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port C3 alternate function = TLI. |
| AFR4<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port B4 alternate function = ADC_ETR, port B5 alternate function = TIM1_BKIN. |
| AFR5<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port D0 alternate function = CLK_CCO. |
| AFR6<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port D7 alternate function = TIM1_CH4. |
| AFR7<br>(check only one option) | [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.<br>[ ] 1: Port C3 alternate function = TIM1_CH1N, port C4 alternate function = TIM1_CH2N. |

## 14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

### 14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

#### ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

#### ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

### 14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

#### C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

#### STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

# 15 Revision history

**Table 61. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 30-Apr-2009 | 1 | Initial release. |
| 03-Jun-2009 | 2 | – Added bullet point concerning unique identifier to *Features* section on cover page.<br>– Highlighted internal reference voltage in *Section 4.13: Analog-to-digital converter (ADC1)*.<br>– Updated wpu and PP status of PB5/12C_SDA[TIM1_BKIN] and PB4/12C_SCL[ADC_ETR] pins in *Section 5: Pinouts and pin descriptions*.<br>– Updated *Section 6.1: Memory map*.<br>– Added *Section 9: Unique ID*.<br>– Added TBD values to *Table 45: SPI characteristics*.<br>– Added max values to *Table 48: ADC accuracy with $R_{AIN}$< 10 kΩ $V_{DD}$= 5 V* and *Table 49: ADC accuracy with $R_{AIN}$< 10 kΩ $V_{DD}$= 3.3 V*. |