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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903k3u6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s903k3u6tr</a>

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## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

## 4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. **Timeout:** At 16 MHz CPU clock the time-out period can be adjusted between 75  $\mu$ s up to 64 ms.
2. **Refresh out of window:** The downcounter is refreshed before its value is lower than the one stored in the window register.

### Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60  $\mu$ s to 1 s.

## 4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

## 4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

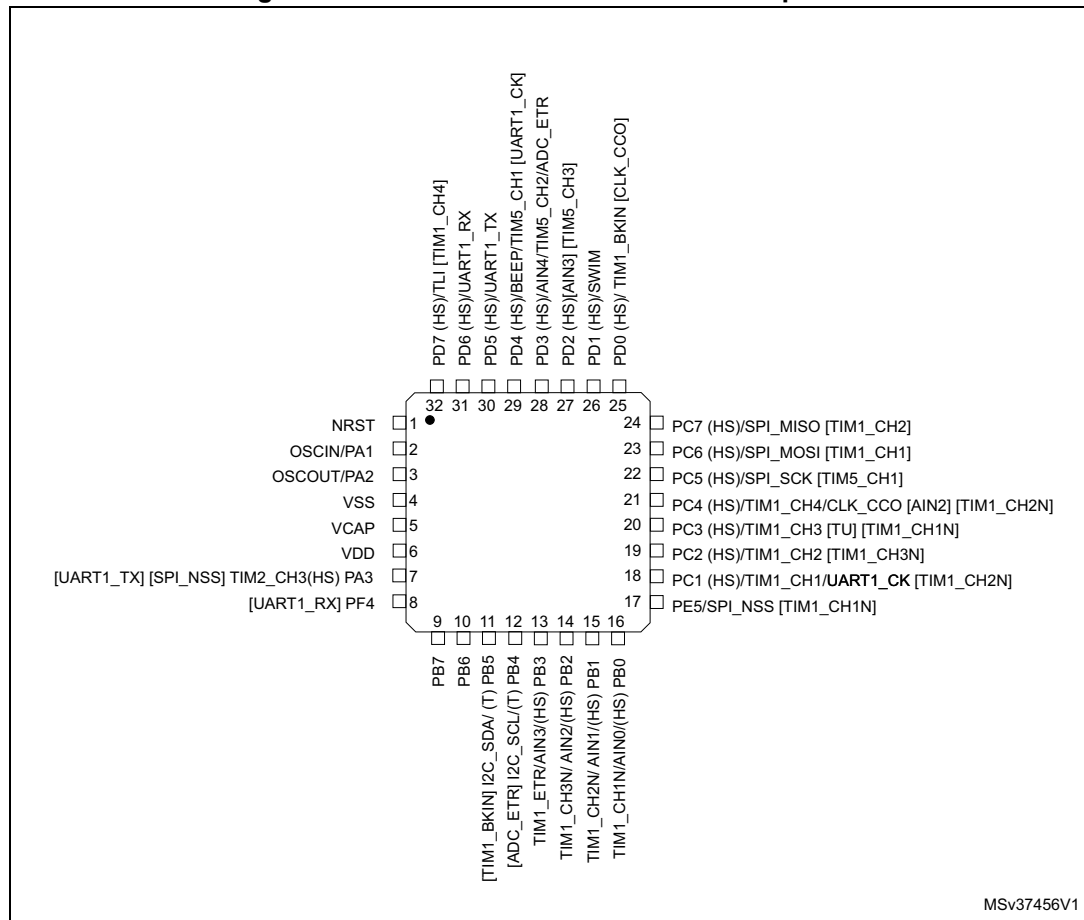
## 4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals or to synchronize with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break
-

## 5.4 STM8S903K3 UFQFPN32/LQFP32 and SDIP32 pinouts

Figure 5. STM8S903K3 UFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to  $V_{DD}$  not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S903K3 UFQFPN32/LQFP32/SDIP32 pin descriptions (continued)

SDIP32	LQFP/UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink <sup>(1)</sup>	Speed	OD	PP			
4	31	PD6/ AIN6/ UART1_RX	I/O	X	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
5	32	PD7/ TLI [TIM1_CH4]	I/O	X	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see [Section 10: Electrical characteristics](#)).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V<sub>DD</sub> are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

## 6.2 Register map

### 6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xFF <sup>(1)</sup>
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xFF <sup>(1)</sup>
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xFF <sup>(1)</sup>
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xFF <sup>(1)</sup>
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xFF <sup>(1)</sup>
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xFF <sup>(1)</sup>
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C Own address register low	0x00
0x00 5214		I2C_OARH	I2C Own address register high	0x00
0x00 5215		Reserved		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x0X
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xFF
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (21 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF
0x00 5349 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC_DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			

## 9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

**Table 17. Unique ID registers (96 bits)**

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4865	X co-ordinate on the wafer	U_ID[7:0]							
0x4866		U_ID[15:8]							
0x4867	Y co-ordinate on the wafer	U_ID[23:16]							
0x4868		U_ID[31:24]							
0x4869	Wafer number	U_ID[39:32]							
0x486A	Lot number	U_ID[47:40]							
0x486B		U_ID[55:48]							
0x486C		U_ID[63:56]							
0x486D		U_ID[71:64]							
0x486E		U_ID[79:72]							
0x486F		U_ID[87:80]							
0x4870		U_ID[95:88]							

Table 19. Current characteristics (continued)

Symbol	Ratings	Max. <sup>(1)</sup>	Unit
$I_{INJ(PIN)}^{(3)(4)}$	Injected current on NRST pin	±4	mA
	Injected current on OSCIN pin	±4	
	Injected current on any other pin <sup>(5)</sup>	±4	
$\Sigma I_{INJ(PIN)}^{(3)}$	Total injected current (sum of all I/O and control pins) <sup>(5)</sup>	±20	

1. Guaranteed by characterization results.
2. All power ( $V_{DD}$ ,  $V_{DDIO}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSIO}$ ,  $V_{SSA}$ ) pins must always be connected to the external supply.
3.  $I_{INJ(PIN)}$  must never be exceeded. This condition is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ . For true open-drain pads, there is no positive injection current allowed and the corresponding  $V_{IN}$  maximum must always be respected.
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to 150	°C
$T_J$	Maximum junction temperature	150	

## 10.3 Operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{CPU}$	Internal CPU clock frequency	-	0	16	MHz
$V_{DD}/V_{DDIO}$	Standard operating voltage	-	2.95	5.5	V
$V_{CAP}^{(1)}$	$C_{EXT}$ : capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz <sup>(2)</sup>	-	0.3	Ω
	ESL of external capacitor		-	15	nH
$P_D^{(3)}$	Power dissipation at $T_A = 85^\circ\text{C}$ for suffix 6	TSSOP20	-	182	mW
		SO20W	-	1000	
		UFQFPN20	-	198	
		LQFP32	-	333	
		UFQFPN32	-	526	
		SDIP32	-	333	

2. Measured from interrupt event to interrupt vector fetch
3.  $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK\_ICR register.
5. Configured by the AHALT bit in the FLASH\_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

### Total current consumption and timing in forced reset state

**Table 32. Total current consumption and timing in forced reset state**

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>	Unit
$I_{DD(R)}$	Supply current in reset state <sup>(2)</sup>	$V_{DD} = 5\text{ V}$	400	-	$\mu\text{A}$
		$V_{DD} = 3.3\text{ V}$	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	$\mu\text{s}$

1. Guaranteed by design.
2. Characterized with all I/Os tied to  $V_{SS}$ .

### Current consumption of on-chip peripherals

Subject to general operating conditions for  $V_{DD}$  and  $T_A$ .

HSI internal  $RC/f_{CPU} = f_{MASTER} = 16\text{ MHz}$ ,  $V_{DD} = 5\text{ V}$

**Table 33. Peripheral current consumption**

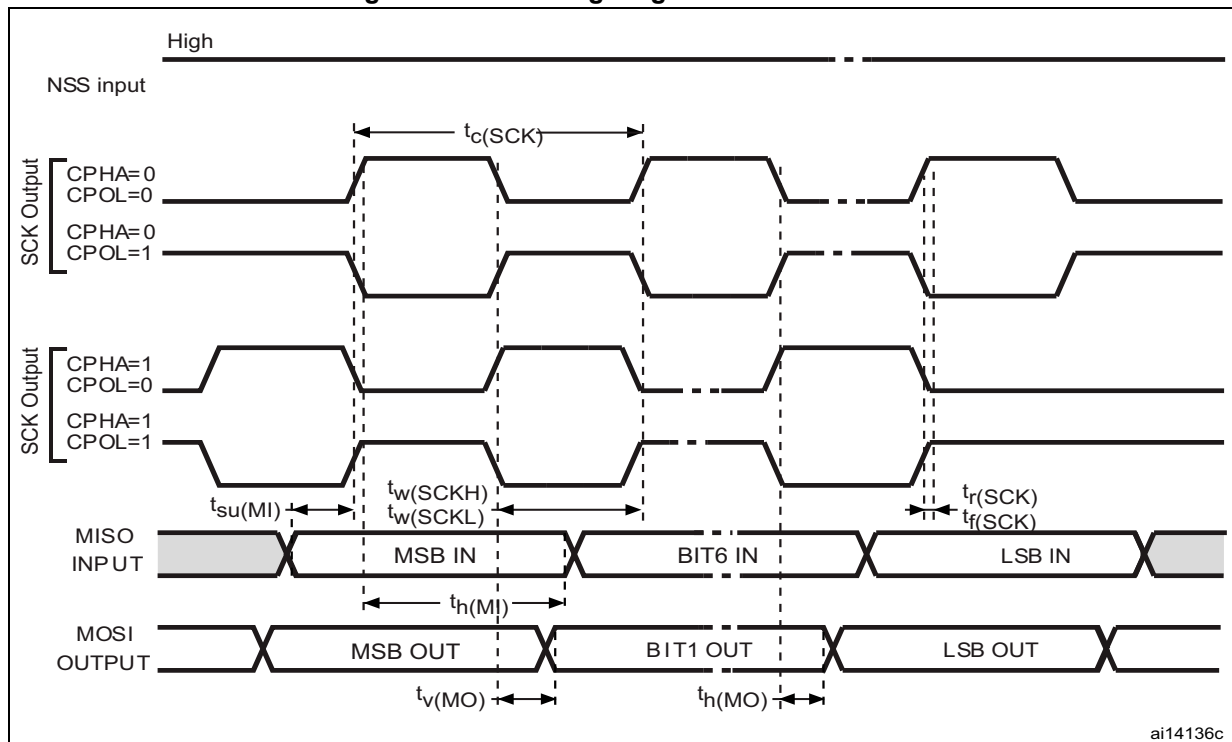
Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current <sup>(1)</sup>	210	$\mu\text{A}$
$I_{DD(TIM5)}$	TIM5 supply current <sup>(1)</sup>	130	
$I_{DD(TIM6)}$	TIM6 supply current <sup>(1)</sup>	50	
$I_{DD(UART1)}$	UART1 supply current <sup>(2)</sup>	120	
$I_{DD(SPI)}$	SPI supply current <sup>(2)</sup>	45	
$I_{DD(I2C)}$	I2C supply current <sup>(2)</sup>	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting <sup>(3)</sup>	1000	

1. Data based on a differential  $I_{DD}$  measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential  $I_{DD}$  measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential  $I_{DD}$  measurement between reset configuration and continuous A/D conversions. Not tested in production.

### Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 41. SPI timing diagram - master mode



1. Measurement points are at CMOS levels:  $0.3 V_{DD}$  and  $0.7 V_{DD}$ .

### Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

**Table 51. EMI data**

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f <sub>CPU</sub> <sup>(1)</sup>		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 5 V, T <sub>A</sub> = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBμV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level	EMI level	2.5	2.5	-	

1. Guaranteed by characterization results.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**Table 52. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	$T_A = 25\text{ }^{\circ}\text{C}$ , conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	$T_A = 25\text{ }^{\circ}\text{C}$ , conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

### Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

The drawing shows a rectangular connector with a total width of 9.70 and a total height of 9.70. The pin layout is as follows:

- Top Row:** 8 pins, numbered 24 on the left and 17 on the right. The pitch between pins is 0.80. The height of the pins is 1.20.
- Left Column:** 6 pins, numbered 25 at the top and 32 at the bottom. The pitch between pins is 6.10. The height of the pins is 1.20.
- Right Column:** 6 pins, numbered 16 at the top and 9 at the bottom. The pitch between pins is 6.10. The height of the pins is 1.20.
- Bottom Row:** 8 pins, numbered 1 on the left and 8 on the right. The pitch between pins is 6.10. The height of the pins is 1.20.

Additional dimensions include a 0.30 offset for the right column pins and a 0.50 offset for the top right pin (16).

Table 57. SDIP32 package mechanical data (continued)

Dim.	mm			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
eB	-	-	12.700	-	-	0.5000
L	2.540	3.048	3.810	0.1000	0.1200	0.1500

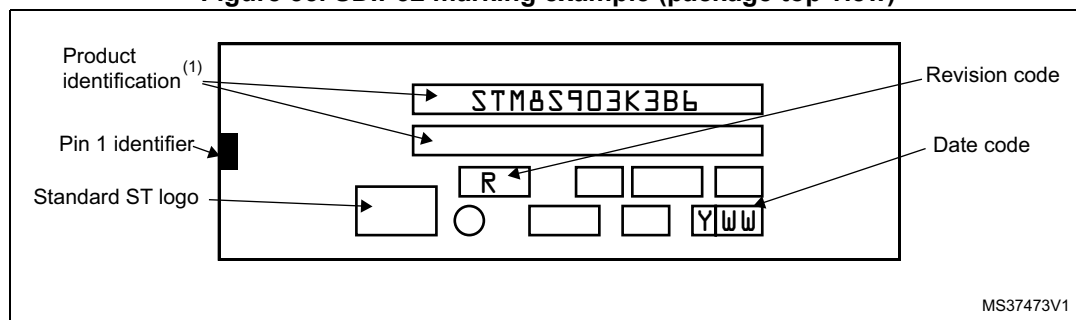
1. Values in inches are converted from mm and rounded to 4 decimal digits

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 55. SDIP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 12 Thermal characteristics

The maximum junction temperature ( $T_{Jmax}$ ) of the device must never exceed the values specified in [Table 21: General operating conditions](#), otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature  $T_{Jmax}$ , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- $T_{Amax}$  is the maximum ambient temperature in °C
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance in °C/W
- $P_{Dmax}$  is the sum of  $P_{INTmax}$  and  $P_{I/Omax}$  ( $P_{Dmax} = P_{INTmax} + P_{I/Omax}$ )
- $P_{INTmax}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$  represents the maximum power dissipation on output pins

Where:

$$P_{I/Omax} = \Sigma (V_{OL} \cdot I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \cdot I_{OH}),$$

taking into account the actual  $V_{OL}/I_{OL}$  and  $V_{OH}/I_{OH}$  of the I/Os at low and high level in the application.

**Table 60. Thermal characteristics<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	Thermal resistance junction-ambient TSSOP20 - 4.4mm	110	°C/W
	Thermal resistance junction-ambient SO20W (300 mils)	20	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	101	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm	38	
	Thermal resistance junction-ambient SDIP32 - 400 mils	60	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

### 12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from [www.jedec.org](http://www.jedec.org).

## 12.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see [Section 13: Ordering information](#)).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 75^{\circ}\text{C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 8\text{ mA}$ ,  $V_{DD} = 5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with

$$I_{OL} = 8\text{ mA}, V_{OL} = 0.4\text{ V}$$

$$P_{INTmax} = 8\text{ mA} \times 5\text{ V} = 400\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 400\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 400\text{ mW} + 64\text{ mW}$$

Thus:  $P_{Dmax} = 464\text{ mW}$ .

Using the values obtained in [Table 60: Thermal characteristics on page 107](#)  $T_{Jmax}$  is calculated as follows:

For LQFP32  $60^{\circ}\text{C/W}$

$$T_{Jmax} = 75^{\circ}\text{C} + (60^{\circ}\text{C/W} \times 464\text{ mW}) = 75^{\circ}\text{C} + 27.8^{\circ}\text{C} = 102.8^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105^{\circ}\text{C}$ ).

Parts must be ordered at least with the temperature range suffix 6.

## 13 Ordering information

Figure 63. STM8S903K3/F3 access line ordering information scheme<sup>(1)</sup>

<b>Example:</b>	STM8	S	903	K	3	T	6	C	TR
<b>Product class</b>	STM8 microcontroller								
<b>Family type</b>	S = Standard								
<b>Sub-family type</b>	903 = 903 sub-family								
<b>Pin count</b>	K = 32 pins F = 20 pins								
<b>Program memory size</b>	3 = 8 Kbytes								
<b>Package type</b>	B = SDIP T = LQFP U = VFQFPN P = TSSOP M = SO								
<b>Temperature range</b>	3 = -40 to 125 °C 6 = -40 to 85 °C								
<b>Package pitch</b>	Blank = 0.5 to 0.65 mm <sup>(2)</sup> C = 0.8 mm <sup>(3)</sup>								
<b>Packing</b>	No character = Tray or tube TR = Tape and reel								

1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required. The letter "P" will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP903K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

**OTP2 alternate function remapping for STM8S903K3**

Do not use more than one remapping option in the same port.

AFR1, AFR0 (check only one option)	<p><input type="checkbox"/> 00: Remapping options inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 01: Port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, and port C7 alternate function = TIM1_CH2.</p> <p><input type="checkbox"/> 10: Port A3 alternate function = SPI_NSS and port D2 alternate function = TIM5_CH3.</p> <p><input type="checkbox"/> 11: Port D2 alternate function = TIM5_CH3, port C5 alternate function = TIM5_CH1, port C6 alternate function = TIM1_CH1, port C7 alternate function = TIM1_CH2, port C2 alternate function = TIM1_CH3N, port C1 alternate function = TIM1_CH2N, port E5 alternate function = TIM1_CH1N, port A3 alternate function = UART1_TX, and port F4 alternate function = UART1_RX.</p>
AFR2 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port C4 alternate function = AIN2, port D2 alternate function = AIN3, port D4 alternate function = UART1_CK.</p>
AFR3 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port C3 alternate function = TLI.</p>
AFR4 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port B4 alternate function = ADC_ETR, port B5 alternate function = TIM1_BKIN.</p>
AFR5 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port D0 alternate function = CLK_CCO.</p>
AFR6 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port D7 alternate function = TIM1_CH4.</p>
AFR7 (check only one option)	<p><input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description.</p> <p><input type="checkbox"/> 1: Port C3 alternate function = TIM1_CH1N, port C4 alternate function = TIM1_CH2N.</p>

## 15 Revision history

Table 61. Document revision history

Date	Revision	Changes
30-Apr-2009	1	Initial release.
03-Jun-2009	2	<ul style="list-style-type: none"> <li>– Added bullet point concerning unique identifier to <a href="#">Features</a> section on cover page.</li> <li>– Highlighted internal reference voltage in <a href="#">Section 4.13: Analog-to-digital converter (ADC1)</a>.</li> <li>– Updated wpu and PP status of PB5/12C_SDA[TIM1_BKIN] and PB4/12C_SCL[ADC_ETR] pins in <a href="#">Section 5: Pinouts and pin descriptions</a>.</li> <li>– Updated <a href="#">Section 6.1: Memory map</a>.</li> <li>– Added <a href="#">Section 9: Unique ID</a>.</li> <li>– Added TBD values to <a href="#">Table 45: SPI characteristics</a>.</li> <li>– Added max values to <a href="#">Table 48: ADC accuracy with <math>R_{AIN} &lt; 10\text{ k}\Omega</math> <math>V_{DD} = 5\text{ V}</math></a> and <a href="#">Table 49: ADC accuracy with <math>R_{AIN} &lt; 10\text{ k}\Omega</math> <math>V_{DD} = 3.3\text{ V}</math></a>.</li> </ul>