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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	· ·
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg895f256-bga120

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG895 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG895 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

2.1.12 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.13 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.14 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.15 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.16 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.17 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.18 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.3 Memory Map

The *EFM32WG895* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG895 Memory Map with largest RAM and Flash sizes





Symbol	Parameter	Condition	Min	Тур	Max	Unit
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} =85°C		3.0 ¹	4.0 ¹	μΑ
	EM3 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.65	1.3	μA
I'EM3		V _{DD} = 3.0 V, T _{AMB} =85°C		2.65	4.0	μA
I _{EM4}	EM4 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.02	0.055	μA
	EIVI4 CUITENT	V _{DD} = 3.0 V, T _{AMB} =85°C		0.44	0.9	μA

¹Using backup RTC.

3.4.1 EM1 Current Consumption

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Figure 3.1. EM1 Current consumption with all peripheral clocks disabled and HFXO running at 48MHz
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Figure 3.2. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28MHz





Figure 3.3. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz



Figure 3.4. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz





Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V _{DD}	V
I _{IOLEAK}	Input leakage cur- rent	High Impedance IO connected to GROUND or Vdd		±0.1	±100	nA
R _{PU}	I/O pin pull-up resis- tor			40		kOhm
R _{PD}	I/O pin pull-down re- sistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of puls- es to be removed by the glitch sup- pression filter		10		50	ns
•	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capaci- tance C_L =12.5-25pF.	20+0.1C _L		250	ns
tioof			20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.10V _{DD}			V

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{LFRCO}	Oscillation frequen- cy , V_{DD} = 3.0 V, T_{AMB} =25°C		31.29	32.768	34.28	kHz
t _{LFRCO}	Startup time not in- cluding software calibration			150		μs
I _{LFRCO}	Current consump- tion			300		nA
TUNESTEP _L . FRCO	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.17. Calibrated LFRCO Frequency vs Temperature and Supply Voltage





Figure 3.19. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature



Figure 3.20. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature



Figure 3.21. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature







Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		79		dBc
	Offset voltage	After calibration, single ended	-3.5	0.3	3	mV
ADCOFFSET		After calibration, differential		0.3		mV
				-1.92		mV/°C
TGRAD _{ADCTH}	Thermometer out- put gradient			-6.3		ADC Codes/ °C
DNL _{ADC}	Differential non-lin- earity (DNL)		-1	±0.7	4	LSB
INL _{ADC}	Integral non-linear- ity (INL), End point method			±1.2	±3	LSB
MC _{ADC}	No missing codes		11.999 ¹	12		bits
CAIN	Coip orror drift	1.25V reference		0.01 ²	0.033 ³	%/°C
GAINED		2.5V reference		0.01 ²	0.03 ³	%/°C
OFFRET	Offect error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
OFFSET _{ED}	Offset error drift	2.5V reference		0.2 ²	0.62 ³	LSB/°C

¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by abs(Mean) / (85 - 25).

³Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.24 (p. 37) and Figure 3.25 (p. 37), respectively.



Figure 3.24. Integral Non-Linearity (INL)



Figure 3.25. Differential Non-Linearity (DNL)



Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C





Figure 3.29. ADC Absolute Offset, Common Mode = Vdd /2



Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V





Figure 3.40. EBI Read Enable Related Output Timing



Table 3.22. EBI Read Enable Related Output Timing

Symbol	Parameter	Min	Тур	Мах	Unit
t _{OH_REn} ¹²³⁴	Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-10.00 + (RDHOLD * thfcoreclk)			ns
tosu_REn ¹²³⁴⁵	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge	-10.00 + (RDSETUP ^{* t} hfcoreclk)			ns
twiDTH_REn ¹²³⁴⁵⁶	EBI_REn pulse width	-9.00 + ((RD- STRB+1) * t _{HFCORE-} _{CLK})			ns

¹Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

²Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

 $^4\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $_{\text{VDD}})$

⁵The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * $t_{HFCLKNODIV}$.

⁶When page mode is used, RDSTRB is replaced by RDPA for page hits.

3.17 I2C

Table 3.26	. <i>1</i> 2C	Standard-mode	(Sm)
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Symbol	Parameter	Min	Тур	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and a START condi- tion	4.7			μs

¹For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual. ²The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}). ³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 4).

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Тур	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{ніGн}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and a START condi- tion	1.3			μs

¹For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32WG Reference Manual. ²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 4).



Symbol	Parameter	Min	Тур	Max	Unit
t _{SCLK_hi} ¹²	SCLK high period	3 * t _{HFPER-} CLK			ns
t _{SCLK_lo} 12	SCLK low period	3 * t _{HFPER-} CLK			ns
tcs_ACT_MI 12	CS active to MISO	5.00		35.00	ns
t _{CS_DIS_MI} ¹²	CS disable to MISO	5.00		35.00	ns
t _{SU_MO} ¹²	MOSI setup time	5.00			ns
t _{H_MO} 12	MOSI hold time	2 + 2 * t _{HF-} PERCLK			ns
t _{SCLK_MI} ¹²	SCLK to MISO	-264 + t _{HF-} PERCLK		-234 + 2 * t _{HFPERCLK}	ns

Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

 $^2\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $_{\text{VDD}})$

3.19 Digital Peripherals

Table 3.33. Digital Peripherals

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I _{USART}	USART current	USART idle current, clock en- abled		4.0		µA/ MHz
I _{UART}	UART current	UART idle current, clock en- abled		3.8		µA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock en- abled		194.0		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		7.6		µA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.5		µA/ MHz
I _{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		85.8		nA
I _{PCNT}	PCNT current	PCNT idle current, clock en- abled		91.4		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		54.6		nA
I _{LCD}	LCD current	LCD idle current, clock enabled		72.7		nA
I _{AES}	AES current	AES idle current, clock enabled		1.8		µA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock en- abled		3.4		µA/ MHz
I _{EBI}	EBI current	EBI idle current, clock enabled		6.5		µA/ MHz
I _{PRS}	PRS current	PRS idle current		3.9		μΑ/ MHz
I _{DMA}	DMA current	Clock enable		10.9		µA/ MHz



В	GA120 Pin# and Name	Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
A6	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
A7	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A8	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A9	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A10	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
A11	USB_VREGI	USB Input to internal 3.3	3 V regulator.	•		
A12	USB_VREGO	USB Decoupling for inte	rnal 3.3 V USB regulator ar	nd regulator output.		
A13	PF11				U1_RX #1	
B1	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
B6	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
B7	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B8	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B9	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B10	PF1			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
B11	PF12					
B12	USB_VBUS	USB 5.0 V VBUS input.				
B13	PF10				U1_TX #1	
C1	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
С3	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1
C5	VSS	Ground				
C6	IOVDD_0	Digital IO power supply	0.			
C7	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
C8	VSS	Ground				
C9	IOVDD_1	Digital IO power supply	1.			
C10	PF0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3

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Alternate			L	OCATIO	Ν			
Functionality	0	1	2	3	4	5	6	Description
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
								LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.
LCD_BEXT	PA14							An external LCD voltage may also be applied to this pin if the booster is not enabled.
								If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.



Figure 5.2. BGA120 PCB Solder Mask



 Table 5.2. BGA120 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
а	0.35
b	0.50
d	6.00
e	6.00



Figure 5.3. BGA120 PCB Stencil Design



 Table 5.3. BGA120 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
а	0.25
b	0.50
d	6.00
e	6.00

- 1. The drawings are not to scale.
- 2. All dimensions are in millimeters.
- 3. All drawings are subject to change without notice.
- 4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
- 5. Stencil thickness 0.125 mm.
- 6. For detailed pin-positioning, see Figure 4.3 (p. 71).

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.



List of Equations

3.1. Total ACMP Active Current	47
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