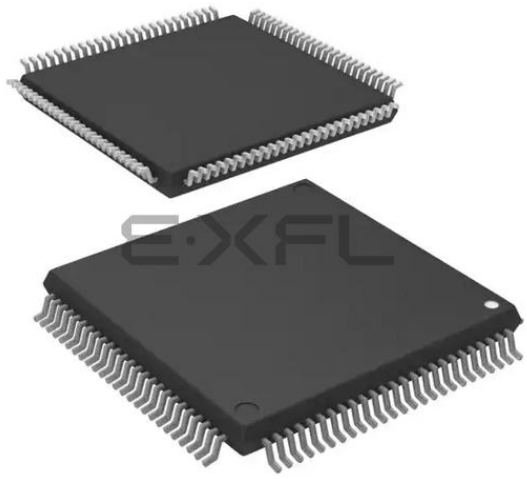

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64175dfb-ub

Table 1.2 Performance Overview for the 144-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I^2C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional (1)) (UART0 to UART6)
A/D Converter		10-bit resolution × 34 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 24 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional (1))
Multi-master I^2C-bus Interface		1 channel
CAN Module		1 channel CAN functionality compliant with ISO 11898-1 32 mailboxes
Flash Memory		Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		64 MHz (high speed version)/VCC = 3.0 to 5.5 V 50 MHz (normal speed version)/VCC = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version)
Current Consumption		45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 35 mA (VCC = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		144-pin plastic molded LQFP (PLQP0144KA-A)

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.6 R32C/117 Group Product List for High Speed Version (2/2) As of February, 2013

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F6417BHNFB (P)	PLQP0100KB-A	128 Kbytes + 8 Kbytes	20 Kbytes	-20°C to 85°C (N version)
R5F6417BHDFB				-40°C to 85°C (D version)
R5F6417BHPFB				-40°C to 85°C (P version)
R5F6417AHNFB (P)	PLQP0100KB-A	256 Kbytes + 8 Kbytes		-20°C to 85°C (N version)
R5F6417AHDFB				-40°C to 85°C (D version)
R5F6417AHPFB				-40°C to 85°C (P version)
R5F64175HNFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64175HDFD				-40°C to 85°C (D version)
R5F64175HPFD				-40°C to 85°C (P version)
R5F64175HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64175HDFB				-40°C to 85°C (D version)
R5F64175HPFB				-40°C to 85°C (P version)
R5F64176HNFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes		-20°C to 85°C (N version)
R5F64176HDFD				-40°C to 85°C (D version)
R5F64176HPFD				-40°C to 85°C (P version)
R5F64176HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64176HDFB				-40°C to 85°C (D version)
R5F64176HPFB				-40°C to 85°C (P version)
R5F64177HNFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64177HDFD				-40°C to 85°C (D version)
R5F64177HPFD				-40°C to 85°C (P version)
R5F64177HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64177HDFB				-40°C to 85°C (D version)
R5F64177HPFB				-40°C to 85°C (P version)
R5F64178HNFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64178HDFD				-40°C to 85°C (D version)
R5F64178HPFD				-40°C to 85°C (P version)
R5F64178HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64178HDFB				-40°C to 85°C (D version)
R5F64178HPFB				-40°C to 85°C (P version)
R5F64179HNFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes		-20°C to 85°C (N version)
R5F64179HDFD				-40°C to 85°C (D version)
R5F64179HPFD				-40°C to 85°C (P version)
R5F64179HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64179HDFB				-40°C to 85°C (D version)
R5F64179HPFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:
1. The old package codes are as follows:
   PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
2. “8 Kbytes” in the ROM capacity indicates the data flash memory capacity.

1.5 Pin Definitions and Functions

Tables 1.14 to 1.18 list the pin definitions and functions.

Table 1.14 Pin Definitions and Functions (1/4)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	
BCLK output	BCLK	O	BCLK output
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ (1)	I	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus
	D16 to D31 (2)	I/O	Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus
	A0 to A23	O	Output of address bits A0 to A23
	A0/D0 to A7/D7	I/O	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus

Notes:
1. Pins $\overline{\text{INT6}}$ to $\overline{\text{INT8}}$ are available in the 144-pin package only.
2. Pins D16 to D31 are available in the 144-pin package only.

3. Memory

Figure 3.1 shows the memory map of the R32C/117 Group.
The R32C/117 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

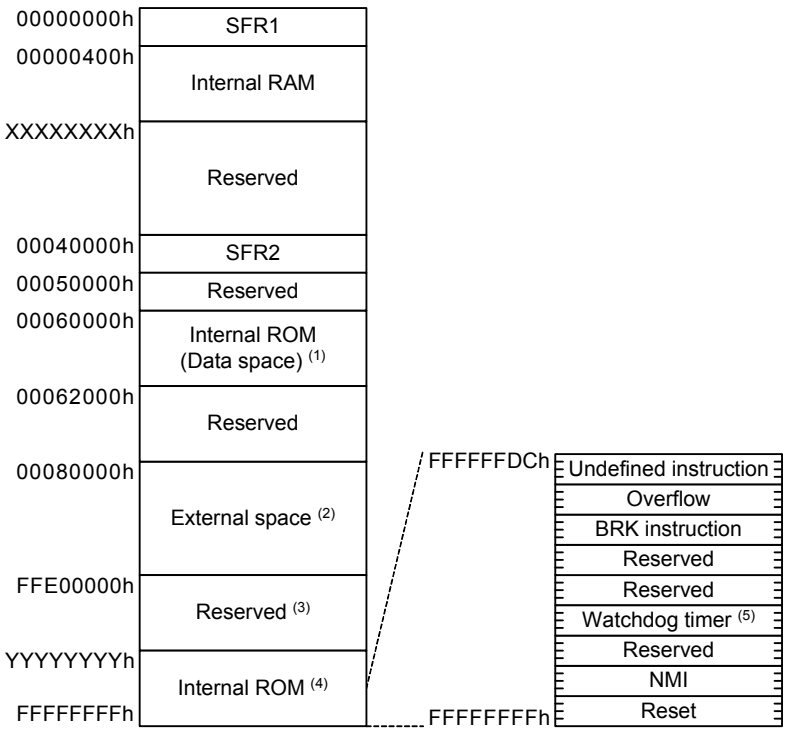
The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 1-Mbyte internal ROM is mapped from FFF00000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 63-Kbyte internal RAM is mapped from 00000400h to 0000FFFFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

In memory expansion mode or microprocessor mode, some spaces are reserved for internal use and should not be accessed.

Internal RAM	
Capacity	XXXXXXXXh
20 Kbytes	00005400h
40 Kbytes	0000A400h
48 Kbytes	0000C400h
63 Kbytes	00010000h

Internal ROM	
Capacity	YYYYYYYYh
128 Kbytes	FFFE0000h
256 Kbytes	FFFC0000h
384 Kbytes	FFFA0000h
512 Kbytes	FFF80000h
640 Kbytes	FFF60000h
768 Kbytes	FFF40000h
1 Mbyte	FFF00000h



Notes:
1. The flash memory version provides two additional 4-Kbyte spaces (blocks A and B) for storing data.
2. This space can be used in memory expansion mode or microprocessor mode. Addresses from 02000000h to FDFFFFFFh are inaccessible.
3. This space is reserved in memory expansion mode. It becomes an external space in microprocessor mode.
4. This space can be used in single-chip mode or memory expansion mode. It becomes an external space in microprocessor mode.
5. The watchdog timer interrupt shares a vector with the oscillator stop detection interrupt and low voltage detection interrupt.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.39 SFR List (39) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus Control Register 3	EBC3/FEBC3	0000h
000011h			
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus Control Register 0	EBC0/FEBC0	0000h
00001Dh			
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h	CAN0 Transmit Interrupt Control Register	C0TIC	XXXX X000b
0000C2h			
0000C3h	CAN0 Error Interrupt Control Register	C0EIC	XXXX X000b
0000C4h			
0000C5h			
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0000D1h			
0000D2h			
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h	UART5 Special Mode Register 4	U5SMR4	00h
0001C5h	UART5 Special Mode Register 3	U5SMR3	00h
0001C6h	UART5 Special Mode Register 2	U5SMR2	00h
0001C7h	UART5 Special Mode Register	U5SMR	00h
0001C8h	UART5 Transmit/Receive Mode Register	U5MR	00h
0001C9h	UART5 Bit Rate Register	U5BRG	XXh
0001CAh	UART5 Transmit Buffer Register	U5TB	XXXXh
0001CBh			
0001CCh	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
0001CDh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
0001CEh	UART5 Receive Buffer Register	U5RB	XXXXh
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX X0XXb
0003F2h	Pull-up Control Register 2	PUR2	000X XXXXb
0003F3h	Pull-up Control Register 3	PUR3	0000 0000b
0003F4h	Pull-up Control Register 4	PUR4	XXXX 0000b
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	0XXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0 (1)	PM0	1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High)
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h	Chip Select Output Pin Setting Register 0	CSOP0	1000 XXXXb
040055h	Chip Select Output Pin Setting Register 1	CSOP1	01X0 XXXXb
040056h	Chip Select Output Pin Setting Register 2	CSOP2	XXXX 0000b
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The value in the PM0 register is retained even after a software reset or watchdog timer reset.

Table 4.28 SFR List (28)

Address	Register	Symbol	Reset Value
047C60h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXXX XXXXh
047C61h			
047C62h			
047C63h			
047C64h			
047C65h	CAN0 Mailbox 6: Data Length		XXh
047C66h	CAN0 Mailbox 6: Data Field		XXXX XXXX
047C67h			XXXX XXXXh
047C68h			
047C69h			
047C6Ah			
047C6Bh			
047C6Ch			
047C6Dh			
047C6Eh	CAN0 Mailbox 6: Time Stamp		XXXXh
047C6Fh			
047C70h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXXX XXXXh
047C71h			
047C72h			
047C73h			
047C74h			
047C75h	CAN0 Mailbox 7: Data Length		XXh
047C76h	CAN0 Mailbox 7: Data Field		XXXX XXXX
047C77h			XXXX XXXXh
047C78h			
047C79h			
047C7Ah			
047C7Bh			
047C7Ch			
047C7Dh			
047C7Eh	CAN0 Mailbox 7: Time Stamp		XXXXh
047C7Fh			
047C80h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXXX XXXXh
047C81h			
047C82h			
047C83h			
047C84h			
047C85h	CAN0 Mailbox 8: Data Length		XXh
047C86h	CAN0 Mailbox 8: Data Field		XXXX XXXX
047C87h			XXXX XXXXh
047C88h			
047C89h			
047C8Ah			
047C8Bh			
047C8Ch			
047C8Dh			
047C8Eh	CAN0 Mailbox 8: Time Stamp		XXXXh
047C8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.29 SFR List (29)

Address	Register	Symbol	Reset Value
047C90h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXXX XXXXh
047C91h			
047C92h			
047C93h			
047C94h			
047C95h	CAN0 Mailbox 9: Data Length		XXh
047C96h	CAN0 Mailbox 9: Data Field		XXXX XXXX
047C97h			XXXX XXXXh
047C98h			
047C99h			
047C9Ah			
047C9Bh			
047C9Ch			
047C9Dh			
047C9Eh	CAN0 Mailbox 9: Time Stamp		XXXXh
047C9Fh			
047CA0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXXX XXXXh
047CA1h			
047CA2h			
047CA3h			
047CA4h			
047CA5h	CAN0 Mailbox 10: Data Length		XXh
047CA6h	CAN0 Mailbox 10: Data Field		XXXX XXXX
047CA7h			XXXX XXXXh
047CA8h			
047CA9h			
047CAAh			
047CABh			
047CACh			
047CADh			
047CAEh	CAN0 Mailbox 10: Time Stamp		XXXXh
047CAFh			
047CB0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXXX XXXXh
047CB1h			
047CB2h			
047CB3h			
047CB4h			
047CB5h	CAN0 Mailbox 11: Data Length		XXh
047CB6h	CAN0 Mailbox 11: Data Field		XXXX XXXX
047CB7h			XXXX XXXXh
047CB8h			
047CB9h			
047CBAh			
047CBBh			
047CBCh			
047CBDh			
047CBEh	CAN0 Mailbox 11: Time Stamp		XXXXh
047CBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

Address	Register	Symbol	Reset Value
047CF0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXXX XXXXh
047CF1h			
047CF2h			
047CF3h			
047CF4h			
047CF5h	CAN0 Mailbox 15: Data Length		XXh
047CF6h	CAN0 Mailbox 15: Data Field		XXXX XXXX
047CF7h			XXXX XXXXh
047CF8h			
047CF9h			
047CFAh			
047CFBh			
047CFCh			
047CFDh			
047CFEh	CAN0 Mailbox 15: Time Stamp		XXXXh
047CFFh			
047D00h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXXX XXXXh
047D01h			
047D02h			
047D03h			
047D04h			
047D05h	CAN0 Mailbox 16: Data Length		XXh
047D06h	CAN0 Mailbox 16: Data Field		XXXX XXXX
047D07h			XXXX XXXXh
047D08h			
047D09h			
047D0Ah			
047D0Bh			
047D0Ch			
047D0Dh			
047D0Eh	CAN0 Mailbox 16: Time Stamp		XXXXh
047D0Fh			
047D10h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXXX XXXXh
047D11h			
047D12h			
047D13h			
047D14h			
047D15h	CAN0 Mailbox 17: Data Length		XXh
047D16h	CAN0 Mailbox 17: Data Field		XXXX XXXX
047D17h			XXXX XXXXh
047D18h			
047D19h			
047D1Ah			
047D1Bh			
047D1Ch			
047D1Dh			
047D1Eh	CAN0 Mailbox 17: Time Stamp		XXXXh
047D1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.5 Operating Conditions (4/5)

(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency		4		16	MHz
$f_{(XRef)}$	Reference clock frequency		2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency		96		128	MHz
$f_{(Base)}$	Base clock frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(Base)}$	Base clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(CPU)}$	CPU operating frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(CPU)}$	CPU clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency	High speed version			32	MHz
		Normal speed version			25	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	High speed version	31.25			ns
		Normal speed version	40			ns
$f_{(PER)}$	Peripheral clock source frequency				32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency			32.768	62.5	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

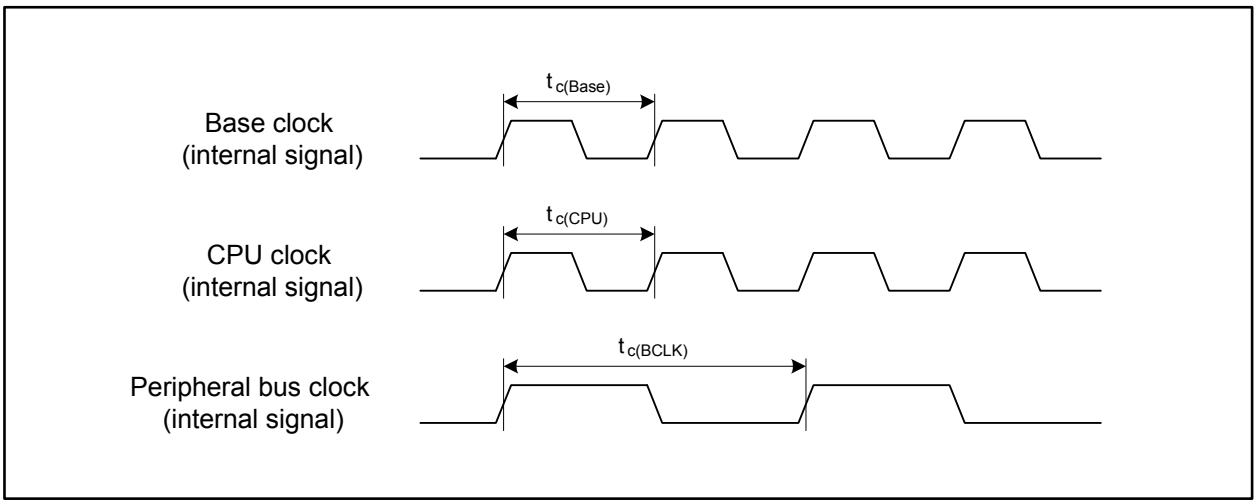


Figure 5.1 Clock Cycle Time

Table 5.6 Operating Conditions (5/5)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage gradient	V_{CC} = 5.0 V			±0.3	V/ms
		V_{CC} = 3.0 V			±0.3	V/ms
$f_{r(VCC)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

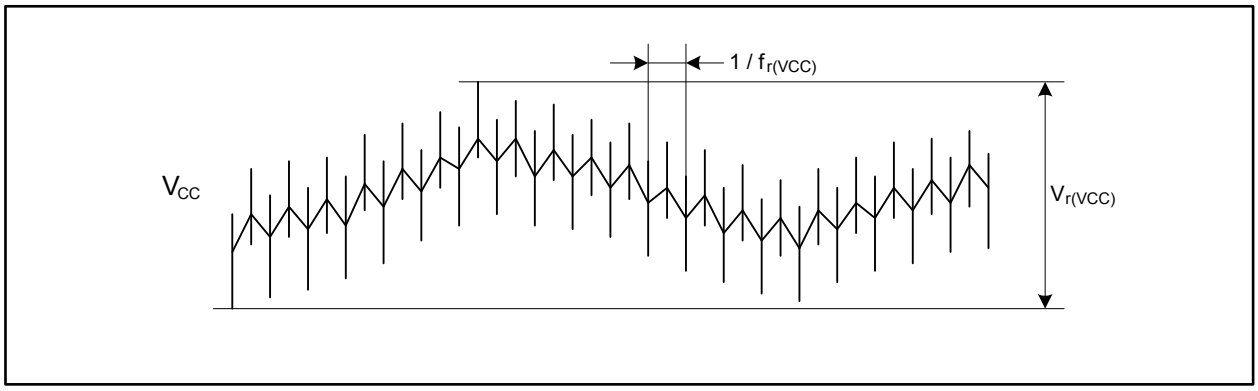


Figure 5.2 Ripple Waveform

V_{CC} = 5 V

Table 5.17 Electrical Characteristics (3/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive strength: low XCIN-XCOUT Drive strength: low	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		45	60	mA
			$f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		35	50	mA
			$f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		12		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		1.2		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		220		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		230		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		960	1600	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA

V_{CC} = 5 V

Table 5.18 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		16	MHz
		With sample and hold function		1		16	MHz

Note:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.60 Multi-master I^2C-bus Interface

Symbol	Characteristic	Value				Unit
		Standard-mode		Fast-mode		
		Min.	Max.	Min.	Max.	
$t_{w(SCLH)}$	MSCL input high level pulse width	600		600		ns
$t_{w(SCLL)}$	MSCL input low level pulse width	600		600		ns
$t_{r(SCL)}$	MSCL input rise time		1000		300	ns
$t_{f(SCL)}$	MSCL input fall time		300		300	ns
$t_{r(SDA)}$	MSDA input rise time		1000		300	ns
$t_{f(SDA)}$	MSDA input fall time		300		300	ns
$t_{h(SDA-SCL)S}$	MSCL high level hold time after START condition/repeated START condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SCL-SDA)P}$	MSCL high level setup time for repeated START condition/STOP condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{w(SDAH)P}$	MSDA high level pulse width after STOP condition	(1)		4 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SDA-SCL)}$	MSDA input setup time	100		100		ns
$t_{h(SCL-SDA)}$	MSDA input hold time	0		0		ns

Note:

1. The value is calculated using the formulas below based on a value SSC set by bits SSC4 to SSC0 in the I2CSSCR register:

   $t_{h(SDA-SCL)S}$ = SSC ÷ 2 × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{su(SCL-SDA)P}$ = (SSC ÷ 2 + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{w(SDAH)P}$ = (SSC + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

V_{CC} = 3.3 V

Switching Characteristics (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.61 External Bus Timing (separate bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-R)}$	Chip-select setup time before read	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$t_{c(Base)}$ - 15		ns
$t_{su(A-R)}$	Address setup time before read		(1)		ns
$t_{h(R-A)}$	Address hold time after read		$t_{c(Base)}$ - 15		ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{su(S-W)}$	Chip-select setup time before write		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 15		ns
$t_{su(A-W)}$	Address setup time before write		(1)		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 15		ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-R)} = t_{su(A-R)}$ = Tsu(A-R) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ - 10 [ns]

   $t_{su(S-W)} = t_{su(A-W)}$ = Tsu(A-W) × $t_{c(Base)}$ - 15 [ns]

   $t_{w(W)} = t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ - 10 [ns]

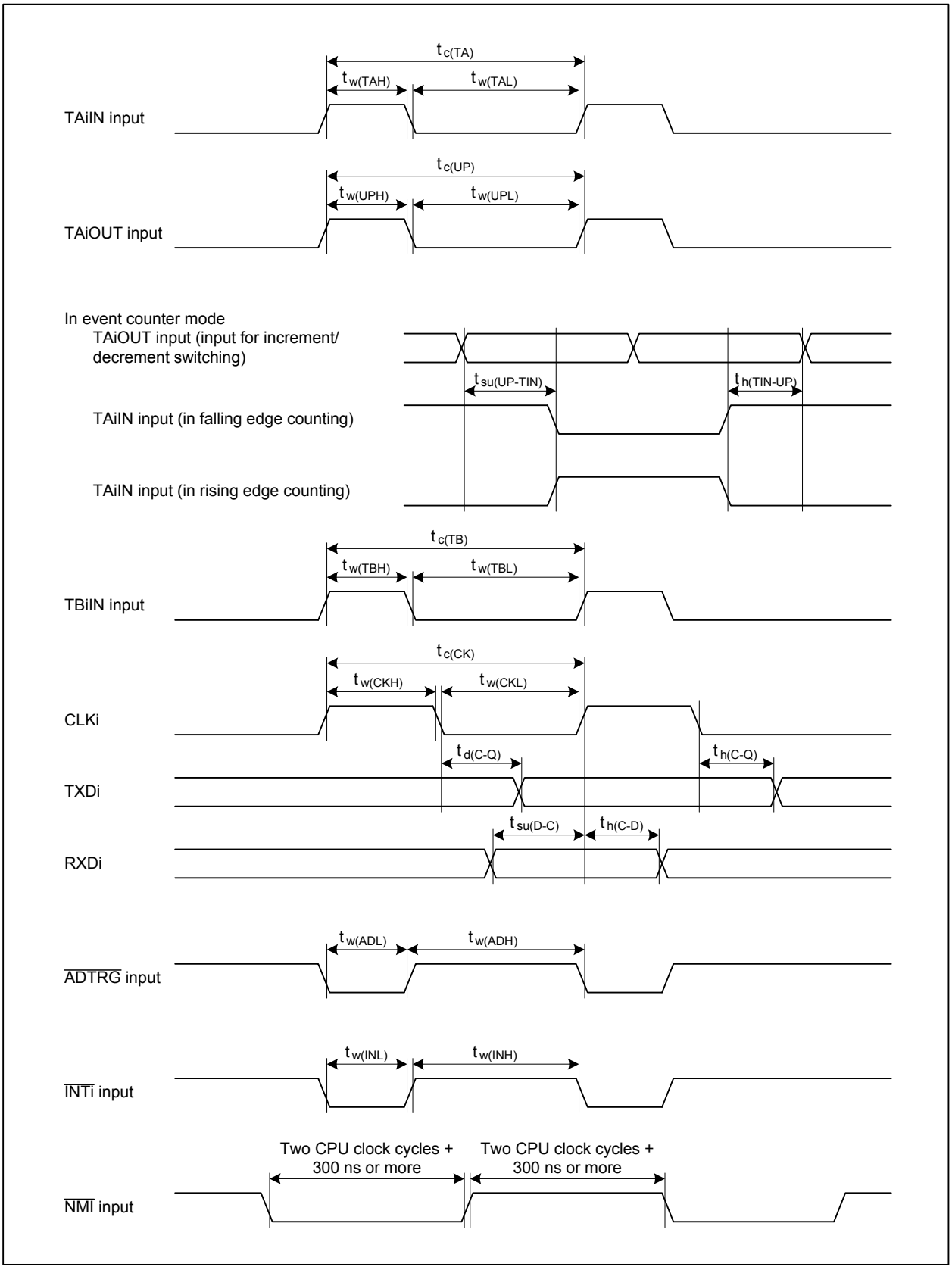


Figure 5.10 Timing of Peripherals

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