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Details

Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	120
Program Memory Size	640KB (640K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64177dfd-ub

Table 1.6 R32C/117 Group Product List for High Speed Version (2/2) As of February, 2013

Part Number	Package Code ⁽¹⁾	ROM Capacity ⁽²⁾	RAM Capacity	Remarks
R5F6417BHNFB (P)	PLQP0100KB-A	128 Kbytes + 8 Kbytes	20 Kbytes	-20°C to 85°C (N version)
R5F6417BHDFB				-40°C to 85°C (D version)
R5F6417BHPFB				-40°C to 85°C (P version)
R5F6417AHNFB (P)	PLQP0100KB-A	256 Kbytes + 8 Kbytes		-20°C to 85°C (N version)
R5F6417AHDFB				-40°C to 85°C (D version)
R5F6417AHPFB				-40°C to 85°C (P version)
R5F64175HNFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64175HDFD				-40°C to 85°C (D version)
R5F64175HPFD				-40°C to 85°C (P version)
R5F64175HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64175HDFB				-40°C to 85°C (D version)
R5F64175HPFB				-40°C to 85°C (P version)
R5F64176HNFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes		-20°C to 85°C (N version)
R5F64176HDFD				-40°C to 85°C (D version)
R5F64176HPFD				-40°C to 85°C (P version)
R5F64176HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64176HDFB				-40°C to 85°C (D version)
R5F64176HPFB				-40°C to 85°C (P version)
R5F64177HNFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64177HDFD				-40°C to 85°C (D version)
R5F64177HPFD				-40°C to 85°C (P version)
R5F64177HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64177HDFB				-40°C to 85°C (D version)
R5F64177HPFB				-40°C to 85°C (P version)
R5F64178HNFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64178HDFD				-40°C to 85°C (D version)
R5F64178HPFD				-40°C to 85°C (P version)
R5F64178HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64178HDFB				-40°C to 85°C (D version)
R5F64178HPFB				-40°C to 85°C (P version)
R5F64179HNFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes		-20°C to 85°C (N version)
R5F64179HDFD				-40°C to 85°C (D version)
R5F64179HPFD				-40°C to 85°C (P version)
R5F64179HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64179HDFB				-40°C to 85°C (D version)
R5F64179HPFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:

- The old package codes are as follows:
PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
- "8 Kbytes" in the ROM capacity indicates the data flash memory capacity.

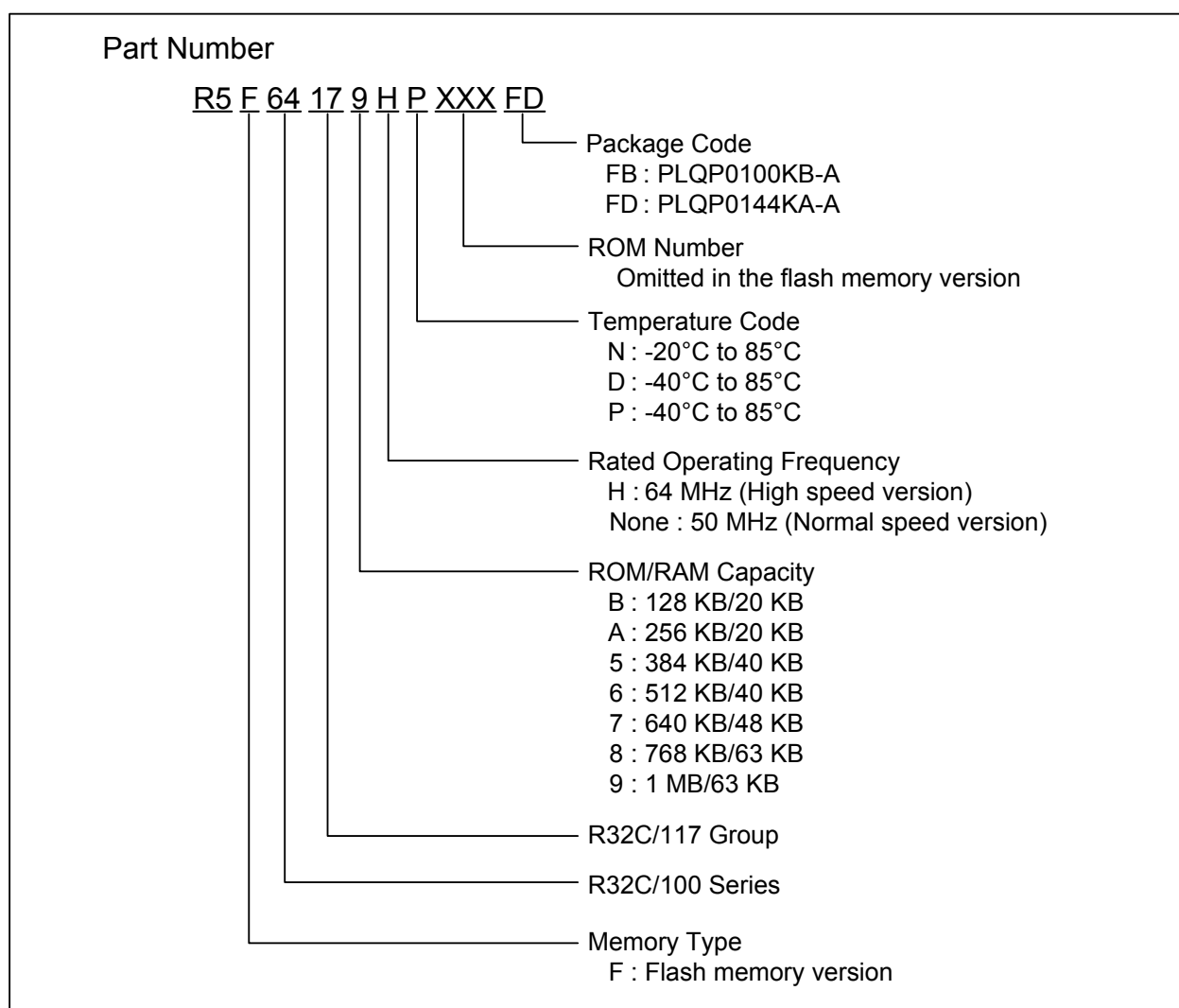


Figure 1.1 Part Numbering

Table 1.11 Pin Characteristics for the 100-pin Package (1/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2		P9_3		TB3IN			DA0	
3	VDC0							
4		P9_1						
5	VDC1							
6	NSD							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	RESET							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	NMI					
16		P8_4	INT2					
17		P8_3	INT1		CAN0IN/CAN0WU			
18		P8_2	INT0		CAN0OUT			
19		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21		P7_7		TA3IN	CLK5/CAN0IN/ CAN0WU	IIO1_4/UD0B/UD1B		
22		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT	IIO1_3/UD0A/UD1A		
23		P7_5		TA2IN/W	RXD8	IIO1_2		
24		P7_4		TA2OUT/W	CLK8	IIO1_1		
25		P7_3		TA1IN/V	CTS2/RTS2/SS2/TXD8	IIO1_0		
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2/ MSCL	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28		P7_0		TA0OUT	TXD2/SDA2/SRXD2/ MSDA	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29		P6_7			TXD1/SDA1/SRXD1			
30		P6_6			RXD1/SCL1/STXD1			
31		P6_5			CLK1			
32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33		P6_3			TXD0/SDA0/SRXD0			
34		P6_2		TB2IN	RXD0/SCL0/STXD0			
35		P6_1		TB1IN	CLK0			
36		P6_0		TB0IN	CTS0/RTS0/SS0			
37		P5_7			CTS7/RTS7			RDY/CS3
38		P5_6			RXD7			ALE/CS2

Table 1.16 Pin Definitions and Functions (3/4)

Function	Symbol	I/O	Description
I/O port (1, 2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Some ports are 5 V tolerant inputs. Pull-up resistors and N-channel open drain setting can be enabled on some ports. Refer to Table 1.18 "Pin Specifications" for details
Input port (2)	P9_1 (for 100-pin package) P14_1 (for 144-pin package)	I	Input port in CMOS Pull-up resistor is selectable. Refer to Table 1.18 "Pin Specifications" for details
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	Timers B0 to B5 input
Three-phase motor control timer output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Three-phase motor control timer output
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS8}}$	I	Handshake input
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS8}}$	O	Handshake output
	CLK0 to CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD8	I	Serial data input
	TXD0 to TXD8	O	Serial data output
I ² C-bus (simplified)	SDA0 to SDA6	I/O	Serial data input/output
	SCL0 to SCL6	I/O	Transmit/receive clock input/output
Serial interface special functions	STXD0 to STXD6	O	Serial data output in slave mode
	SRXD0 to SRXD6	I	Serial data input in slave mode
	$\overline{\text{SS0}}$ to $\overline{\text{SS6}}$	I	Input to control serial interface special functions

Notes:

1. Port P9_1 in the 100-pin package is an input-only port.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only.

Table 1.17 Pin Definitions and Functions (4/4)

Function	Symbol	I/O	Description
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 (1)	I	Analog input for the A/D converter
	ADTRG	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_7 (2)	O	Output for OC (output compare) of Intelligent I/O group 2
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface
Multi-master I ² C-bus	MSDA	I/O	Serial data input/output
	MSCL	I/O	Transmit/receive clock input/output
CAN Module	CAN0IN	I	Receive data input for the CAN communications
	CAN0OUT	O	Transmit data output for the CAN communications
	CAN0WU	I	Input for the CAN wake-up interrupt

Notes:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.
2. Pins OUTC2_3 to OUTC2_7 are available in the 144-pin package only.

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.39 SFR List (39) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus	EBC3/FEBC3	0000h
000011h	Control Register 3		
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus	EBC0/FEBC0	0000h
00001Dh	Control Register 0		
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register/I ² C-bus Line Interrupt Control Register	S2RIC/I2CLIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register/I ² C-bus Interrupt Control Register	S2TIC/I2CIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1/4 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h			
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh			
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh			
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh			
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 XXX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X 0XX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	000X 0XX1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	000X 0XX1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	X00X 0XX1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	XX0X 0XX1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0X00 0XX1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0X00 0XX1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0X00 0XX1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000140h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
000141h			
000142h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
000143h			
000144h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
000145h			
000146h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
000147h			
000148h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
000149h			
00014Ah	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
00014Bh			
00014Ch	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
00014Dh			
00014Eh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh
00014Fh			
000150h	Group 2 Waveform Generation Control Register 0	G2POCR0	0000 0000b
000151h	Group 2 Waveform Generation Control Register 1	G2POCR1	0000 0000b
000152h	Group 2 Waveform Generation Control Register 2	G2POCR2	0000 0000b
000153h	Group 2 Waveform Generation Control Register 3	G2POCR3	0000 0000b
000154h	Group 2 Waveform Generation Control Register 4	G2POCR4	0000 0000b
000155h	Group 2 Waveform Generation Control Register 5	G2POCR5	0000 0000b
000156h	Group 2 Waveform Generation Control Register 6	G2POCR6	0000 0000b
000157h	Group 2 Waveform Generation Control Register 7	G2POCR7	0000 0000b
000158h			
000159h			
00015Ah			
00015Bh			
00015Ch			
00015Dh			
00015Eh			
00015Fh			
000160h	Group 2 Base Timer Register	G2BT	XXXXh
000161h			
000162h	Group 2 Base Timer Control Register 0	G2BCR0	0000 0000b
000163h	Group 2 Base Timer Control Register 1	G2BCR1	0000 0000b
000164h	Base Timer Start Register	BTSR	XXXX 0000b
000165h			
000166h	Group 2 Function Enable Register	G2FE	00h
000167h	Group 2 RTP Output Buffer Register	G2RTP	00h
000168h			
000169h			
00016Ah	Group 2 Serial Interface Mode Register	G2MR	00XX X000b
00016Bh	Group 2 Serial Interface Control Register	G2CR	0000 X110b
00016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
00016Dh			
00016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
00016Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XXXXb
040098h	Input Function Select Register 0	IFS0	X000 0000b
040099h	Input Function Select Register 1	IFS1	XXXX X0X0b
04009Ah	Input Function Select Register 2	IFS2	0000 00X0b
04009Bh	Input Function Select Register 3	IFS3	XXXX XX00b
04009Ch			
04009Dh			
04009Eh			
04009Fh			
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.28 SFR List (28)

Address	Register	Symbol	Reset Value
047C60h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXXX XXXXh
047C61h			
047C62h			
047C63h			
047C64h			
047C65h	CAN0 Mailbox 6: Data Length		XXh
047C66h	CAN0 Mailbox 6: Data Field		XXXX XXXX XXXX XXXXh
047C67h			
047C68h			
047C69h			
047C6Ah			
047C6Bh			
047C6Ch			
047C6Dh			
047C6Eh	CAN0 Mailbox 6: Time Stamp		XXXXh
047C6Fh			
047C70h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXXX XXXXh
047C71h			
047C72h			
047C73h			
047C74h			
047C75h	CAN0 Mailbox 7: Data Length		XXh
047C76h	CAN0 Mailbox 7: Data Field		XXXX XXXX XXXX XXXXh
047C77h			
047C78h			
047C79h			
047C7Ah			
047C7Bh			
047C7Ch			
047C7Dh			
047C7Eh	CAN0 Mailbox 7: Time Stamp		XXXXh
047C7Fh			
047C80h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXXX XXXXh
047C81h			
047C82h			
047C83h			
047C84h			
047C85h	CAN0 Mailbox 8: Data Length		XXh
047C86h	CAN0 Mailbox 8: Data Field		XXXX XXXX XXXX XXXXh
047C87h			
047C88h			
047C89h			
047C8Ah			
047C8Bh			
047C8Ch			
047C8Dh			
047C8Eh	CAN0 Mailbox 8: Time Stamp		XXXXh
047C8Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

Address	Register	Symbol	Reset Value
047D80h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXXX XXXXh
047D81h			
047D82h			
047D83h			
047D84h			
047D85h	CAN0 Mailbox 24: Data Length		XXh
047D86h	CAN0 Mailbox 24: Data Field		XXXX XXXX XXXX XXXXh
047D87h			
047D88h			
047D89h			
047D8Ah			
047D8Bh			
047D8Ch			
047D8Dh			
047D8Eh	CAN0 Mailbox 24: Time Stamp		XXXXh
047D8Fh			
047D90h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXXX XXXXh
047D91h			
047D92h			
047D93h			
047D94h			
047D95h	CAN0 Mailbox 25: Data Length		XXh
047D96h	CAN0 Mailbox 25: Data Field		XXXX XXXX XXXX XXXXh
047D97h			
047D98h			
047D99h			
047D9Ah			
047D9Bh			
047D9Ch			
047D9Dh			
047D9Eh	CAN0 Mailbox 25: Time Stamp		XXXXh
047D9Fh			
047DA0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXXX XXXXh
047DA1h			
047DA2h			
047DA3h			
047DA4h			
047DA5h	CAN0 Mailbox 26: Data Length		XXh
047DA6h	CAN0 Mailbox 26: Data Field		XXXX XXXX XXXX XXXXh
047DA7h			
047DA8h			
047DA9h			
047DAAh			
047DABh			
047DACH			
047DADh			
047DAEh	CAN0 Mailbox 26: Time Stamp		XXXXh
047DAFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.37 SFR List (37)

Address	Register	Symbol	Reset Value
047E10h	CAN0 Mask Register 4	C0MKR4	XXXX XXXXh
047E11h			
047E12h			
047E13h			
047E14h	CAN0 Mask Register 5	C0MKR5	XXXX XXXXh
047E15h			
047E16h			
047E17h			
047E18h	CAN0 Mask Register 6	C0MKR6	XXXX XXXXh
047E19h			
047E1Ah			
047E1Bh			
047E1Ch	CAN0 Mask Register 7	C0MKR7	XXXX XXXXh
047E1Dh			
047E1Eh			
047E1Fh			
047E20h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXXX XXXXh
047E21h			
047E22h			
047E23h			
047E24h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXXX XXXXh
047E25h			
047E26h			
047E27h			
047E28h	CAN0 Mask Invalid Register	C0MKIVLR	XXXX XXXXh
047E29h			
047E2Ah			
047E2Bh			
047E2Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXXX XXXXh
047E2Dh			
047E2Eh			
047E2Fh			
047E30h			
047E31h			
047E32h			
047E33h			
047E34h			
047E35h			
047E36h			
047E37h			
047E38h			
047E39h			
047E3Ah			
047E3Bh			
047E3Ch			
047E3Dh			
047E3Eh			
047E3Fh			
047E40h to 047F1Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.6 Operating Conditions (5/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) ⁽¹⁾

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	$V_{CC} = 5.0$ V		0.5	Vp-p
		$V_{CC} = 3.0$ V		0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage gradient	$V_{CC} = 5.0$ V		± 0.3	V/ms
		$V_{CC} = 3.0$ V		± 0.3	V/ms
$f_{r(VCC)}$	Allowable ripple frequency			10	kHz

Note:

1. The device is operationally guaranteed under these operating conditions.

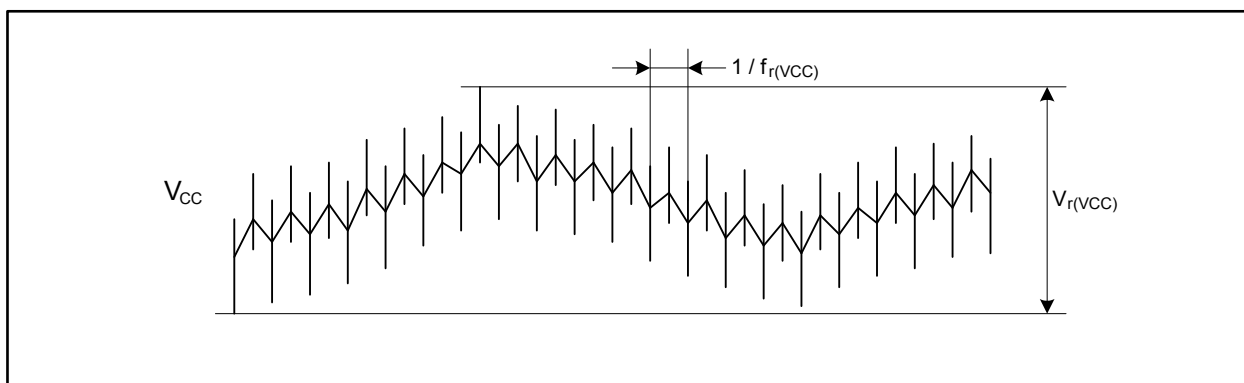


Figure 5.2 Ripple Waveform

$$V_{CC} = 5\text{ V}$$

Table 5.18 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2\text{ to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32\text{ MHz}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute error	$V_{REF} = V_{CC} = 5\text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC} = 5\text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
DNL	Differential non-linearity error				± 1	LSB
—	Offset error				± 3	LSB
—	Gain error				± 3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC}$	4		20	k Ω
t_{CONV}	Conversion time (10 bits)	$\phi_{AD} = 16\text{ MHz}$, with sample and hold function	2.06			μs
		$\phi_{AD} = 16\text{ MHz}$, without sample and hold function	3.69			μs
t_{CONV}	Conversion time (8 bits)	$\phi_{AD} = 16\text{ MHz}$, with sample and hold function	1.75			μs
		$\phi_{AD} = 16\text{ MHz}$, without sample and hold function	3.06			μs
t_{SAMP}	Sampling time	$\phi_{AD} = 16\text{ MHz}$	0.188			μs
V_{IA}	Analog input voltage		0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function	0.25		16	MHz
		With sample and hold function	1		16	MHz

Note:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.46 External Clock Input

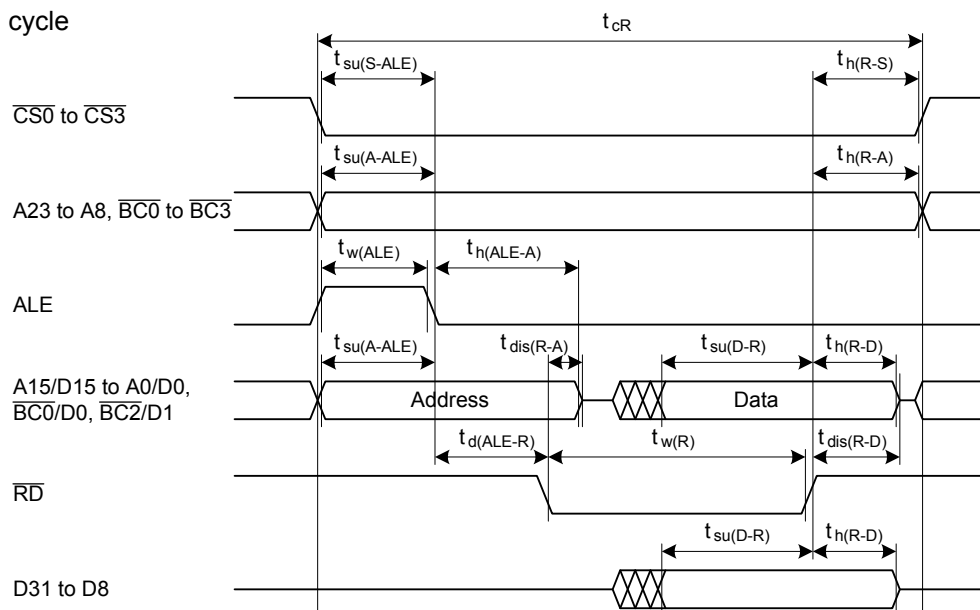
Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	62.5	250	ns
$t_{W(XH)}$	External clock input high level pulse width	25		ns
$t_{W(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

Table 5.47 External Bus Timing

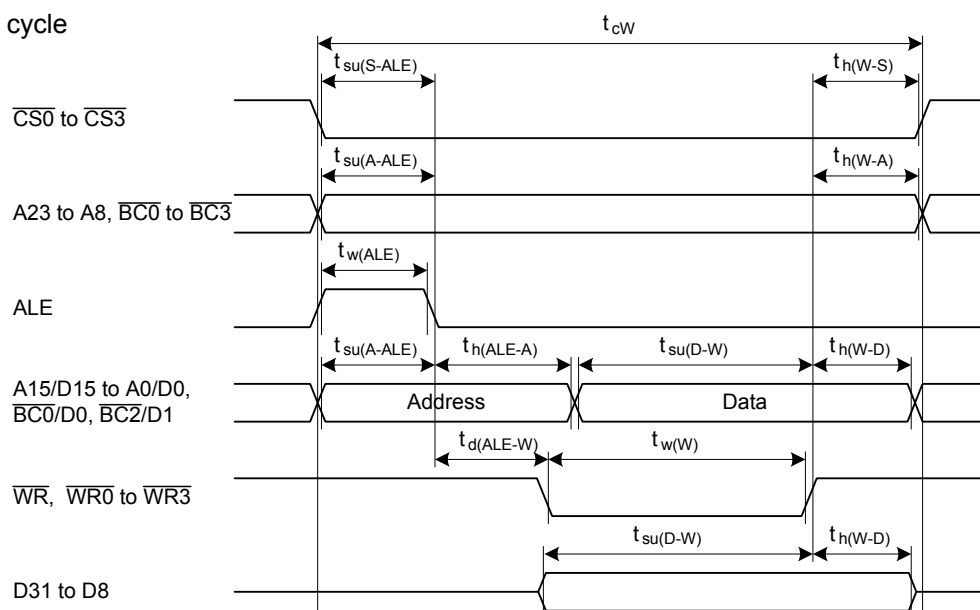
Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{C(Base)} + 10$	ns

External bus timing (multiplexed bus)

Read cycle



Write cycle



Measurement conditions

Item		$V_{CC} = 4.2$ to 5.5 V	$V_{CC} = 3.0$ to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.9 External Bus Timing for Multiplexed Bus

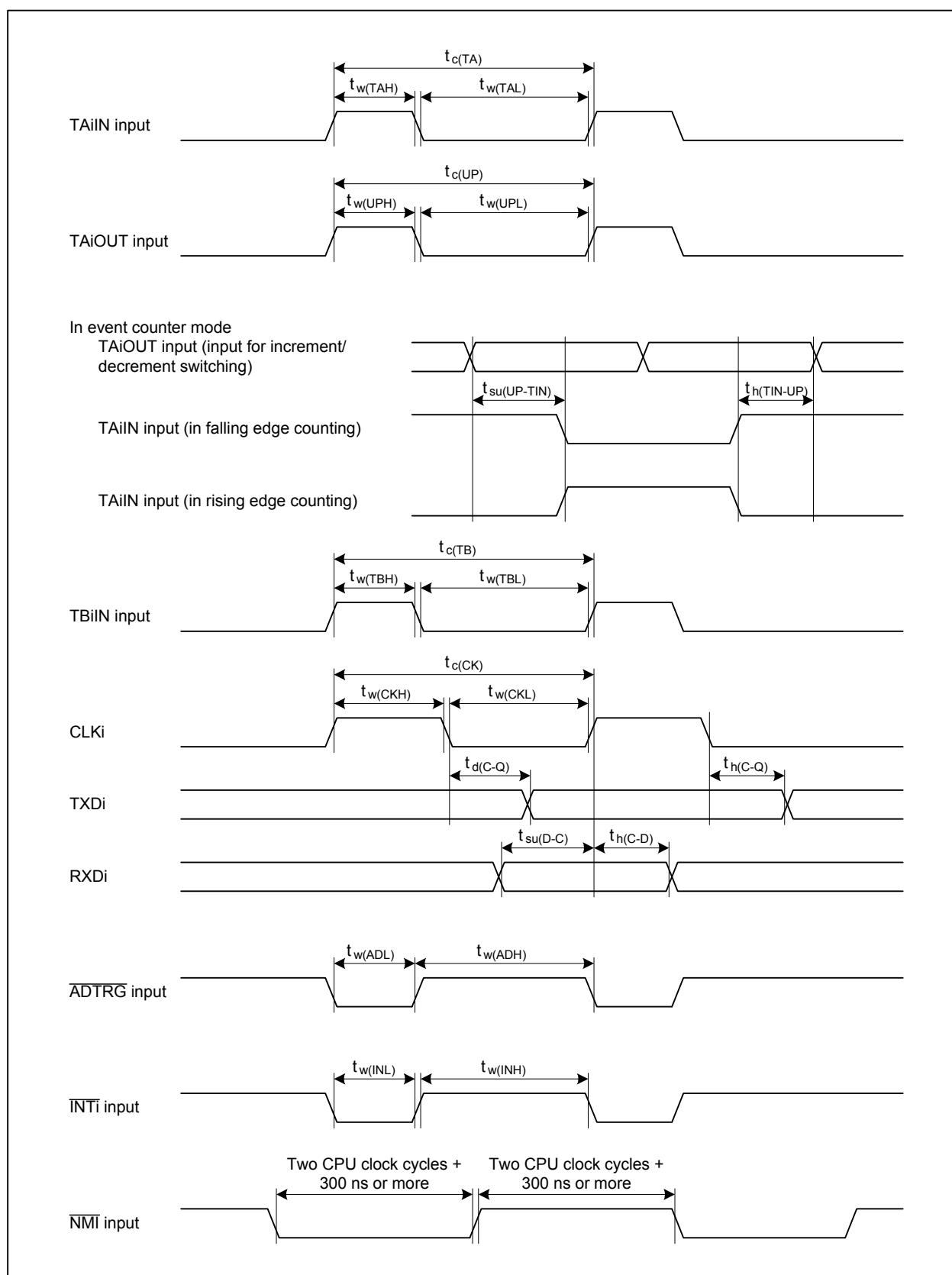
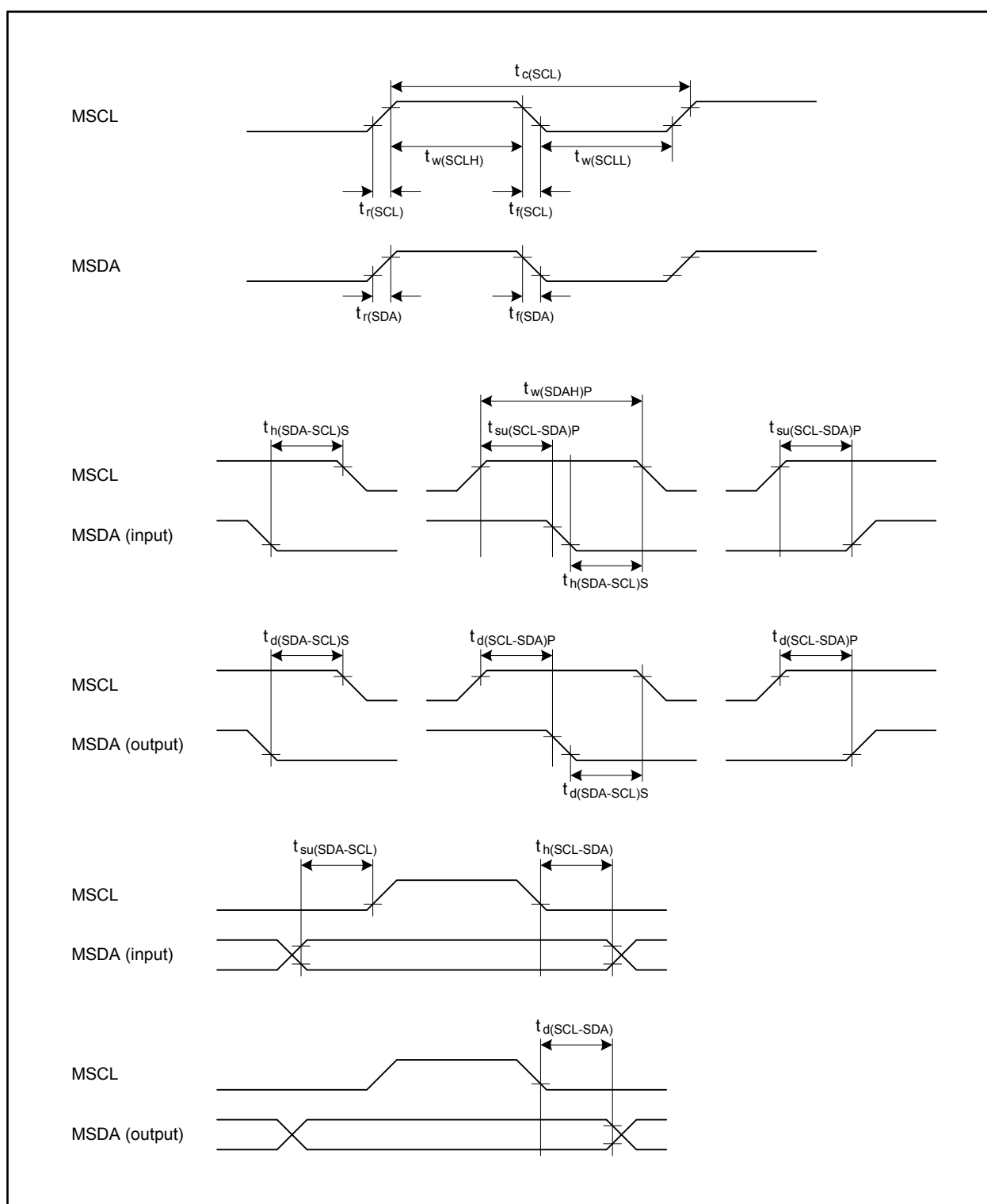


Figure 5.10 Timing of Peripherals

Figure 5.11 Timing of Multi-master I²C-bus Interface

Revision History	R32C/117 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
		87, 90, 100, 103	• Changed expression “restart condition” in Tables 5.34, 5.39, 5.40, 5.60, 5.65, and 5.66 to “repeated START condition”

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