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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	120
Program Memory Size	640KB (640K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64177pfd-ub

Table 1.2 Performance Overview for the 144-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I^2C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional (1)) (UART0 to UART6)
A/D Converter		10-bit resolution × 34 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 24 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional (1))
Multi-master I^2C-bus Interface		1 channel
CAN Module		1 channel CAN functionality compliant with ISO 11898-1 32 mailboxes
Flash Memory		Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		64 MHz (high speed version)/VCC = 3.0 to 5.5 V 50 MHz (normal speed version)/VCC = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version)
Current Consumption		45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 35 mA (VCC = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		144-pin plastic molded LQFP (PLQP0144KA-A)

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

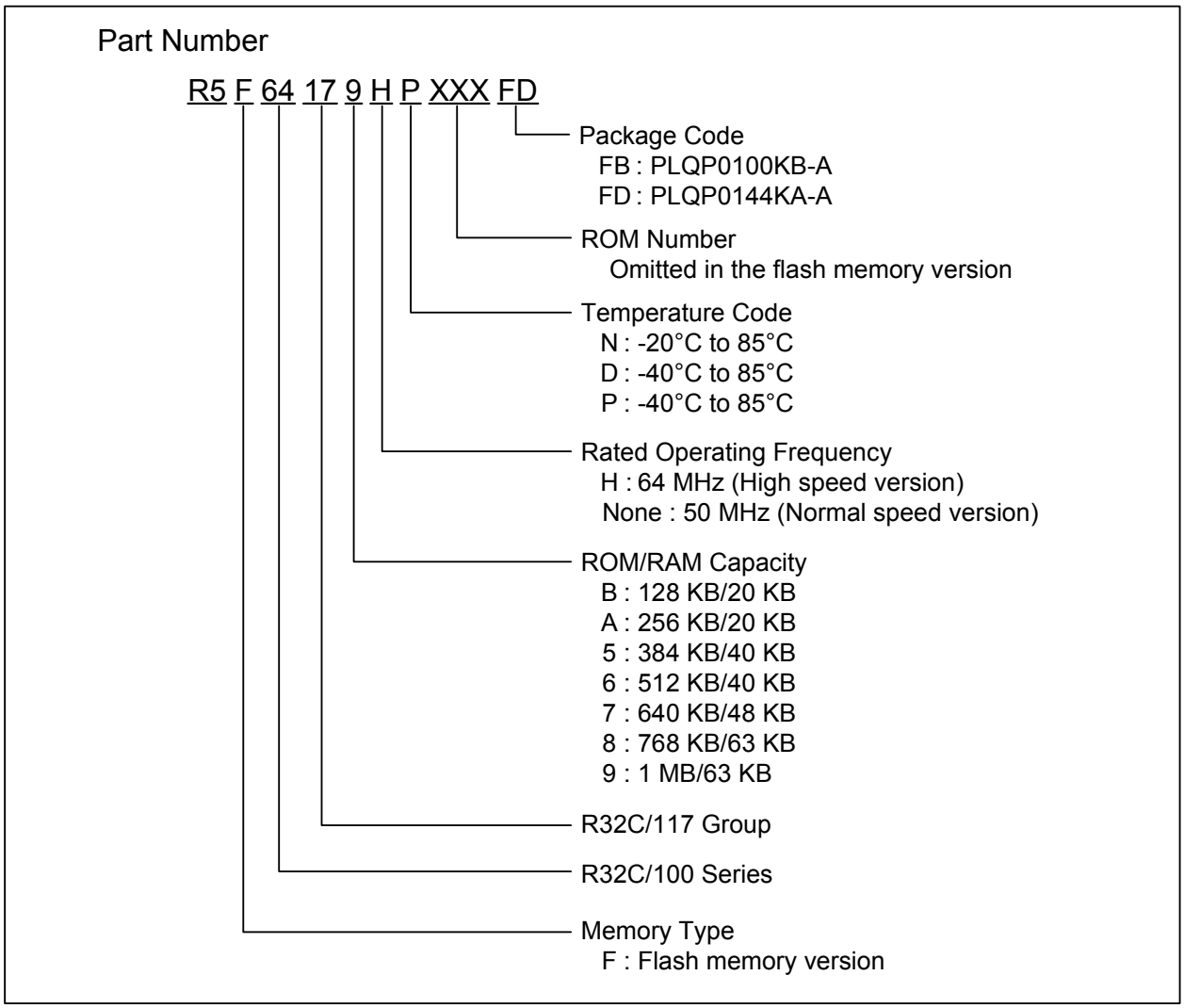


Figure 1.1 Part Numbering

Table 1.7 Pin Characteristics for the 144-pin Package (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4		ANEX1	
2		P9_5			CLK4		ANEX0	
3		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	ISRXD2/IEIN		
7		P9_0		TB0IN	CLK3			
8		P14_6	INT8					
9		P14_5	INT7					
10		P14_4	INT6					
11		P14_3						
12	VDC0							
13		P14_1						
14	VDC1							
15	NSD							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	RESET							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P8_5	NMI					
25		P8_4	INT2					
26		P8_3	INT1		CAN0IN/CAN0WU			
27		P8_2	INT0		CAN0OUT			
28		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
29		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
30		P7_7		TA3IN	CLK5/CAN0IN/ CAN0WU	IIO1_4/UD0B/UD1B		
31		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT	IIO1_3/UD0A/UD1A		
32		P7_5		TA2IN/W	RXD8	IIO1_2		
33		P7_4		TA2OUT/W	CLK8	IIO1_1		
34		P7_3		TA1IN/V	CTS2/RTS2/SS2/TXD8	IIO1_0		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2/ MSCL	IIO1_7/OUTC2_2/ ISRXD2/IEIN		

Table 1.9 Pin Characteristics for the 144-pin Package (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
75		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
76	VSS							
77		P4_1			CLK3			A17
78		P4_0			$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$			A16
79		P3_7		TA4IN/$\overline{\text{U}}$				A15(/D15)
80		P3_6		TA4OUT/U				A14(/D14)
81		P3_5		TA2IN/$\overline{\text{W}}$				A13(/D13)
82		P3_4		TA2OUT/W				A12(/D12)
83		P3_3		TA1IN/$\overline{\text{V}}$				A11(/D11)
84		P3_2		TA1OUT/V				A10(/D10)
85		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
86		P12_4						D20
87		P12_3			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$			D19
88		P12_2			RXD6/SCL6/STXD6			D18
89		P12_1			CLK6			D17
90		P12_0			TXD6/SDA6/SRXD6			D16
91	VCC							
92		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
93	VSS							
94		P2_7					AN2_7	A7(/D7)
95		P2_6					AN2_6	A6(/D6)
96		P2_5					AN2_5	A5(/D5)
97		P2_4					AN2_4	A4(/D4)
98		P2_3					AN2_3	A3(/D3)
99		P2_2					AN2_2	A2(/D2)
100		P2_1					AN2_1	A1(/D1)/ $\overline{\text{BC2}}$(/D1)
101		P2_0					AN2_0	A0(/D0)/ $\overline{\text{BC0}}$(/D0)
102		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7		D15
103		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6		D14
104		P1_5	$\overline{\text{INT3}}$			IIO0_5/IIO1_5		D13
105		P1_4				IIO0_4/IIO1_4		D12
106		P1_3				IIO0_3/IIO1_3		D11
107		P1_2				IIO0_2/IIO1_2		D10
108		P1_1				IIO0_1/IIO1_1		D9
109		P1_0				IIO0_0/IIO1_0		D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						$\overline{\text{BC3}}$/$\overline{\text{WR3}}$

Table 1.15 Pin Definitions and Functions (2/4)

Function	Symbol	I/O	Description
Bus control pins	$\overline{BC0}$/D0, $\overline{BC2}$/D1 (1)	I/O	Output of byte control ($\overline{BC0}$ and $\overline{BC2}$) and input/output of data (D0 and D1) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	Chip select output
	$\overline{WR0}$/$\overline{WR1}$/$\overline{WR2}$/$\overline{WR3}$, $\overline{WR}$/$\overline{BC0}$/$\overline{BC1}$/$\overline{BC2}$/$\overline{BC3}$, $\overline{RD}$ (1)	O	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. • When $\overline{WR0}$, $\overline{WR1}$, $\overline{WR2}$, $\overline{WR3}$, and $\overline{RD}$ are selected, data is written to the following address: 4n+0, when $\overline{WR0}$ is low 4n+1, when $\overline{WR1}$ is low 4n+2, when $\overline{WR2}$ is low 4n+3, when $\overline{WR3}$ is low on 32-bit external data bus or an even address, when $\overline{WR0}$ is low an odd address, when $\overline{WR1}$ is low on 16-bit external data bus • When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, $\overline{BC2}$, $\overline{BC3}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: 4n+0, when $\overline{BC0}$ is low 4n+1, when $\overline{BC1}$ is low 4n+2, when $\overline{BC2}$ is low 4n+3, when $\overline{BC3}$ is low on 32-bit external data bus or an even address, when $\overline{BC0}$ is low an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

Note:
1. Pins $\overline{BC2}$/D1, $\overline{WR2}$, $\overline{WR3}$, $\overline{BC2}$, and $\overline{BC3}$ are available in the 144-pin package only.

Table 1.17 Pin Definitions and Functions (4/4)

Function	Symbol	I/O	Description
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 (1)	I	Analog input for the A/D converter
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for Intelligent I/O group 1. Either input capture or output compare is selectable
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
	OUTC2_0 to OUTC2_7 (2)	O	Output for OC (output compare) of Intelligent I/O group 2
	ISCLK2	I/O	Clock input/output for the serial interface
	ISRXD2	I	Receive data input for the serial interface
	ISTXD2	O	Transmit data output for the serial interface
	IEIN	I	Receive data input for the serial interface
	IEOUT	O	Transmit data output for the serial interface
Multi-master I^2C-bus	MSDA	I/O	Serial data input/output
	MSCL	I/O	Transmit/receive clock input/output
CAN Module	CAN0IN	I	Receive data input for the CAN communications
	CAN0OUT	O	Transmit data output for the CAN communications
	$\overline{\text{CAN0WU}}$	I	Input for the CAN wake-up interrupt

Notes:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.
2. Pins OUTC2_3 to OUTC2_7 are available in the 144-pin package only.

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.
Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R1 can be divided into R3 and R1, etc.
Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).
Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 “Flag Register (FLG)” for details.
To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag retains a carry, borrow, or shifted-out bit generated by the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt occurs.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt occurs.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt occurs.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1/4 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h			
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh			
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh			
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh			
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 XXX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X 0XX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	000X 0XX1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	000X 0XX1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	X00X 0XX1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	XX0X 0XX1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0X00 0XX1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0X00 0XX1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0X00 0XX1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0 (1)	PM0	1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High)
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h	Chip Select Output Pin Setting Register 0	CSOP0	1000 XXXXb
040055h	Chip Select Output Pin Setting Register 1	CSOP1	01X0 XXXXb
040056h	Chip Select Output Pin Setting Register 2	CSOP2	XXXX 0000b
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The value in the PM0 register is retained even after a software reset or watchdog timer reset.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
047D20h	CAN0 Mailbox 18: Message Identifier	C0MB18	XXXX XXXXh
047D21h			
047D22h			
047D23h			
047D24h			
047D25h	CAN0 Mailbox 18: Data Length		XXh
047D26h	CAN0 Mailbox 18: Data Field		XXXX XXXX
047D27h			XXXX XXXXh
047D28h			
047D29h			
047D2Ah			
047D2Bh			
047D2Ch			
047D2Dh			
047D2Eh	CAN0 Mailbox 18: Time Stamp		XXXXh
047D2Fh			
047D30h	CAN0 Mailbox 19: Message Identifier	C0MB19	XXXX XXXXh
047D31h			
047D32h			
047D33h			
047D34h			
047D35h	CAN0 Mailbox 19: Data Length		XXh
047D36h	CAN0 Mailbox 19: Data Field		XXXX XXXX
047D37h			XXXX XXXXh
047D38h			
047D39h			
047D3Ah			
047D3Bh			
047D3Ch			
047D3Dh			
047D3Eh	CAN0 Mailbox 19: Time Stamp		XXXXh
047D3Fh			
047D40h	CAN0 Mailbox 20: Message Identifier	C0MB20	XXXX XXXXh
047D41h			
047D42h			
047D43h			
047D44h			
047D45h	CAN0 Mailbox 20: Data Length		XXh
047D46h	CAN0 Mailbox 20: Data Field		XXXX XXXX
047D47h			XXXX XXXXh
047D48h			
047D49h			
047D4Ah			
047D4Bh			
047D4Ch			
047D4Dh			
047D4Eh	CAN0 Mailbox 20: Time Stamp		XXXXh
047D4Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.35 SFR List (35)

Address	Register	Symbol	Reset Value
047DB0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXXX XXXXh
047DB1h			
047DB2h			
047DB3h			
047DB4h			
047DB5h	CAN0 Mailbox 27: Data Length		XXh
047DB6h	CAN0 Mailbox 27: Data Field		XXXX XXXX
047DB7h			XXXX XXXXh
047DB8h			
047DB9h			
047DBAh			
047DBBh			
047DBCh			
047DBDh			
047DBEh	CAN0 Mailbox 27: Time Stamp		XXXXh
047DBFh			
047DC0h	CAN0 Mailbox 28: Message Identifier	C0MB28	XXXX XXXXh
047DC1h			
047DC2h			
047DC3h			
047DC4h			
047DC5h	CAN0 Mailbox 28: Data Length		XXh
047DC6h	CAN0 Mailbox 28: Data Field		XXXX XXXX
047DC7h			XXXX XXXXh
047DC8h			
047DC9h			
047DCAh			
047DCBh			
047DCCh			
047DCDh			
047DCEh	CAN0 Mailbox 28: Time Stamp		XXXXh
047DCFh			
047DD0h	CAN0 Mailbox 29: Message Identifier	C0MB29	XXXX XXXXh
047DD1h			
047DD2h			
047DD3h			
047DD4h			
047DD5h	CAN0 Mailbox 29: Data Length		XXh
047DD6h	CAN0 Mailbox 29: Data Field		XXXX XXXX
047DD7h			XXXX XXXXh
047DD8h			
047DD9h			
047DDAh			
047DDBh			
047DDCh			
047DDDh			
047DDEh	CAN0 Mailbox 29: Time Stamp		XXXXh
047DDFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.5 Operating Conditions (4/5)

(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency		4		16	MHz
$f_{(XRef)}$	Reference clock frequency		2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency		96		128	MHz
$f_{(Base)}$	Base clock frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(Base)}$	Base clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(CPU)}$	CPU operating frequency	High speed version			64	MHz
		Normal speed version			50	MHz
$t_{c(CPU)}$	CPU clock cycle time	High speed version	15.625			ns
		Normal speed version	20			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency	High speed version			32	MHz
		Normal speed version			25	MHz
$t_{c(BCLK)}$	Peripheral bus clock cycle time	High speed version	31.25			ns
		Normal speed version	40			ns
$f_{(PER)}$	Peripheral clock source frequency				32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency			32.768	62.5	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

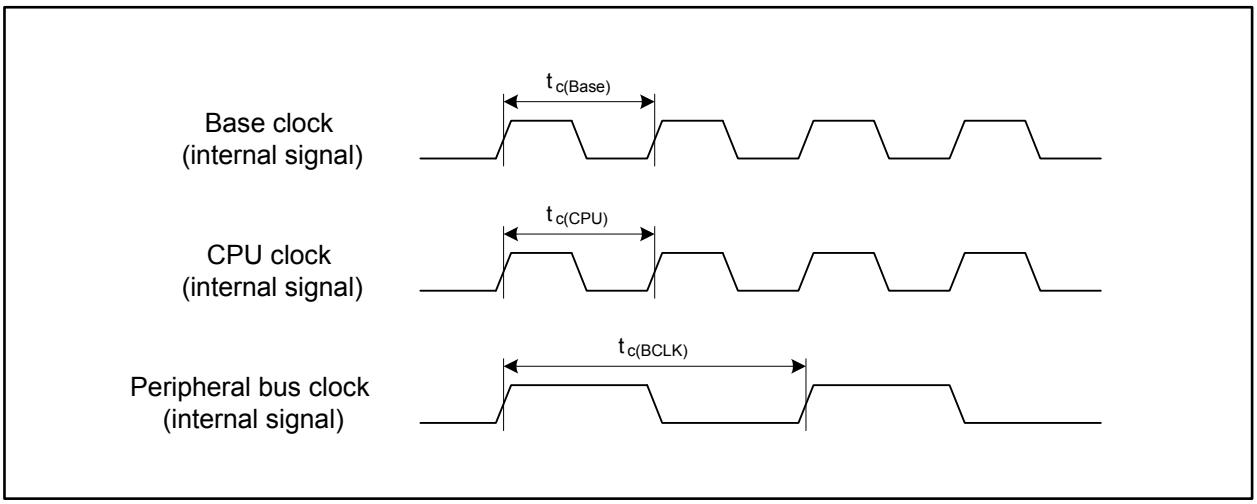


Figure 5.1 Clock Cycle Time

V_{CC} = 5 V

Table 5.16 Electrical Characteristics (2/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $\overline{NMI}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{KI0}$ to $\overline{KI3}$, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{CTS0}$ to $\overline{CTS8}$, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, $\overline{SS0}$ to $\overline{SS6}$, SRXD0 to SRXD6, $\overline{ADTRG}$, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, MSCL, MSDA, CAN0IN, $\overline{CAN0WU}$ (1)		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	High level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V_I = 5 V			5.0	µA
I_{IL}	Low level input current	XIN, $\overline{RESET}$, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V_I = 0 V			-5.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Notes:
1. Pins $\overline{INT6}$ to $\overline{INT8}$ are available in the 144-pin package only.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

V_{CC} = 5 V

Switching Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.37 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.38 Intelligent I/O

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

Table 5.39 Multi-master I²C-bus Interface (standard-mode)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2		ns
$t_{f(SDA)}$	MSDA output fall time		2		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$20 \times t_{c(\phi IIC)} - 120$	$52 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$20 \times t_{c(\phi IIC)} + 40$	$52 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

Table 5.40 Multi-master I²C-bus Interface (fast-mode)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2 (1)		ns
$t_{f(SDA)}$	MSDA output fall time		2 (1)		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$10 \times t_{c(\phi IIC)} - 120$	$26 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$10 \times t_{c(\phi IIC)} + 40$	$26 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

Note:

1. External circuits are required to satisfy the I²C-bus specification.

V_{CC} = 3.3 V

Table 5.41 Electrical Characteristics (1/3) (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I_{OH} = -1 mA	V_{CC} - 0.6		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I_{OL} = 1 mA			0.5	V

Note:
1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

V_{CC} = 3.3 V

Switching Characteristics (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.63 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.64 Intelligent I/O

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

Table 5.65 Multi-master I²C-bus Interface (Standard-mode)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2		ns
$t_{f(SDA)}$	MSDA output fall time		2		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$20 \times t_{c(\phi IIC)} - 120$	$52 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$20 \times t_{c(\phi IIC)} + 40$	$52 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

Table 5.66 Multi-master I²C-bus Interface (Fast-mode)

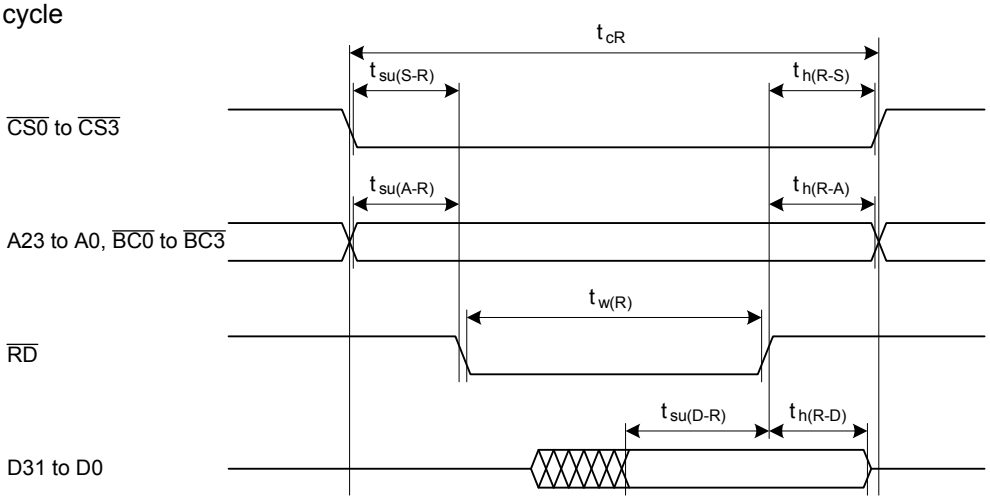
Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2 (1)		ns
$t_{f(SDA)}$	MSDA output fall time		2 (1)		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$10 \times t_{c(\phi IIC)} - 120$	$26 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$10 \times t_{c(\phi IIC)} + 40$	$26 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

Note:

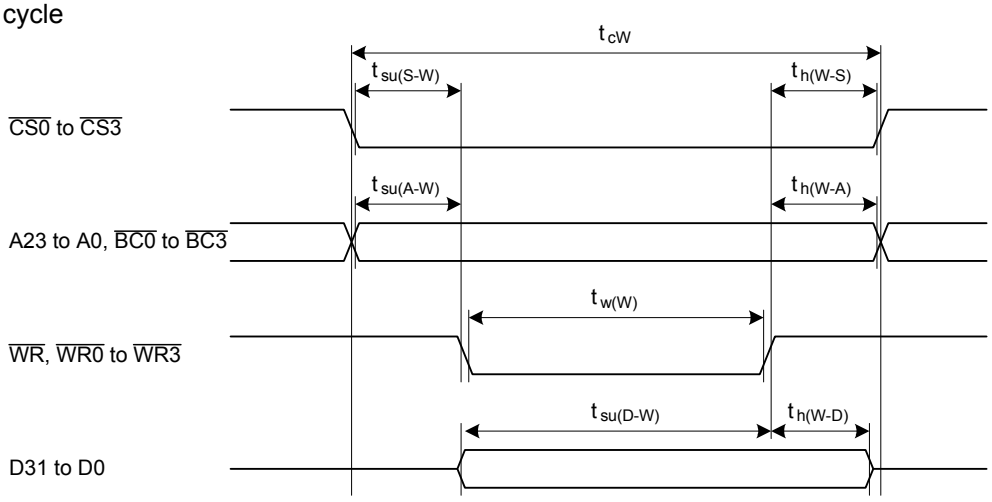
1. External circuits are required to satisfy the I²C-bus specification.

External bus timing (separate bus)

Read cycle



Write cycle



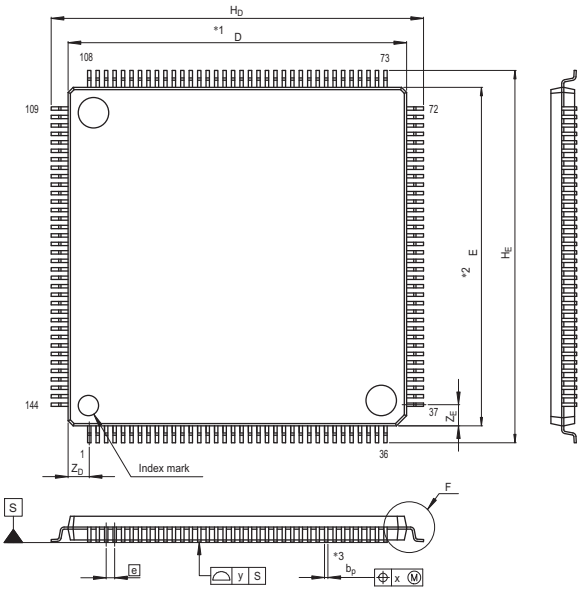
Measurement conditions

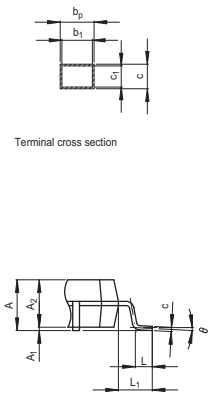
Item		V_{CC} = 4.2 to 5.5 V	V_{CC} = 3.0 to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.8 External Bus Timing for Separate Bus

Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g

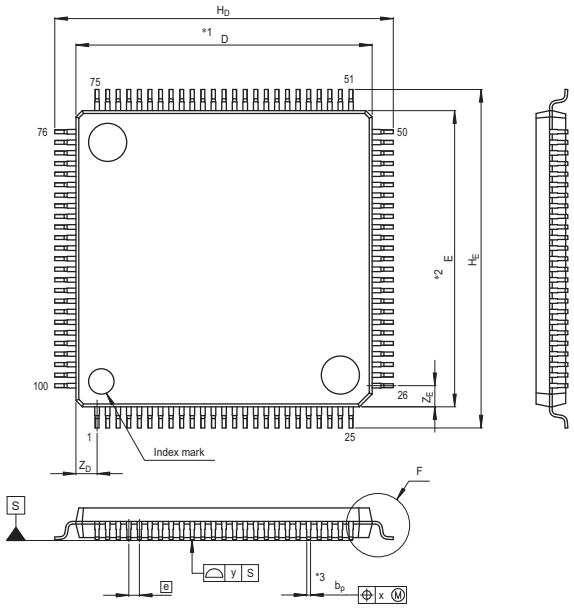


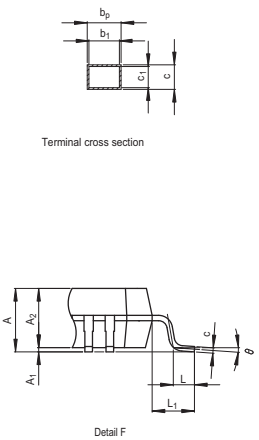


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

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