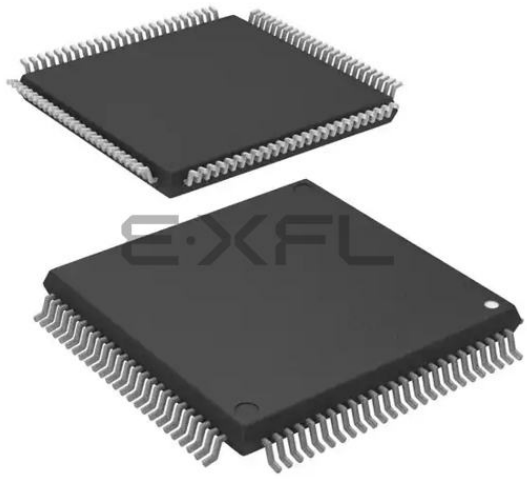

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

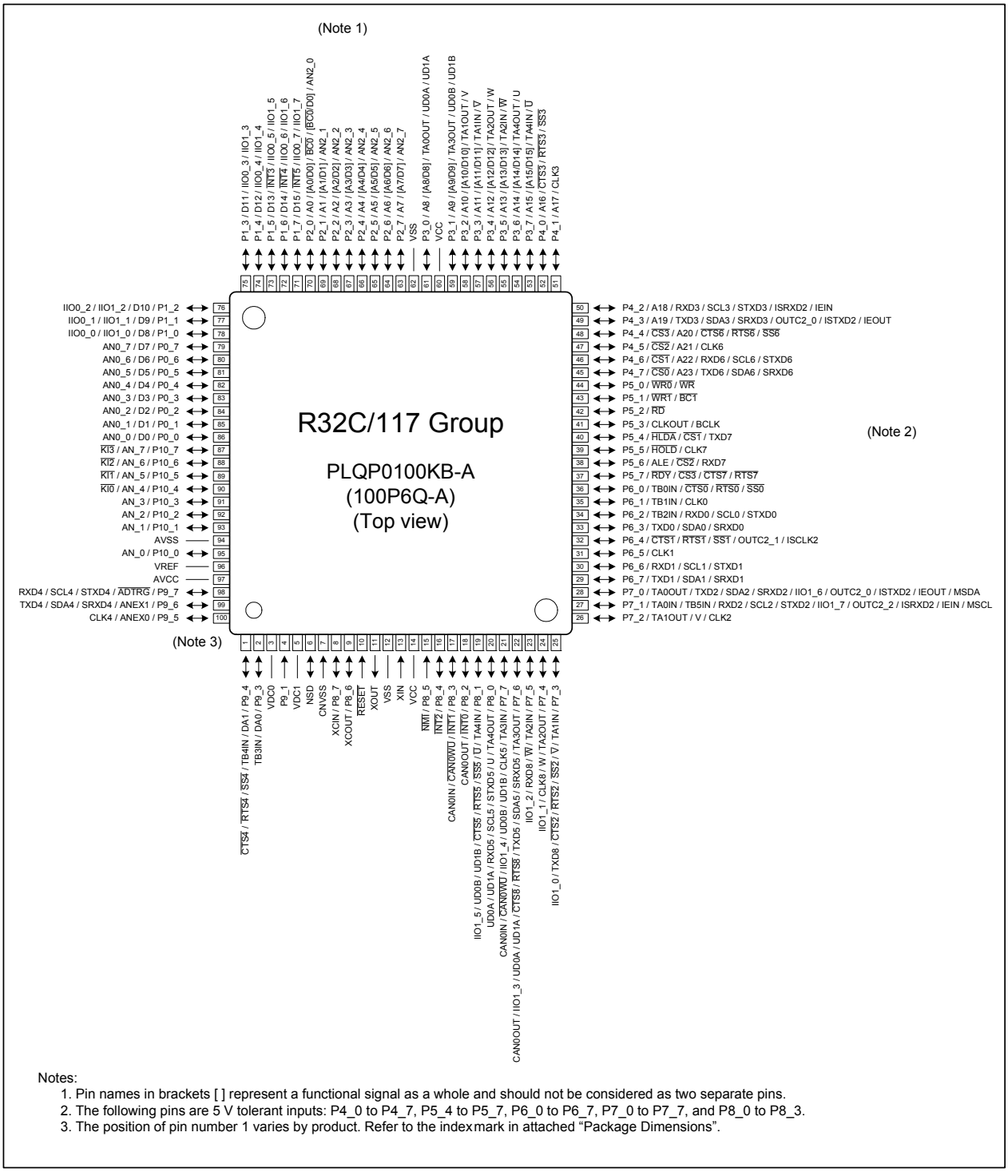
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | R32C/100 |
| Core Size | 16/32-Bit |
| Speed | 50MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IEBus, UART/USART |
| Peripherals | DMA, LVD, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 63K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64179dfb-ub |

**Table 1.4 Performance Overview for the 100-pin Package (2/2)**

| Unit | Function | Explanation |
|---|---|---|
| Timer | Timer A | 16-bit timer × 5<br>Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode<br>Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 |
| | Timer B | 16-bit timer × 6<br>Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode |
| | Three-phase motor control timer | Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used)<br>8-bit programmable dead time timer |
| Serial Interface | UART0 to UART8 | Asynchronous/synchronous serial interface × 9 channels<br>• $I^2C$-bus (UART0 to UART6)<br>• Special mode 2 (UART0 to UART6)<br>• IEBus (optional (1)) (UART0 to UART6) |
| A/D Converter | | 10-bit resolution × 26 channels<br>Sample and hold functionality integrated |
| D/A Converter | | 8-bit resolution × 2 |
| CRC Calculator | | CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) |
| X-Y Converter | | 16 bits × 16 bits |
| Intelligent I/O | | Time measurement (input capture): 16 bits × 16<br>Waveform generation (output compare): 16 bits × 19<br>Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional (1)) |
| Multi-master $I^2C$-bus Interface | | 1 channel |
| CAN Module | | 1 channel<br>CAN functionality compliant with ISO 11898-1<br>32 mailboxes |
| Flash Memory | | Programming and erasure supply voltage: VCC = 3.0 to 5.5 V<br>Minimum endurance: 1,000 program/erase cycles<br>Security protection: ROM code protect, ID code protect<br>Debugging: On-chip debug, on-board flash programming |
| Operating Frequency/Supply Voltage | | 64 MHz (high speed version)/VCC = 3.0 to 5.5 V<br>50 MHz (normal speed version)/VCC = 3.0 to 5.5 V |
| Operating Temperature | | -20°C to 85°C (N version)<br>-40°C to 85°C (D version)<br>-40°C to 85°C (P version) |
| Current Consumption | | 45 mA (VCC = 5.0 V, f(CPU) = 64 MHz)<br>35 mA (VCC = 5.0 V, f(CPU) = 50 MHz)<br>8 µA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode) |
| Package | | 100-pin plastic molded LQFP (PLQP0100KB-A) |

Note:
1. Contact a Renesas Electronics sales office to use the optional features.




Notes:
1. Pin names in brackets [ ] represent a functional signal as a whole and should not be considered as two separate pins.
2. The following pins are 5 V tolerant inputs: P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, and P8_0 to P8_3.
3. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

**Figure 1.4 Pin Assignment for the 100-pin Package (top view)**

**Table 1.18 Pin Specifications**

| Pin Names | Package | | Selectable Functions | | 5 V Tolerant Input (3) |
|---|---|---|---|---|---|
| | 144-pin | 100-pin | Pull-up resistor (1) | N-channel open drain (2) | |
| P0_0 to P0_7 | ✓ | ✓ | ✓ | | |
| P1_0 to P1_7 | ✓ | ✓ | ✓ | | |
| P2_0 to P2_7 | ✓ | ✓ | ✓ | | |
| P3_0 to P3_7 | ✓ | ✓ | ✓ | | |
| P4_0 to P4_7 | ✓ | ✓ | | ✓ | ✓ |
| P5_0 to P5_3 | ✓ | ✓ | ✓ | | |
| P5_4 to P5_7 | ✓ | ✓ | | ✓ | ✓ |
| P6_0 to P6_7 | ✓ | ✓ | | ✓ | ✓ |
| P7_0 to P7_7 | ✓ | ✓ | | ✓ | ✓ |
| P8_0 to P8_3 | ✓ | ✓ | | ✓ | ✓ |
| P8_4, P8_6, P8_7 | ✓ | ✓ | ✓ | | |
| P9_0 to P9_3 (144-pin) | ✓ | | ✓ | ✓ | |
| P9_1, P9_3 (100-pin) | | ✓ | ✓ | | |
| P9_4 to P9_7 | ✓ | ✓ | ✓ | ✓ | |
| P10_0 to P10_7 | ✓ | ✓ | ✓ | | |
| P11_0 to P11_3 | ✓ | | ✓ | ✓ | |
| P11_4 | ✓ | | ✓ | | |
| P12_0 to P12_3 | ✓ | | ✓ | ✓ | |
| P12_4 to P12_7 | ✓ | | ✓ | | |
| P13_0 to P13_7 | ✓ | | ✓ | | |
| P14_1, P14_3 | ✓ | | ✓ | | |
| P14_4 to P14_6 | ✓ | | ✓ | | |
| P15_0 to P15_7 | ✓ | | ✓ | ✓ | |

Notes:
1. Pull-up resistors are selected for the following 4-pin units: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 15); however, they are enabled only for the input pins.
2. N-channel open drain output can be enabled on the applicable pins on a discrete pin basis.
3. 5 V tolerant input is enabled when an applicable pin is set as an input port. When it is set as an I/O port, to enable 5 V tolerant input, this pin should be set as N-channel open drain output.

#### 2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

#### 2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

#### 2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

#### 2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

#### 2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

#### 2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

#### 2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

#### 2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

#### 2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

#### 2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

**Table 4.8 SFR List (8)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 000170h | Group 2 IEBus Address Register | IEAR | XXXXh |
| 000171h | | | |
| 000172h | Group 2 IEBus Control Register | IECR | 00XX X000b |
| 000173h | Group 2 IEBus Transmit Interrupt Source Detect Register | IETIF | XXX0 0000b |
| 000174h | Group 2 IEBus Receive Interrupt Source Detect Register | IERIF | XXX0 0000b |
| 000175h | | | |
| 000176h | | | |
| 000177h | | | |
| 000178h | | | |
| 000179h | | | |
| 00017Ah | | | |
| 00017Bh | | | |
| 00017Ch | | | |
| 00017Dh | | | |
| 00017Eh | | | |
| 00017Fh | | | |
| 000180h | Group 0 Time Measurement/Waveform Generation Register 0 | G0TM0/G0PO0 | XXXXh |
| 000181h | | | |
| 000182h | Group 0 Time Measurement/Waveform Generation Register 1 | G0TM1/G0PO1 | XXXXh |
| 000183h | | | |
| 000184h | Group 0 Time Measurement/Waveform Generation Register 2 | G0TM2/G0PO2 | XXXXh |
| 000185h | | | |
| 000186h | Group 0 Time Measurement/Waveform Generation Register 3 | G0TM3/G0PO3 | XXXXh |
| 000187h | | | |
| 000188h | Group 0 Time Measurement/Waveform Generation Register 4 | G0TM4/G0PO4 | XXXXh |
| 000189h | | | |
| 00018Ah | Group 0 Time Measurement/Waveform Generation Register 5 | G0TM5/G0PO5 | XXXXh |
| 00018Bh | | | |
| 00018Ch | Group 0 Time Measurement/Waveform Generation Register 6 | G0TM6/G0PO6 | XXXXh |
| 00018Dh | | | |
| 00018Eh | Group 0 Time Measurement/Waveform Generation Register 7 | G0TM7/G0PO7 | XXXXh |
| 00018Fh | | | |
| 000190h | Group 0 Waveform Generation Control Register 0 | G0POCR0 | 0000 X000b |
| 000191h | Group 0 Waveform Generation Control Register 1 | G0POCR1 | 0X00 X000b |
| 000192h | Group 0 Waveform Generation Control Register 2 | G0POCR2 | 0X00 X000b |
| 000193h | Group 0 Waveform Generation Control Register 3 | G0POCR3 | 0X00 X000b |
| 000194h | Group 0 Waveform Generation Control Register 4 | G0POCR4 | 0X00 X000b |
| 000195h | Group 0 Waveform Generation Control Register 5 | G0POCR5 | 0X00 X000b |
| 000196h | Group 0 Waveform Generation Control Register 6 | G0POCR6 | 0X00 X000b |
| 000197h | Group 0 Waveform Generation Control Register 7 | G0POCR7 | 0X00 X000b |
| 000198h | Group 0 Time Measurement Control Register 0 | G0TMCR0 | 00h |
| 000199h | Group 0 Time Measurement Control Register 1 | G0TMCR1 | 00h |
| 00019Ah | Group 0 Time Measurement Control Register 2 | G0TMCR2 | 00h |
| 00019Bh | Group 0 Time Measurement Control Register 3 | G0TMCR3 | 00h |
| 00019Ch | Group 0 Time Measurement Control Register 4 | G0TMCR4 | 00h |
| 00019Dh | Group 0 Time Measurement Control Register 5 | G0TMCR5 | 00h |
| 00019Eh | Group 0 Time Measurement Control Register 6 | G0TMCR6 | 00h |
| 00019Fh | Group 0 Time Measurement Control Register 7 | G0TMCR7 | 00h |

X: Undefined
Blanks are reserved. No access is allowed.

**Table 4.9 SFR List (9)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 0001A0h | Group 0 Base Timer Register | G0BT | XXXXh |
| 0001A1h | | | |
| 0001A2h | Group 0 Base Timer Control Register 0 | G0BCR0 | 0000 0000b |
| 0001A3h | Group 0 Base Timer Control Register 1 | G0BCR1 | 0000 0000b |
| 0001A4h | Group 0 Time Measurement Prescaler Register 6 | G0TPR6 | 00h |
| 0001A5h | Group 0 Time Measurement Prescaler Register 7 | G0TPR7 | 00h |
| 0001A6h | Group 0 Function Enable Register | G0FE | 00h |
| 0001A7h | Group 0 Function Select Register | G0FS | 00h |
| 0001A8h | | | |
| 0001A9h | | | |
| 0001AAh | | | |
| 0001ABh | | | |
| 0001ACh | | | |
| 0001ADh | | | |
| 0001AEh | | | |
| 0001AFh | | | |
| 0001B0h | | | |
| 0001B1h | | | |
| 0001B2h | | | |
| 0001B3h | | | |
| 0001B4h | | | |
| 0001B5h | | | |
| 0001B6h | | | |
| 0001B7h | | | |
| 0001B8h | | | |
| 0001B9h | | | |
| 0001BAh | | | |
| 0001BBh | | | |
| 0001BCh | | | |
| 0001BDh | | | |
| 0001BEh | | | |
| 0001BFh | | | |
| 0001C0h | | | |
| 0001C1h | | | |
| 0001C2h | | | |
| 0001C3h | | | |
| 0001C4h | UART5 Special Mode Register 4 | U5SMR4 | 00h |
| 0001C5h | UART5 Special Mode Register 3 | U5SMR3 | 00h |
| 0001C6h | UART5 Special Mode Register 2 | U5SMR2 | 00h |
| 0001C7h | UART5 Special Mode Register | U5SMR | 00h |
| 0001C8h | UART5 Transmit/Receive Mode Register | U5MR | 00h |
| 0001C9h | UART5 Bit Rate Register | U5BRG | XXh |
| 0001CAh | UART5 Transmit Buffer Register | U5TB | XXXXh |
| 0001CBh | | | |
| 0001CCh | UART5 Transmit/Receive Control Register 0 | U5C0 | 0000 1000b |
| 0001CDh | UART5 Transmit/Receive Control Register 1 | U5C1 | 0000 0010b |
| 0001CEh | UART5 Receive Buffer Register | U5RB | XXXXh |
| 0001CFh | | | |

X: Undefined
Blanks are reserved. No access is allowed.

**Table 4.18 SFR List (18)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 040000h | Flash Memory Control Register 0 | FMR0 | 0X01 XX00b |
| 040001h | Flash Memory Status Register 0 | FMSR0 | 1000 0000b |
| 040002h | | | |
| 040003h | | | |
| 040004h | | | |
| 040005h | | | |
| 040006h | | | |
| 040007h | | | |
| 040008h | Flash Register Protection Unlock Register 0 | FPR0 | 00h |
| 040009h | Flash Memory Control Register 1 | FMR1 | 0000 0010b |
| 04000Ah | Block Protect Bit Monitor Register 0 | FBPM0 | ??X? ????b (1) |
| 04000Bh | Block Protect Bit Monitor Register 1 | FBPM1 | XXX? ????b (1) |
| 04000Ch | | | |
| 04000Dh | | | |
| 04000Eh | | | |
| 04000Fh | | | |
| 040010h | | | |
| 040011h | Block Protect Bit Monitor Register 2 | FBPM2 | ???? ????b (1) |
| 040012h | | | |
| 040013h | | | |
| 040014h | | | |
| 040015h | | | |
| 040016h | | | |
| 040017h | | | |
| 040018h | | | |
| 040019h | | | |
| 04001Ah | | | |
| 04001Bh | | | |
| 04001Ch | | | |
| 04001Dh | | | |
| 04001Eh | | | |
| 04001Fh | | | |
| 040020h | PLL Control Register 0 | PLC0 | 0000 0001b |
| 040021h | PLL Control Register 1 | PLC1 | 0001 1111b |
| 040022h | | | |
| 040023h | | | |
| 040024h | | | |
| 040025h | | | |
| 040026h | | | |
| 040027h | | | |
| 040028h | | | |
| 040029h | | | |
| 04002Ah | | | |
| 04002Bh | | | |
| 04002Ch | | | |
| 04002Dh | | | |
| 04002Eh | | | |
| 04002Fh | | | |

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The reset value reflects the value of the protect bit for each block in the flash memory.

**Table 4.28 SFR List (28)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 047C60h | CAN0 Mailbox 6: Message Identifier | C0MB6 | XXXX XXXXh |
| 047C61h | | | |
| 047C62h | | | |
| 047C63h | | | |
| 047C64h | | | |
| 047C65h | CAN0 Mailbox 6: Data Length | | XXh |
| 047C66h | CAN0 Mailbox 6: Data Field | | XXXX XXXX |
| 047C67h | | | XXXX XXXXh |
| 047C68h | | | |
| 047C69h | | | |
| 047C6Ah | | | |
| 047C6Bh | | | |
| 047C6Ch | | | |
| 047C6Dh | | | |
| 047C6Eh | CAN0 Mailbox 6: Time Stamp | | XXXXh |
| 047C6Fh | | | |
| 047C70h | CAN0 Mailbox 7: Message Identifier | C0MB7 | XXXX XXXXh |
| 047C71h | | | |
| 047C72h | | | |
| 047C73h | | | |
| 047C74h | | | |
| 047C75h | CAN0 Mailbox 7: Data Length | | XXh |
| 047C76h | CAN0 Mailbox 7: Data Field | | XXXX XXXX |
| 047C77h | | | XXXX XXXXh |
| 047C78h | | | |
| 047C79h | | | |
| 047C7Ah | | | |
| 047C7Bh | | | |
| 047C7Ch | | | |
| 047C7Dh | | | |
| 047C7Eh | CAN0 Mailbox 7: Time Stamp | | XXXXh |
| 047C7Fh | | | |
| 047C80h | CAN0 Mailbox 8: Message Identifier | C0MB8 | XXXX XXXXh |
| 047C81h | | | |
| 047C82h | | | |
| 047C83h | | | |
| 047C84h | | | |
| 047C85h | CAN0 Mailbox 8: Data Length | | XXh |
| 047C86h | CAN0 Mailbox 8: Data Field | | XXXX XXXX |
| 047C87h | | | XXXX XXXXh |
| 047C88h | | | |
| 047C89h | | | |
| 047C8Ah | | | |
| 047C8Bh | | | |
| 047C8Ch | | | |
| 047C8Dh | | | |
| 047C8Eh | CAN0 Mailbox 8: Time Stamp | | XXXXh |
| 047C8Fh | | | |

X: Undefined
Blanks are reserved. No access is allowed.

**Table 4.36 SFR List (36)**

| Address | Register | Symbol | Reset Value |
|---|---|---|---|
| 047DE0h | CAN0 Mailbox 30: Message Identifier | C0MB30 | XXXX XXXXh |
| 047DE1h | | | |
| 047DE2h | | | |
| 047DE3h | | | |
| 047DE4h | | | |
| 047DE5h | CAN0 Mailbox 30: Data Length | | XXh |
| 047DE6h | CAN0 Mailbox 30: Data Field | | XXXX XXXX |
| 047DE7h | | | XXXX XXXXh |
| 047DE8h | | | |
| 047DE9h | | | |
| 047DEAh | | | |
| 047DEBh | | | |
| 047DECh | | | |
| 047DEDh | | | |
| 047DEEh | CAN0 Mailbox 30: Time Stamp | | XXXXh |
| 047DEFh | | | |
| 047DF0h | CAN0 Mailbox 31: Message Identifier | C0MB31 | XXXX XXXXh |
| 047DF1h | | | |
| 047DF2h | | | |
| 047DF3h | | | |
| 047DF4h | | | |
| 047DF5h | CAN0 Mailbox 31: Data Length | | XXh |
| 047DF6h | CAN0 Mailbox 31: Data Field | | XXXX XXXX |
| 047DF7h | | | XXXX XXXXh |
| 047DF8h | | | |
| 047DF9h | | | |
| 047DFAh | | | |
| 047DFBh | | | |
| 047DFCh | | | |
| 047DFDh | | | |
| 047DFEh | CAN0 Mailbox 31: Time Stamp | | XXXXh |
| 047DFFh | | | |
| 047E00h | CAN0 Mask Register 0 | C0MKR0 | XXXX XXXXh |
| 047E01h | | | |
| 047E02h | | | |
| 047E03h | | | |
| 047E04h | CAN0 Mask Register 1 | C0MKR1 | XXXX XXXXh |
| 047E05h | | | |
| 047E06h | | | |
| 047E07h | | | |
| 047E08h | CAN0 Mask Register 2 | C0MKR2 | XXXX XXXXh |
| 047E09h | | | |
| 047E0Ah | | | |
| 047E0Bh | | | |
| 047E0Ch | CAN0 Mask Register 3 | C0MKR3 | XXXX XXXXh |
| 047E0Dh | | | |
| 047E0Eh | | | |
| 047E0Fh | | | |

X: Undefined
Blanks are reserved. No access is allowed.

**Table 5.3 Operating Conditions (2/5)**
**($V_{CC}$ = 3.0 to 5.5 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted) (1)**

| Symbol | Characteristic | | Value (2) | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_{VDC}$ | Decoupling capacitance for voltage regulator | Inter-pin voltage: 1.5 V | 2.4 | | 10.0 | µF |

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

$V_{CC}$ = 5 V

**Table 5.15 Electrical Characteristics (1/3)**
**($V_{CC}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V, $T_a$ = $T_{opr}$, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)**

| Symbol | Characteristic | | Measurement Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OH}$ = -5 mA | $V_{CC}$ - 2.0 | | $V_{CC}$ | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OH}$ = -200 µA | $V_{CC}$ - 0.3 | | $V_{CC}$ | V |
| $V_{OL}$ | Low level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OL}$ = 5 mA | | | 2.0 | V |
| | | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OL}$ = 200 µA | | | 0.45 | V |

Note:
1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$V_{CC}$ = 5 V

**Timing Requirements ($V_{CC}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted)**

**Table 5.30 Serial Interface**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input clock cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input high level pulse width | 80 | | ns |
| $t_{w(CKL)}$ | CLKi input low level pulse width | 80 | | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 80 | | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | | ns |

**Table 5.31 A/D Trigger Input**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(ADH)}$ | $\overline{ADTRG}$ input high level pulse width<br>Hardware trigger input high level pulse width | $\frac{3}{\phi_{AD}}$ | | ns |
| $t_{w(ADL)}$ | $\overline{ADTRG}$ input low level pulse width<br>Hardware trigger input high level pulse width | 125 | | ns |

**Table 5.32 External Interrupt $\overline{INTi}$ Input**

| Symbol | Characteristic | | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INTi}$ input high level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{c(CPU)}$ + 200 | | ns |
| $t_{w(INL)}$ | $\overline{INTi}$ input low level pulse width | Edge sensitive | 250 | | ns |
| | | Level sensitive | $t_{c(CPU)}$ + 200 | | ns |

**Table 5.33 Intelligent I/O**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(ISCLK2)}$ | ISCLK2 input clock cycle time | 600 | | ns |
| $t_{w(ISCLK2H)}$ | ISCLK2 input high level pulse width | 270 | | ns |
| $t_{w(ISCLK2L)}$ | ISCLK2 input low level pulse width | 270 | | ns |
| $t_{su(RXD-ISCLK2)}$ | ISRXD2 input setup time | 150 | | ns |
| $t_{h(ISCLK2-RXD)}$ | ISRXD2 input hold time | 100 | | ns |

$V_{CC}$ = 5 V

**Switching Characteristics ($V_{CC}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted)**

**Table 5.37 Serial Interface**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6 | | 80 | ns |
| $t_{h(C-Q)}$ | TXDi output hold time | | 0 | | ns |

**Table 5.38 Intelligent I/O**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{d(ISCLK2-TXD)}$ | ISTXD2 output delay time | Refer to Figure 5.6 | | 180 | ns |
| $t_{h(ISCLK2-RXD)}$ | ISTXD2 output hold time | | 0 | | ns |

**Table 5.39 Multi-master I²C-bus Interface (standard-mode)**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after START condition/repeated START condition | | $20 \times t_{c(\phi IIC)} - 120$ | $52 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Repeated START condition/STOP condition output delay time after MSCL becomes high | | $20 \times t_{c(\phi IIC)} + 40$ | $52 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

**Table 5.40 Multi-master I²C-bus Interface (fast-mode)**

| Symbol | Characteristic | Measurement Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $t_{f(SCL)}$ | MSCL output fall time | Refer to Figure 5.6 | 2 (1) | | ns |
| $t_{f(SDA)}$ | MSDA output fall time | | 2 (1) | | ns |
| $t_{d(SDA-SCL)S}$ | MSCL output delay time after START condition/repeated START condition | | $10 \times t_{c(\phi IIC)} - 120$ | $26 \times t_{c(\phi IIC)} - 40$ | ns |
| $t_{d(SCL-SDA)P}$ | Repeated START condition/STOP condition output delay time after MSCL becomes high | | $10 \times t_{c(\phi IIC)} + 40$ | $26 \times t_{c(\phi IIC)} + 120$ | ns |
| $t_{d(SCL-SDA)}$ | MSDA output delay time | | $2 \times t_{c(\phi IIC)} + 40$ | $3 \times t_{c(\phi IIC)} + 120$ | ns |

Note:

1. External circuits are required to satisfy the I²C-bus specification.

$V_{CC}$ = 3.3 V

**Table 5.41 Electrical Characteristics (1/3) ($V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0 V, $T_a$ = $T_{opr}$, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)**

| Symbol | Characteristic | | Measurement Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OH}$ = -1 mA | $V_{CC}$ - 0.6 | | $V_{CC}$ | V |
| $V_{OL}$ | Low level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1) | $I_{OL}$ = 1 mA | | | 0.5 | V |

Note:
1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$V_{CC}$ = 3.3 V

**Table 5.43 Electrical Characteristics (3/3)**
**($V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted)**

| Symbol | Characteristic | Measurement Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current | In single-chip mode, output pins are left open and others are connected to $V_{SS}$<br><br>XIN-XOUT<br>Drive strength: low<br><br>XCIN-XCOUT<br>Drive strength: low | $f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN, PLL,<br>Stopped: XCIN, OCO | | 40 | 55 | mA |
| | | | $f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN, PLL,<br>Stopped: XCIN, OCO | | 32 | 45 | mA |
| | | | $f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz,<br>Active: PLL (self-oscillation),<br>Stopped: XIN, XCIN, OCO | | 9 | | mA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO | | 670 | | µA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown | | 180 | | µA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown | | 190 | | µA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz,<br>$f_{(XIN)}$ = 8 MHz,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO,<br>$T_a$ = 25°C, Wait mode | | 500 | 900 | µA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown,<br>$T_a$ = 25°C, Wait mode | | 8 | 140 | µA |
| | | | $f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown,<br>$T_a$ = 25°C, Wait mode | | 10 | 150 | µA |
| | | | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a$ = 25°C | | 5 | 70 | µA |

$V_{CC}$ = 3.3 V

**Table 5.44 A/D Conversion Characteristics ($V_{CC}$ = $AV_{CC}$ = $V_{REF}$ = 3.0 to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_a$ = $T_{opr}$, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)**

| Symbol | Characteristic | Measurement Condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| — | Resolution | $V_{REF}$ = $V_{CC}$ | | | | 10 | Bits |
| — | Absolute error | $V_{REF}$ = $V_{CC}$ = 3.3 V | AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1) | | | ±5 | LSB |
| | | | External op-amp connection mode | | | ±7 | LSB |
| INL | Integral non-linearity error | $V_{REF}$ = $V_{CC}$ = 3.3 V | AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1) | | | ±5 | LSB |
| | | | External op-amp connection mode | | | ±7 | LSB |
| DNL | Differential non-linearity error | $V_{REF}$ = $V_{CC}$ = 3.3 V | | | | ±1 | LSB |
| — | Offset error | | | | | ±3 | LSB |
| — | Gain error | | | | | ±3 | LSB |
| $R_{LADDER}$ | Resistor ladder | $V_{REF}$ = $V_{CC}$ | | 4 | | 20 | kΩ |
| $t_{CONV}$ | Conversion time (10 bits) | $\phi_{AD}$ = 10 MHz, with sample and hold function | | 3.3 | | | µs |
| $t_{CONV}$ | Conversion time (8 bits) | $\phi_{AD}$ = 10 MHz, with sample and hold function | | 2.8 | | | µs |
| $t_{SAMP}$ | Sampling time | $\phi_{AD}$ = 10 MHz | | 0.3 | | | µs |
| $V_{IA}$ | Analog input voltage | | | 0 | | $V_{REF}$ | V |
| $\phi_{AD}$ | Operating clock frequency | Without sample and hold function | | 0.25 | | 10 | MHz |
| | | With sample and hold function | | 1 | | 10 | MHz |

Note:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

## $V_{CC}$ = 3.3 V

**Timing Requirements ($V_{CC}$ = 3.0 to 3.6 V, $V_{SS}$ = 0 V, and $T_a$ = $T_{opr}$, unless otherwise noted)**

**Table 5.46 External Clock Input**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(X)}$ | External clock input period | 62.5 | 250 | ns |
| $t_{w(XH)}$ | External clock input high level pulse width | 25 | | ns |
| $t_{w(XL)}$ | External clock input low level pulse width | 25 | | ns |
| $t_{r(X)}$ | External clock input rise time | | 5 | ns |
| $t_{f(X)}$ | External clock input fall time | | 5 | ns |
| $t_w$ / $t_c$ | External clock input duty | 40 | 60 | % |

**Table 5.47 External Bus Timing**

| Symbol | Characteristic | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{su(D-R)}$ | Data setup time before read | 40 | | ns |
| $t_{h(R-D)}$ | Data hold time after read | 0 | | ns |
| $t_{dis(R-D)}$ | Data disable time after read | | 0.5 × $t_{c(Base)}$ + 10 | ns |

| Revision History | R32C/117 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Nov 19, 2009 | — | Initial release |
| 1.01 | Mar 11, 2010 | — | Second edition released |
| | | — | • Added “128 KB/20KB” and “256KB/20KB” for ROM/RAM capacity |
| 1.10 | Jun 23, 2010 | — | Third edition released |
| | | — | This manual in general<br>• Applied new Renesas templates and formats to the manual<br>• Changed company name to “Renesas Electronics Corporation” and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation (under Chapters 1 and 5)<br>• Added specifications of 64 MHz version |
| | | | **Chapter 1. Overview** |
| | | 3, 5 | • Deleted Note 1 from **Tables 1.2 and 1.4** |
| | | 6 | • Completed “under development” phase of part number R5F6417BDFB in **Table 1.5** |
| | | 11 | • Deleted Note 4 from **Figure 1.2** |
| | | 21 | • Modified expression “fC” in **Table 1.16** to “low speed clocks” |
| | | | **Chapter 4. SFRs** |
| | | 36, 39 | • Changed register name “Group i Timer Measurement Prescaler Register” in **Tables 4.6 and 4.9** to “Group i Time Measurement Prescaler Register” |
| | | 41 | • Modified expression “XY Control Register” in **Table 4.11** to “X-Y Control Register” |
| | | 43 | • Changed register name “UART2 Transmission/Receive Mode Register” in **Table 4.13** to “UART2 Transmit/Receive Mode Register”; Changed hexadecimal format of reset values for registers TABSR, ONSF, and TRGSR to binary |
| | | 54 | • Changed register name “External Interrupt Source Select Register i” in **Table 4.24** to “External Interrupt Request Source Select Register i” |
| | | 69 | • Modified register names “CAN0 Reception Error Count Register” and “CAN0 Transmission Error Count Register” in **Table 4.39** to “CAN0 Receive Error Count Register” and “CAN0 Transmit Error Count Register”, respectively |
| | | | **Chapter 5. Electrical Characteristics** |
| | | 79 | • Changed expressions “$\overline{CS0}$” and “A23 to A0, $\overline{BC3}$ to $\overline{BC0}$” in **Figure 5.5** to “Chip select” and “Address”, respectively |
| | | | **Appendix 1. Package Dimensions** |
| | | 111 | • Added a seating plane to the drawing of package dimension |
| 1.20 | Feb 6, 2013 | — | Fourth edition released |
| | | — | This manual in general<br>• Changed document number “REJ03B0254-0110” to “R01DS0064EJ0120”<br>• Modified expressions “version N”, “version D”, and “version P” to “N version”, “D version”, and “P version”, respectively (under Chapters 1 and 5) |

| Revision History | R32C/117 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| | | | **Chapter 1. Overview** |
| | | — | • Modified wording and enhanced description in this chapter |
| | | 2, 4 | • Modified expressions “Main clock oscillator stop/re-oscillation detection”, “calculation transfer”, “chained transfer”, and “inputs/ outputs” in **Tables 1.1 and 1.3** to “Main clock oscillator stop/restart detection”, “calculation result transfer”, “chain transfer”, and “I/O ports”, respectively |
| | | 6 | • Completed “on planning” phase of part number R5F6417APFB in **Table 1.5** |
| | | 6, 7 | • Completed “under development” phase of versions D and P products in **Tables 1.5 and 1.6** |
| | | 10, 15 | • Changed order of signals in **Figures 1.3 and 1.4** |
| | | 11, 16 | • Changed order of timer pins “TB5IN/TA0IN” in **Tables 1.7 and 1.11** to “TA0IN/TB5IN” |
| | | 21 | • Changed expression “$I^2C$ bus” in **Table 1.16** to “$I^2C$-bus” |
| | | 23 | • Modified Note 1 of **Table 1.18** |
| | | | **Chapter 2. CPU** |
| | | — | • Modified wording and enhanced description in this chapter |
| | | 25 | • Corrected a typo “R3R0” in line 3 of **2.1.1** to “R3R1” |
| | | | **Chapter 3. Memory** |
| | | — | • Modified wording and enhanced description in this chapter |
| | | | **Chapter 4. SFRs** |
| | | — | • Changed expressions “$I^2C$ Bus” and “$I^2C$-Bus” to “$I^2C$-bus” |
| | | 34, 35, 37 | • Changed hexadecimal format of reset values for registers G1BCR0, G2BCR0, and G0BCR0 in **Tables 4.6, 4.7, and 4.9** to binary |
| | | 41 | • Changed register name “Increment/Decrement Counting Select Register” in **Table 4.13** to “Increment/Decrement Select Register” |
| | | 43 | • Corrected reset value “X00X X000b” for AD0CON2 register in **Table 4.15** to “XX0X X000b” |
| | | 53 | • Modified register name “$I^2C$ Bus START Condition/STOP Condition Control Register” in **Table 4.25** to “$I^2C$-bus START and STOP Conditions Control Register”; Corrected reset values for the following registers in: I2CSSCR, I2CCR1, I2CCR2, I2CSR, and I2CMR |
| | | 64, 65 | • Changed register name “CAN0 Acceptance Mask Register k” in **Tables 4.36 and 4.37** to “CAN0 Mask Register k” |
| | | 67 | • Corrected reset value “XXXX XX00b” for C0MSMR register in **Table 4.39** to “0000 0000b” |
| | | | **Chapter 5. Electrical Characteristics** |
| | | — | • Modified wording and enhanced description in this chapter |
| | | 74 | • Changed expression “Programming and erasure endurance of flash memory” in **Table 5.8** to “Program/erase cycles”; Changed its unit “times” to “Cycles” |
| | | 79, 92 | • Added “MSCL” and “MSDA” to **Tables 5.16 and 5.42** |
| | | 80, 93 | • Modified description “Drive power” in **Tables 5.17 and 5.43** to “Drive strength” |
| | | 86, 99 | • Corrected “INTi” in the title of **Tables 5.32 and 5.58** to “$\overline{\text{INT}}$i” |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.