E. Analog Devices Inc./Maxim Integrated - <u>ZLP32300H2008G Datasheet</u>



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Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2008g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

Date	Revision Level	Description	Page Number
February 2008	23	Updated Ordering Information section.	87
January 2008	22	Updated Ordering Information section.	87
July 2007	21	Updated Disclaimer section and implemented style guide.	All
February 2007	20	Updated Low-Voltage Detection.	58
May 2006	19	Updated Figure 33 with pin P22 in SMR block input.	52
December 2005	18	Updated Clock and Input/Output Ports sections.	15 and 51







Pin No	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5, 6, 7
4-7	P04-P07	Input/Output	Port 0, Bits 4, 5, 6, 7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1, 2, 3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to
	Port 3 Bit 0		V _{CC} if not used
			Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0, 1, 2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0–4

Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification





Figure 5. 40-Pin PDIP Pin Configuration





Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 9). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

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(see T8 and T16 Common Functions—CTR1(0D)01h on page 28). Other edge detect and IRQ modes are described in Table 6.

Note: Comparators are powered down by entering STOP mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

 Table 6. Port 3 Pin Function Summary

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 11). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

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P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03h

Table 10 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 10.CTR3 (D)03h: T8/T16 Control Register

Field	Bit Position		Value	Description
T ₁₆ Enable	7	R	0*	Counter Disabled
10		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6	R	0*	Counter Disabled
°		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	5	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode
Reserved	43210	R	1	Always reads 11111
		W	х	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).





T8 TRANSMIT Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 17.

interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 21 and Figure 22).



Figure 21. DEMODULATION Mode Count Capture Flowchart





Figure 22. DEMODULATION Mode Flowchart



Port Configuration

Port Configuration Register

The Port Configuration (PCON) register (see Figure 30) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00h



* Default setting after reset

Figure 30. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of Port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the $Z8^{\mathbb{R}}$ if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 35.

WDTMR(0F)0Fh



*Default setting after reset

Figure 35. Watchdog Timer Mode Register (Write Only)

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Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD} . The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD} . When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note:

If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.



D7	D6	D5	D4	D3	D2	D1	D0		
									TRANSMIT Mode* R/W 0 T16_OUT is 0 initially* 1 T16_OUT is 1 initially DEMODULATION Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 TRANSMIT Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially DEMODULATION Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 TRANSMIT Mode* 0 0 Normal Operation* 0 1 PING-PONG Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 DEMODULATION Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved TRANSMIT Mode/T8/T16 Logic 0 0 AND** 0 1 0R 1 0 NOR 1 1 NAND DEMODULATION Mode 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 0 Roth Edge Detection 1 1 Reserved TRANSMIT Mode 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved TRANSMIT Mode 0 0 P36 as Port Output *
									1 P36 as Port Output ^ 1 P36 as T8/T16_OUT DEMODULATION Mode 0 P31 as Demodulator Input
									1 P20 as Demodulator Input 1 P20 as Demodulator Input TRANSMIT/DEMODULATION Mode
**Defa	fault set	tting afte	er reset er Res	et. Not	reset w	vith a S	Stop M	ode	1 DEMODULATION Mode





R249 IPR(F9H)



Figure 49. Interrupt Priority Register (F9H: Write Only)



R250 IRQ(FAH)



Figure 50. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



*Default setting after reset

* *Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 51. Interrupt Mask Register (FBH: Read/Write)

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R252 Flags(FCH)



Figure 52. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 53. Register Pointer (FDH: Read/Write)





Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.







Figure 65. 48-Pin SSOP Package Design

Note: Contact $Zilog^{\mathbb{R}}$ on the actual bonding diagram and coordinate for chip-on-board assembly.



Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon	ZLP32300H4832G	48-pin SSOP 32 K OTP
ZLP32300	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP

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Device	Part Number	Description			
	ZLP32300P2008G	20-pin PDIP 8 K OTP			
	ZLP32300S2008G	20-pin SOIC 8 K OTP			
	ZLP32300H4804G	48-pin SSOP 4 K OTP			
	ZLP32300P4004G	40-pin PDIP 4 K OTP			
	ZLP32300H2804G	28-pin SSOP 4 K OTP			
	ZLP32300P2804G	28-pin PDIP 4 K OTP			
	ZLP32300S2804G	28-pin SOIC 4 K OTP			
	ZLP32300H2004G	20-pin SSOP 4 K OTP			
	ZLP32300P2004G	20-pin PDIP 4 K OTP			
	ZLP32300S2004G	20-pin SOIC 4 K OTP			
	ZLP323ICE01ZAC*	40-PDIP/48-SSOP Accessory Kit			
	Note: *ZLP323ICE01ZAC h ZCRMZNICE02ZAC	as been replaced by an improved version, G.			
	ZLP128ICE01ZEMG	In-Circuit Emulator			
	Note: *ZLP128ICE01ZEMG has been replaced by an improved version, ZCRMZNICE01ZEMG.				
	ZCRMZNICE01ZEMG	Crimzon In-Circuit Emulator			
	ZCRMZN00100KITG	Crimzon In-Circuit Emulator Development Kit			
	ZCRMZNICE01ZACG	20-Pin Accessory Kit			
	ZCRMZNICE02ZACG	40/48-Pin Accessory Kit			
Notos					

Not

1. Replace C with G for Lead-Free Packaging.

2. Contact <u>www.zilog.com</u> for the die form.

For fast results, contact your local Zilog[®] sales office for assistance in ordering the part(s) desired.