E·XFL



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	· .
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h2032c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



40-Pin PDIP No	48-Pin SSOP No	Symbol
	14	NC
	30	NC
	36	NC

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Input/Output Ports

 \wedge

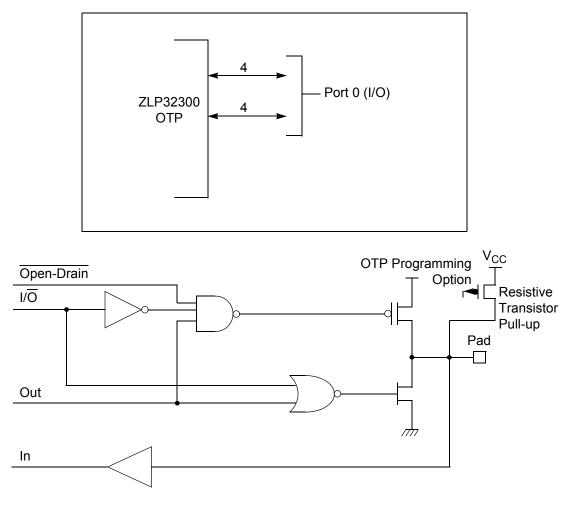
Caution: The CMOS input buffer for each Port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 μ A. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.

Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as







Port 1 (P17–P10)

Port 1 can be configured for standard port input or output mode (see Figure 8). After POR or Stop Mode Recovery, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

- **Notes:** 1. *The Port 1 direction is reset to be input following an SMR.*
 - 2. In 20- and 28-pin packages, Port 1 is reserved. A write to this register will have no effect and will always read FF.



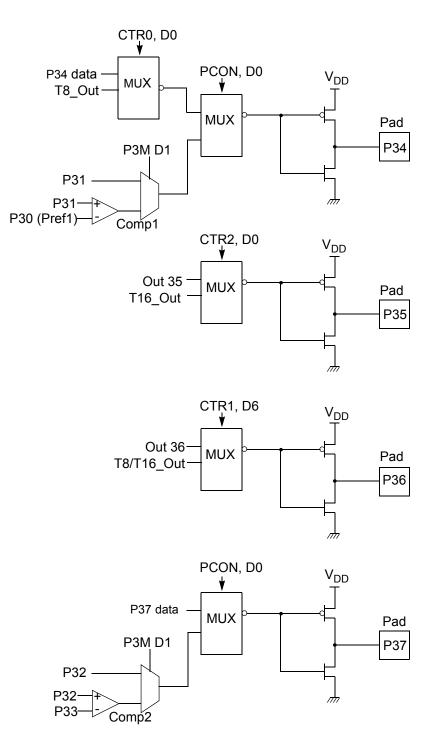


Figure 11. Port 3 Counter/Timer Output Configuration

Initial_T8_Out/Rising_Edge

In TRANSMIT mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8 OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16 OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16 OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02h

Table 9 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
_			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-б	R/W		TRANSMIT Mode
-			0*	Modulo-N
			1	Single Pass
				DEMODULATION Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize
				Edge
Time_Out	5	R	0*	No Counter Timeout
-			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0

Table 9. CTR2(D)02h: Counter/Timer16 Control Register



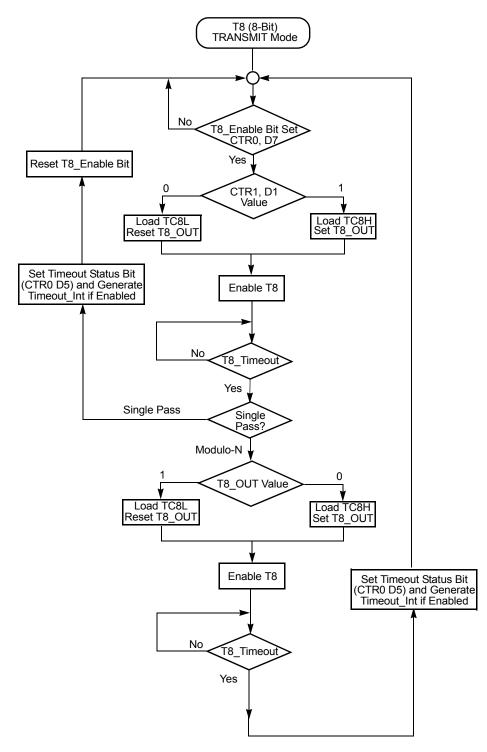
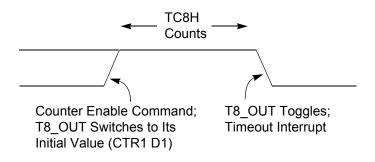


Figure 17. TRANSMIT Mode Flowchart

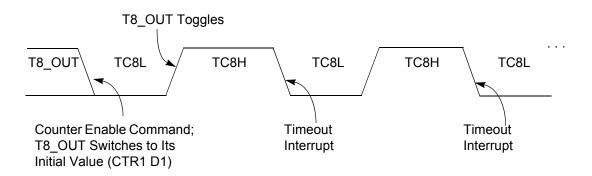


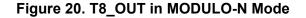
Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see Figure 19 and Figure 20.









T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an

interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 21 and Figure 22).

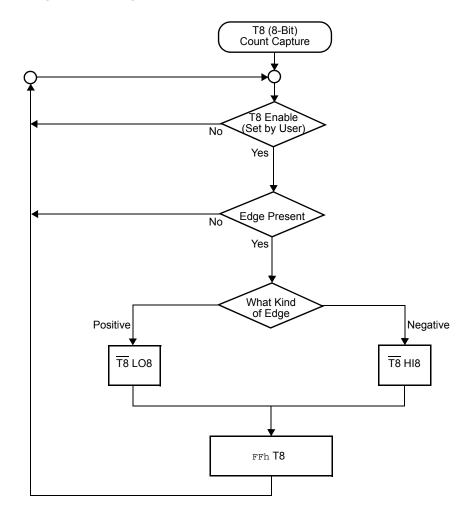


Figure 21. DEMODULATION Mode Count Capture Flowchart

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into SINGLE-PASS mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the PING-PONG mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7), see Figure 26.

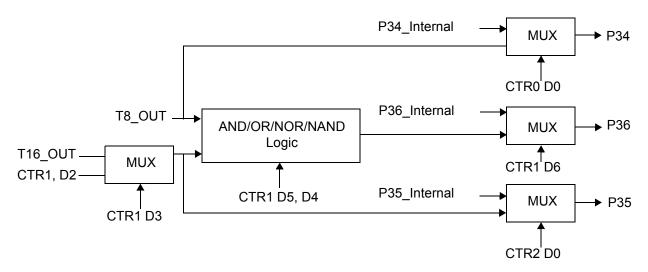


Figure 27. Output Circuit

The initial value of T8 or T16 must not be 1. If you stop the timer and restart the timer, reload the initial value to avoid an unknown previous value.

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Timer Output

The output logic for the timers is displayed in Figure 27. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of TI6-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

Interrupts

The Crimzon ZLP32300 features six different interrupts (see Table 11 on page 45). The interrupts are maskable and prioritized (see Figure 28). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the

zilog ,

Table 13. SMR2(F)0Dh:Stop Mode Recovery Register 2* (Continued)

Field	Bit Position	Value	Description
Source	432 \	N 000 [†]	A. POR Only
		001	B. NAND of P23–P20
		010	C. NAND of P27–P20
		011	D. NOR of P33–P31
		100	E. NAND of P33–P31
		101	F. NOR of P33–P31, P00, P07
		110	G. NAND of P33–P31, P00, P07
		111	H. NAND of P33–P31, P22–P20
Reserved	10	00	Reserved (Must be 0)
*Port pins cont	figured as outputs ar	e ignored	as an SMR recovery source.

[†]Indicates the value upon Power-On Reset.

51



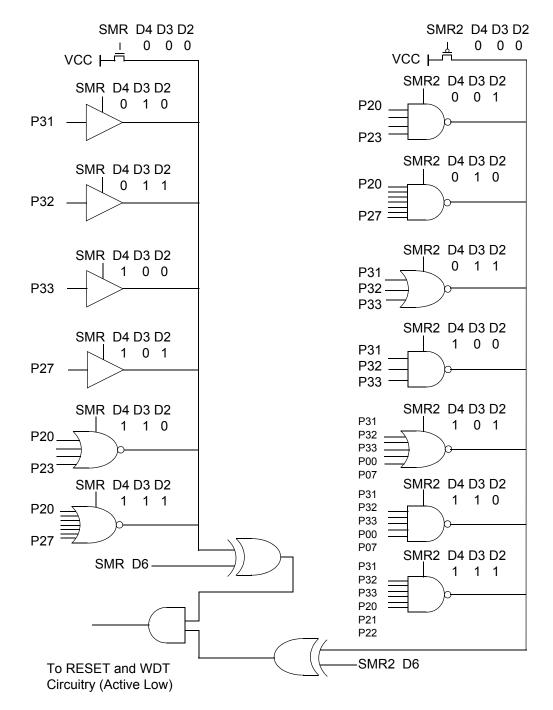


Figure 33. Stop Mode Recovery Source



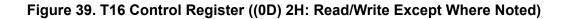


Ensure to differentiate the TRANSMIT mode from DEMODULATION 1. mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

2. Changing from one mode to another cannot be performed without disabling the counter/timers.

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0	
								 0 P35 is Port Output * 1 P35 is TC16 Output 0 Disable T16 Timeout Interrupt* 1 Enable T16 Timeout Interrupt 0 Disable T16 Data Capture Interrupt** 1 Enable T16 Data Capture Interrupt 0 0 SCLK on T16** 0 0 SCLK/2 on T16 1 0 SCLK/2 on T16 1 0 SCLK/8 on T16 1 SCLK/8 on T16 R 0 No T16 Timeout** -R 1 T16 Timeout Occurs W 0 No Effect W 1 Reset Flag to 0
	ault set fault se Reco	tting a			t reset	: with a	Stop Mode	TRANSMIT Mode 0 Modulo-N for T16* 1 Single Pass for T16 DEMODULATOR Mode 0 T16 Recognizes Edge 1 T16 Does Not Recognize Edge R 0 T16 Disabled * R 1 T16 Enabled W 0 Stop T16 W 1 Enable T16

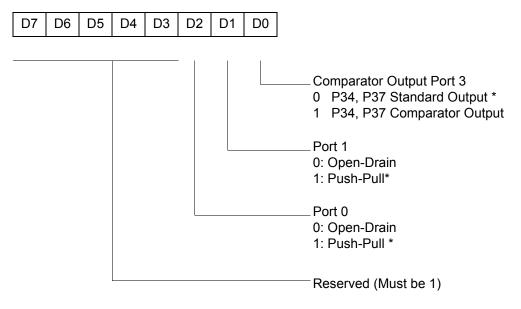




Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H



*Default setting after reset

Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)



Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 18 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 17. Absolute Maximum Ratings

Parameter	Minimum	Maximun	n Units	Notes
Ambient temperature under bias	0	+70	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	
¹ This voltage applies to all pins except the following: V_{DD} , P32,	, P33 and RESET			

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 56).

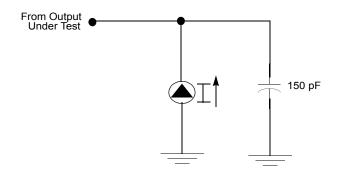
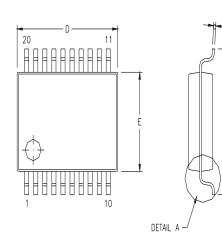
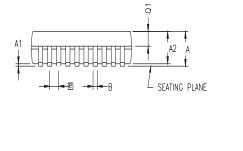


Figure 56. Test Load Diagram





0141001		MILLIMETER		INCH		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
В	0.25	0.30	0.38	0.010	0.012	0.015
С	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
е		0.65 BSC			0.0256 BSC	,
Н	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032



CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

DETAIL A

Н



0-8

INCH

NOM

0.073

0.005

0.068

0.006

0.402

0.209

0.307

0.030

0.0256 TYP



MAX

0.078

0.008

0.070

0.015

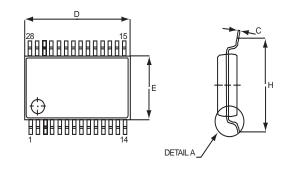
0.008

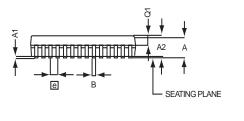
0.407

0.212

0.311

0.037





	1
0-8°	-

SYMBOL

А

A1

A2

В

С

D

Е

е

Н

L

MIN

1.73

0.05

1.68

0.25

0.09

10.07

5.20

7.65

0.63

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

MILLIMETER

NOM

1.86

0.13

1.73

_

10.20

5.30

0.65 TYP

7.80

0.75

MAX

1.99

0.21

1.78

0.38

0.20

10.33

5.38

7.90

0.95

MIN

0.068

0.002

0.066

0.010

0.004

0.397

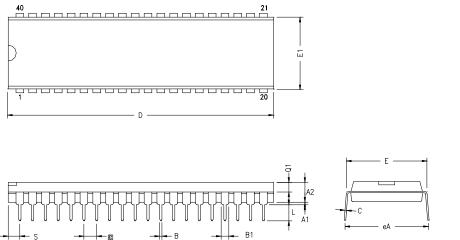
0.205

0.301

0.025







SYMBOL	MILLIN	IETER	INCH		
SIMDUL	MIN	MAX	MIN	MAX	
A1	0.51	1.02	.020	.040	
A2	3.18	3.94	.125	.155	
В	0.38	0.53	.015	.021	
B1	1.02	1.52	.040	.060	
С	0.23	0.38	.009	.015	
D	52.07	52.58	2.050	2.070	
E	15.24	15.75	.600	.620	
E1	13.59	14.22	.535	.560	
e	2.54	TYP	.100 TYP		
eA	15.49	16.76	.610	.660	
L	3.05	3.81	.120	.150	
Q1	1.40	1.91	.055	.075	
S	1.52	2.29	.060	.090	

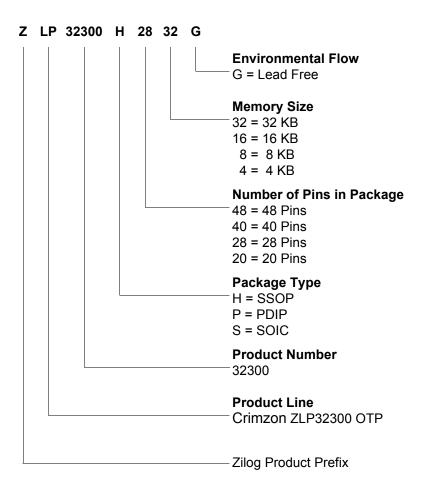
CONTROLLING DIMENSIONS : INCH

Figure 64. 40-Pin PDIP Package Diagram



Part Number Description

Zilog[®] part numbers consist of a number of components, as shown below. ZLP32300H2832G is a Crimzon ZLP32300 OTP product in a 28-pin SSOP package, with 32 KB of OTP and built with lead-free solder.







Index

Numerics

16-bit counter/timer circuits 40 20-pin DIP package diagram 80 20-pin SSOP package diagram 82 28-pin DIP package diagram 84 28-pin SOIC package diagram 83 28-pin SSOP package diagram 85 40-pin DIP package diagram 85 48-pin SSOP package diagram 86 8-bit counter/timer circuits 36

Α

absolute maximum ratings 75 AC characteristics 78 timing diagram 78 address spaces, basic 1 architecture 1 expanded register file 22

В

basic address spaces 1 block diagram, ZLP32300 functional 3

С

capacitance 76 characteristics AC 78 DC 76 clock 46 comparator inputs/outputs 18 configuration port 0 12 port 1 13 port 2 14 port 3 15

port 3 counter/timer 17 counter/timer 16-bit circuits 40 8-bit circuits 36 brown-out voltage/standby 58 clock 46 demodulation mode count capture flowchart 38 demodulation mode flowchart 39 EPROM selectable options 58 glitch filter circuitry 34 halt instruction 47 input circuit 33 interrupt block diagram 44 interrupt types, sources and vectors 45 oscillator configuration 46 output circuit 43 port configuration register 48 resets and WDT 57 SCLK circuit 50 stop instruction 47 stop mode recovery register 49 stop mode recovery register 2 54 stop mode recovery source 52 T16 demodulation mode **41** T16 transmit mode 40 T16 OUT in modulo-N mode 41 T16 OUT in single-pass mode 41 T8 demodulation mode 37 T8 transmit mode 34 T8 OUT in modulo-N mode **37** T8 OUT in single-pass mode 37 transmit mode flowchart 35 voltage detection and flags 59 watch-dog timer mode register 55 watch-dog timer time select 56 CTR(D)01h T8 and T16 Common Functions 29

D

DC characteristics 76 demodulation mode count capture flowchart 38 flowchart 39 T16 41



93

0

oscillator configuration 46 output circuit, counter/timer 43

Ρ

package information 20-pin DIP package diagram 80 20-pin SSOP package diagram 82 28-pin DIP package diagram 84 28-pin SOIC package diagram 83 28-pin SSOP package diagram 85 40-pin DIP package diagram 85 48-pin SSOP package diagram 86 part number format 89 pin configuration 20-pin DIP/SOIC/SSOP 5 28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP **7** 48-pin SSOP 8 pin functions port 0 (P07 - P00) 11 port 0 (P17 - P10) 12 port 0 configuration 12 port 1 configuration 13 port 2 (P27 - P20) 13 port 2 (P37 - P30) 14 port 2 configuration 14 port 3 configuration 15 port 3 counter/timer configuration 17 reset) 18 XTAL1 (time-based input 10 XTAL2 (time-based output) 10 port 0 configuration 12 port 0 pin function 11 port 1 configuration 13 port 1 pin function 12 port 2 configuration 14 port 2 pin function 13 port 3 configuration 15 port 3 pin function 14 port 3counter/timer configuration 17 port configuration register 48

power connections 1 power supply 5 program memory 19 map 20

R

ratings, absolute maximum 75 register 54 CTR(D)01h 28 CTR0(D)00h 27 CTR2(D)02h 31 CTR3(D)03h 33 flag 73 HI16(D)09h 26 HI8(D)0Bh 25 interrupt priority 71 interrupt request 72 interruptmask 72 L016(D)08h 26 L08(D)0Ah 26 LVD(D)0Ch 58 pointer 73 port 0 and 1 70 port 2 configuration 69 port 3 mode 69 port configuration 48, 69 SMR2(F)0Dh 33 stack pointer high 74 stack pointer low 74 stop mode recovery 49 stop mode recovery 2 54 stop mode recovery 66 stop mode recovery 2 67 T16 control 62 T8 and T16 common control functions 61 T8/T16 control 63 TC16H(D)07h 26 TC16L(D)06h 26 TC8 control 60 TC8H(D)05h 27 TC8L(D)04h 27 voltage detection 64 watch-dog timer 68



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For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <u>http://support.zilog.com</u>.