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## What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "[Embedded - Microcontrollers](#)"

### Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2804g">https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2804g</a>

# Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see [Figure 1](#) on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see [Figure 2](#) on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** *All signals with an overline, “ $\overline{\phantom{x}}$ ”, are active Low. For example,  $\overline{B/W}$ , in which *WORD* is active Low, and  $\overline{B/W}$ , in which *BYTE* is active Low.*

Power connections use the conventional descriptions listed in [Table 1](#).

**Table 1. Power Connections**

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

## Development Features

Table 2 lists the features of Crimzon ZLP32300 family.

**Table 2. Crimzon ZLP32300 MCU Features**

Device	OTP(KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon ZLP32300	8, 16, 32	237	32, 24 or 16	2.0–3.6 V
*General purpose				

The additional features include:

- Low power consumption—11 mW (typical)
- Three standby modes:
  - STOP—1.7  $\mu$ A (typical)
  - HALT—0.6 mA (typical)
  - Low-voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One Low-Voltage Detection interrupt
- Low-Voltage Detection and high voltage detection Flags
- Programmable Watchdog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors
  - Port 1: 0–3 pull-up transistors
  - Port 1: 4–7 pull-up transistors

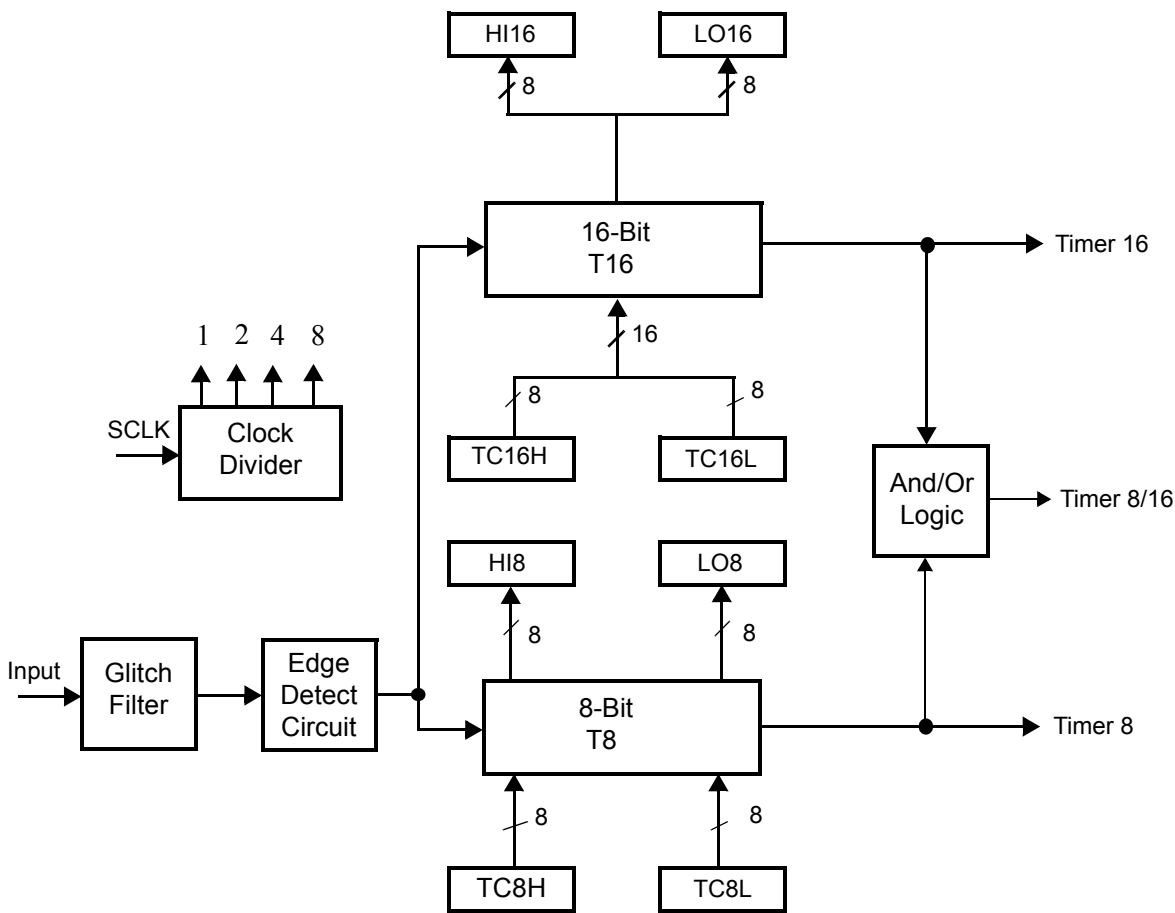
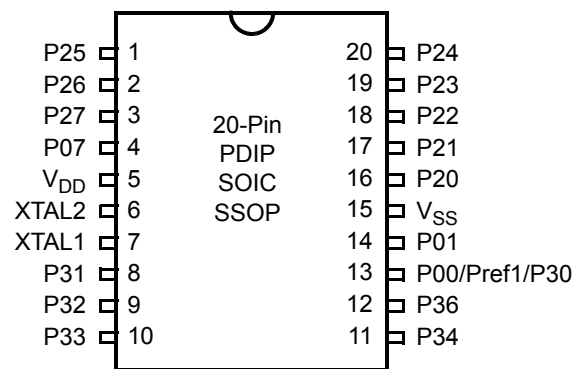


Figure 2. Counter/Timers Diagram

# Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is displayed in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are displayed in Figure 5, Figure 6, and described in Table 5.



**Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration**

**Table 3. 20-Pin PDIP/SOIC/SSOP Pin Identification**

Pin No	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

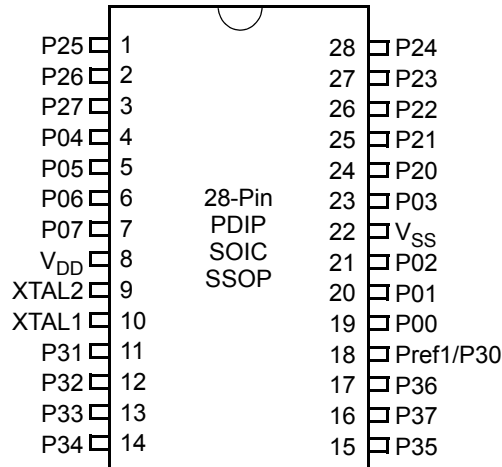


Figure 4. 28-Pin PDIP/SOIC/SSOP Pin Configuration

Table 4. 28-Pin PDIP/SOIC/SSOP Pin Identification

Pin No	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5, 6, 7
4-7	P04-P07	Input/Output	Port 0, Bits 4, 5, 6, 7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1, 2, 3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V <sub>CC</sub> if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0, 1, 2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0–4

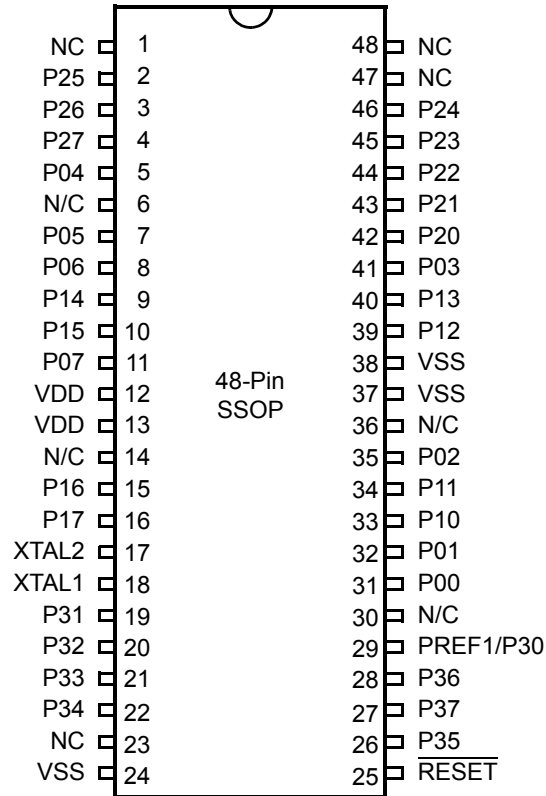
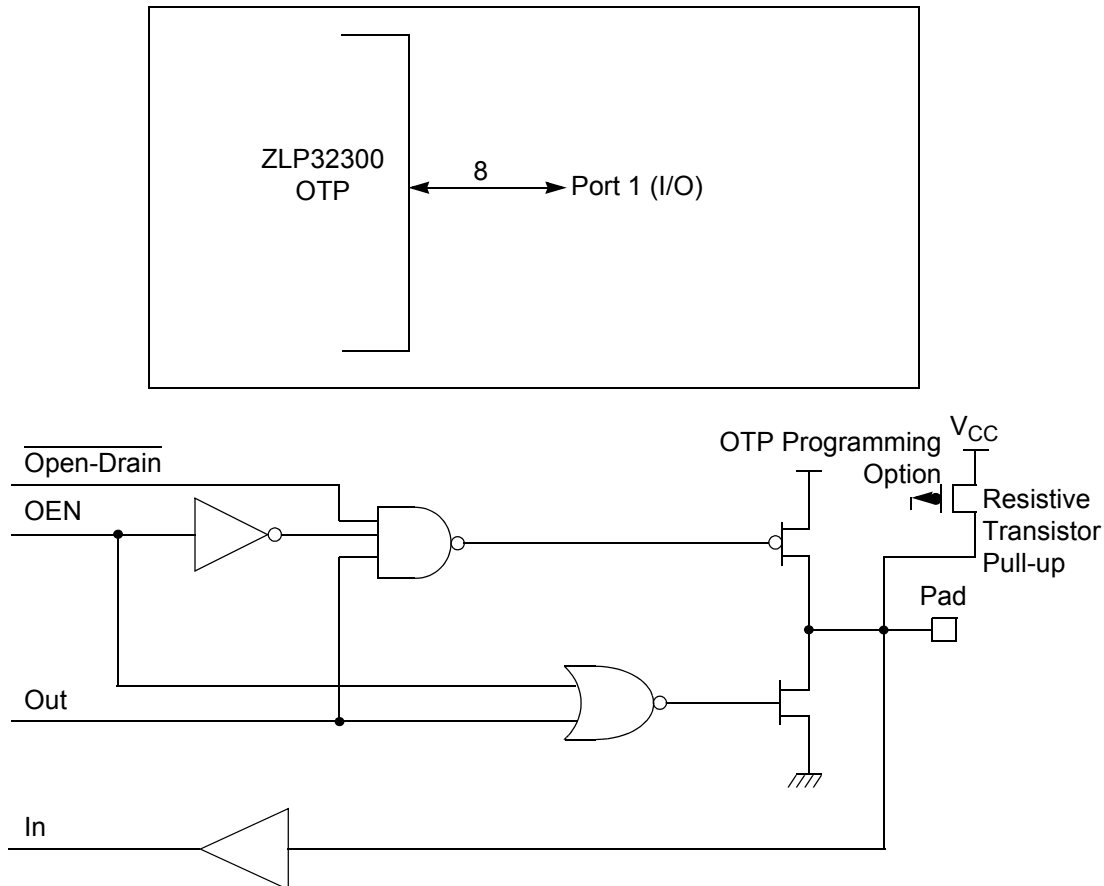


Figure 6. 48-Pin SSOP Pin Configuration

Table 5. 40- and 48-Pin Configuration

40-Pin PDIP No	48-Pin SSOP No	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11



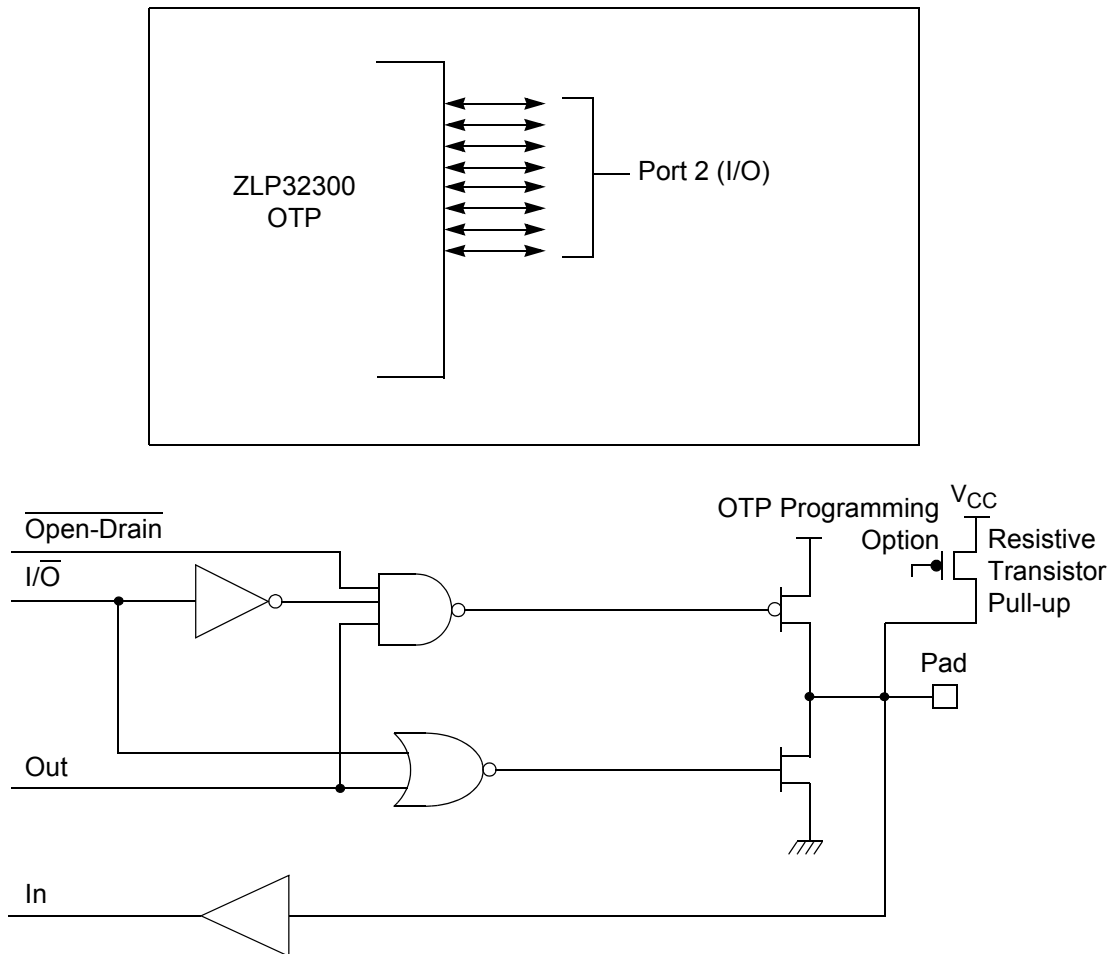
**Figure 8. Port 1 Configuration**

### Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see [Figure 9](#)). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.





**Figure 9. Port 2 Configuration**

### Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see [Figure 10](#)). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

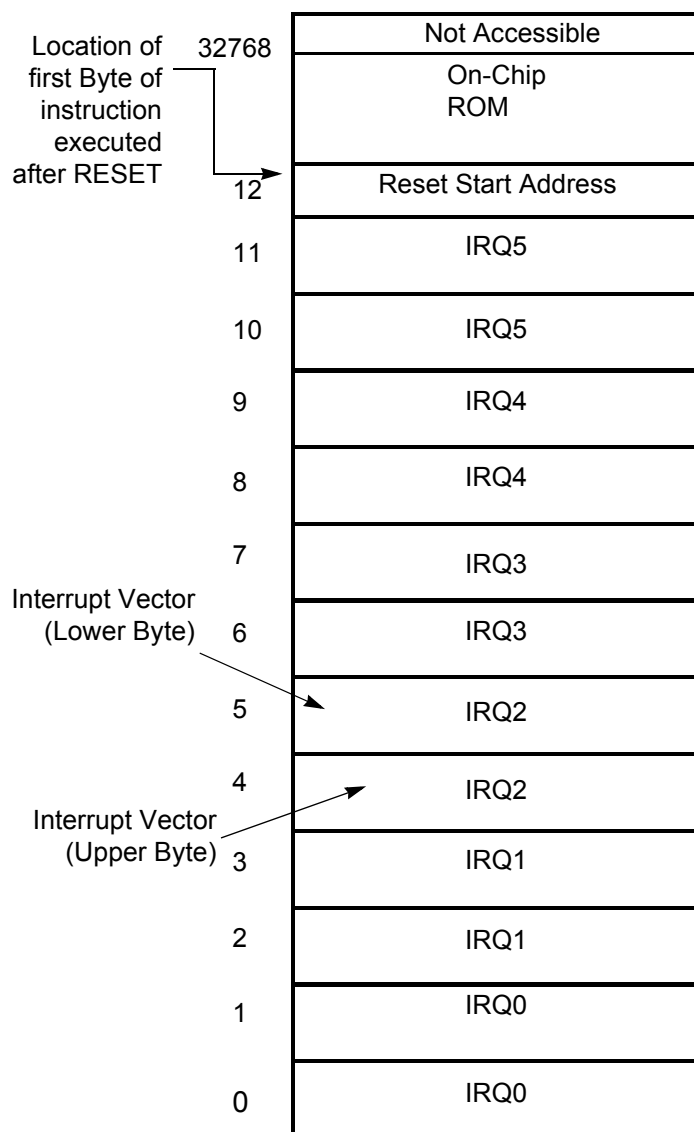
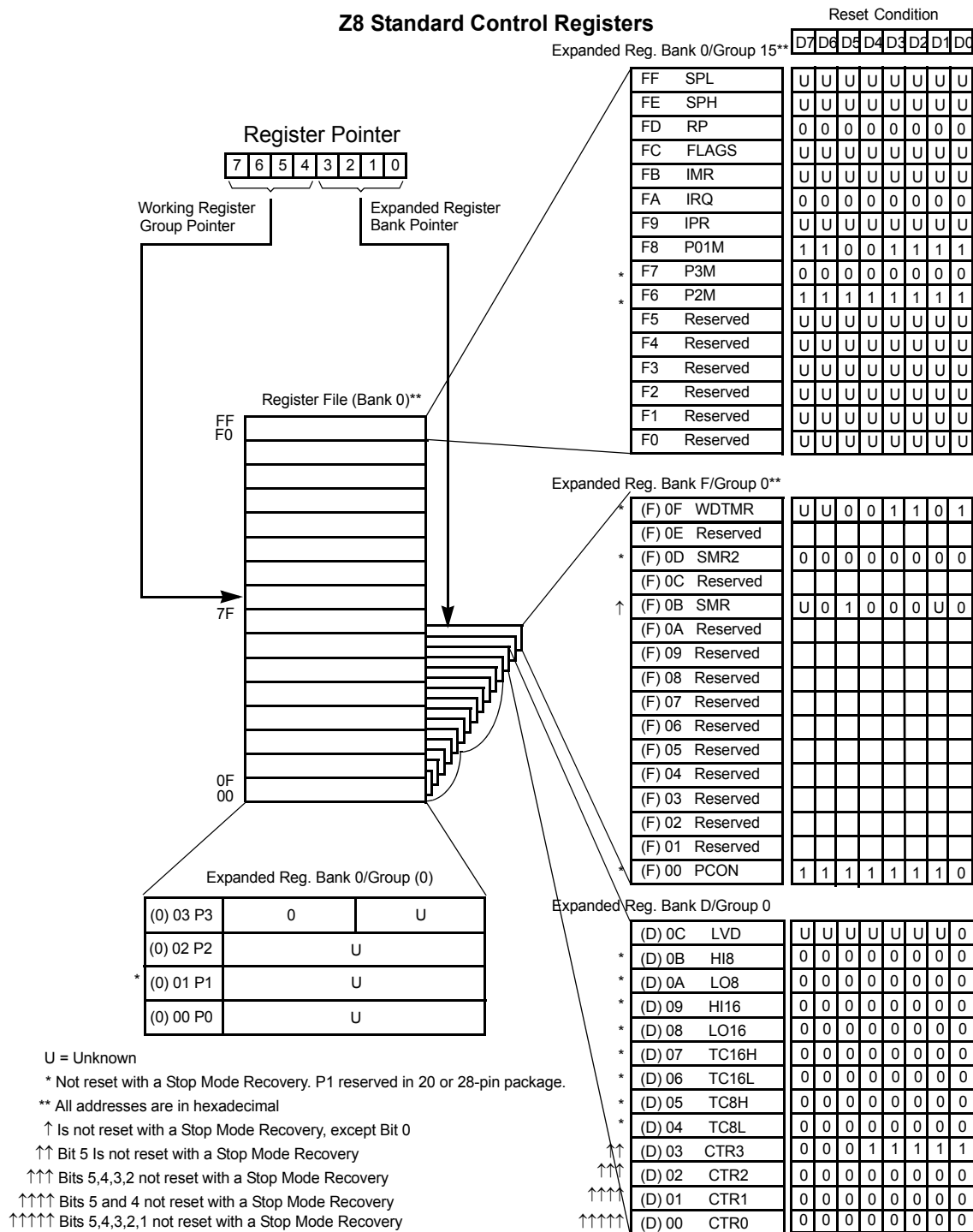


Figure 12. Program Memory Map (32 K OTP)

## Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7–4 of

## Z8 Standard Control Registers

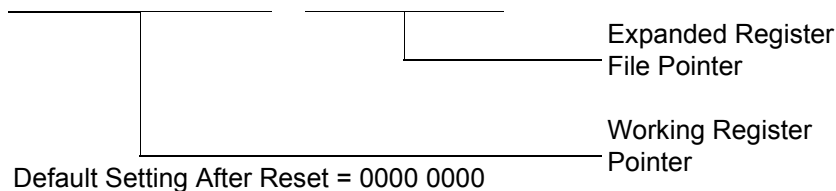


### Figure 13. Expanded Register File Architecture

The upper nibble of the register pointer (see [Figure 14](#)) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLP32300 family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 14. Register Pointer**

**Example:** Crimzon ZLP32300 (see [Figure 13](#) on page 22)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

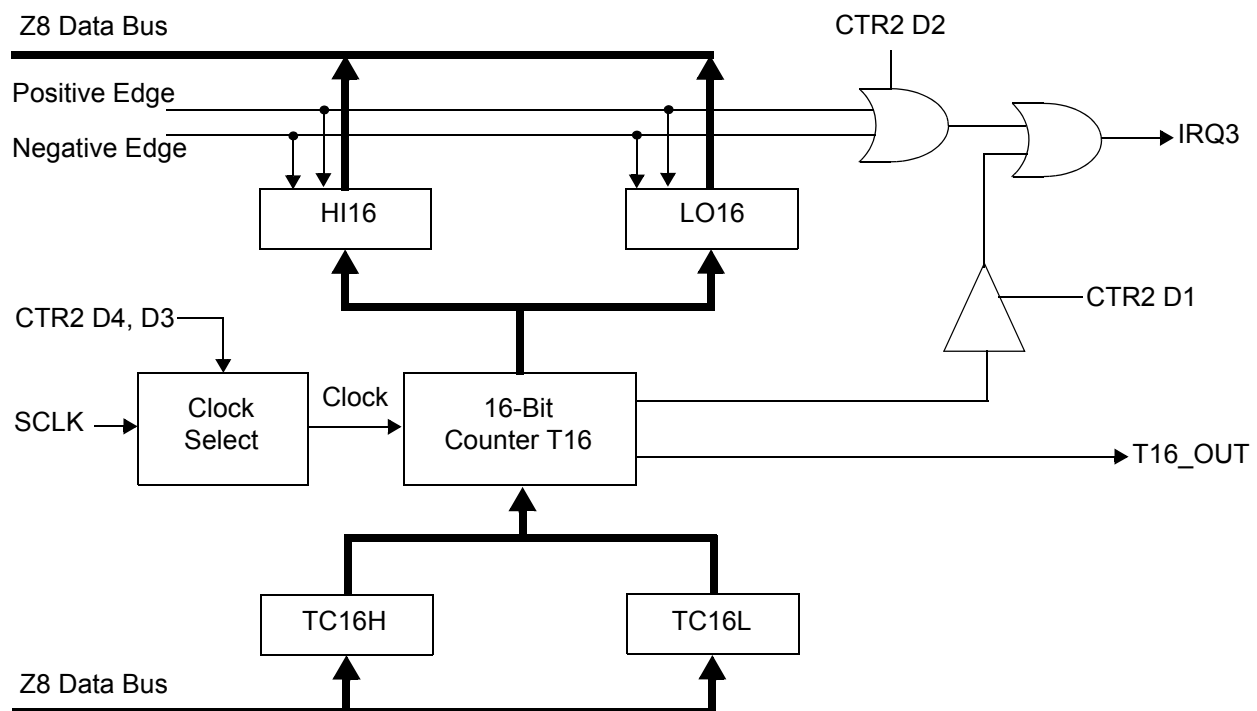
```
LD          RP, #0Dh          ; Select ERF D
for access to bank D

; (working
register group 0)
LD          R0, #xx           ; load CTR0
LD          1, #xx            ; load CTR1
```

### T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16\_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set, see [Figure 23](#).



**Figure 23. 16-Bit Counter/Timer Circuits**

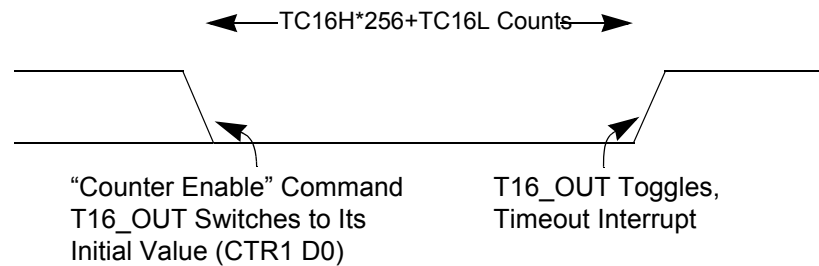
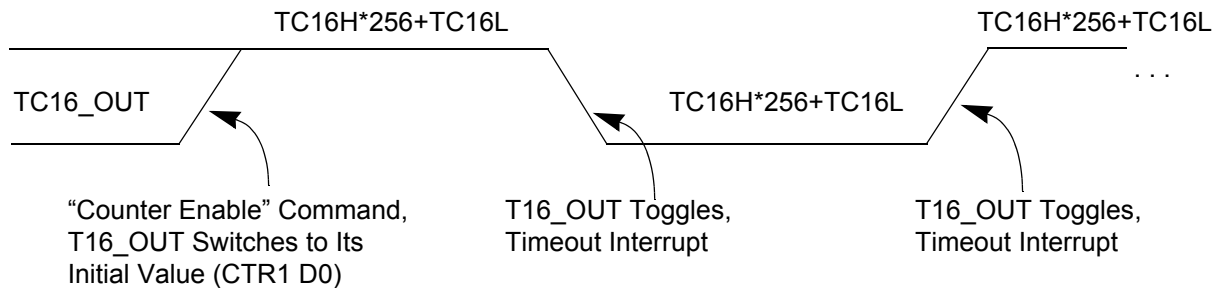
► **Note:** *Global interrupts override this function as described in [Interrupts](#) on page 43.*

If T16 is in SINGLE-PASS mode, it is stopped at this point (see [Figure 24](#)). If it is in MODULO-N mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see [Figure 25](#)).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

**Caution:**

*Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFh to FFFEh. Transition from 0 to FFFFh is not a timeout condition.*

**Figure 24. T16\_OUT in SINGLE-PASS Mode****Figure 25. T16\_OUT in MODULO-N Mode****T16 DEMODULATION Mode**

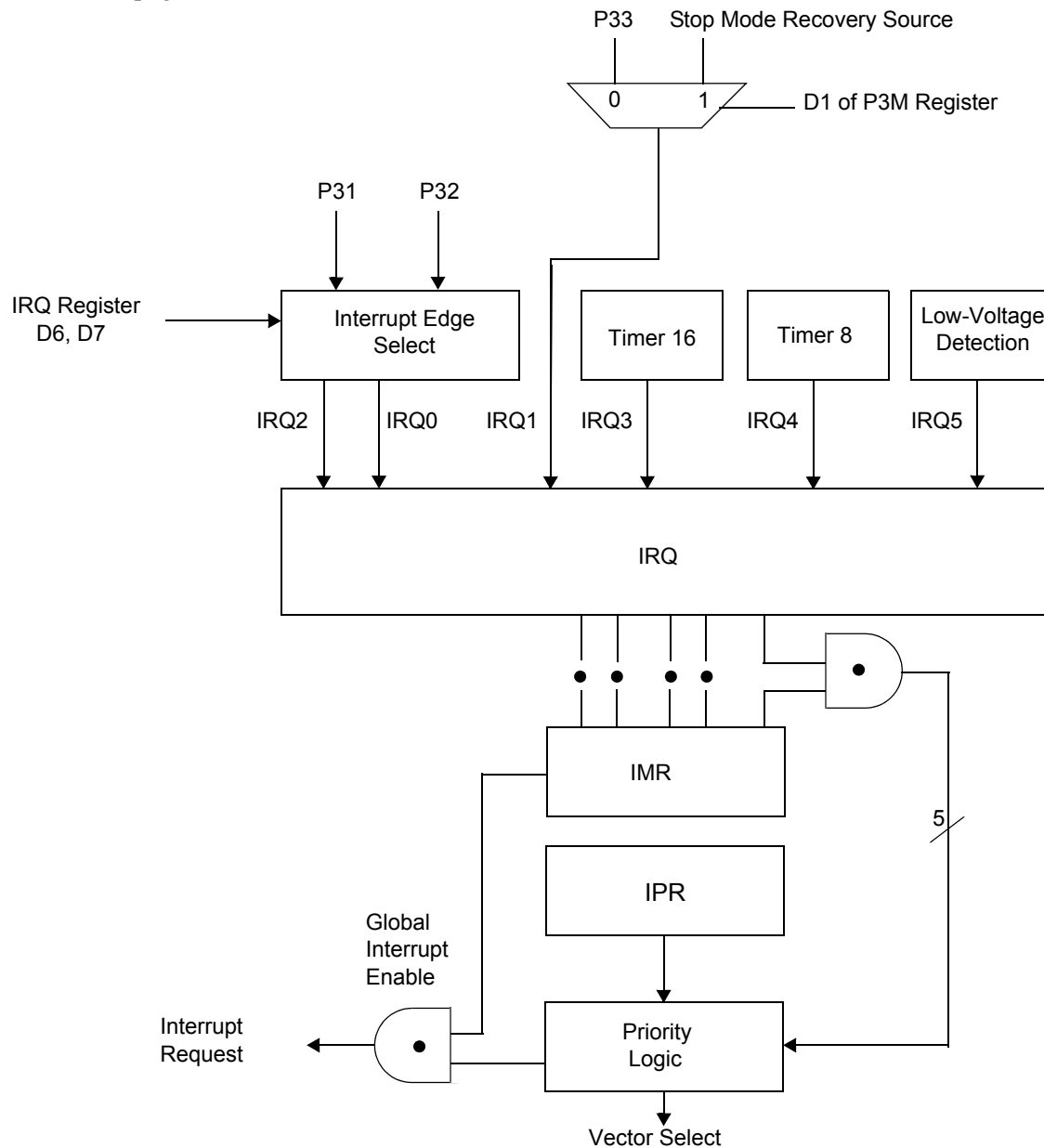
You must program TC16L and TC16H to FFh. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

**If D6 of CTR2 Is 0**

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFh and starts again.

counter/timers (see [Table 11](#) on page 45) and one for low-voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in DIGITAL mode, Pin P33 is the source. When in ANALOG mode, the output of the Stop Mode Recovery source logic is used as the source for the interrupt, see [Figure 33](#) on page 52.



**Figure 28. Interrupt Block Diagram**

**Table 11. Interrupt Types, Sources, and Vectors**

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T <sub>IN</sub>	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Crimzon ZLP32300 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in [Table 12](#).

**Table 12. IRQ Register**

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

**Note:** F = Falling Edge; R = Rising Edge



For both resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

## Power Management

### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

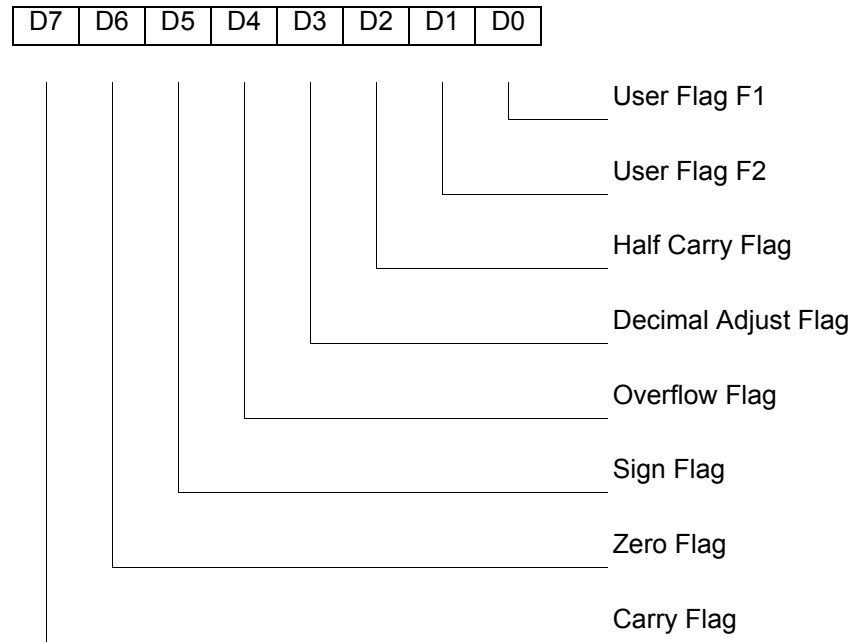
This instruction turns OFF the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP mode is terminated only by a reset, such as WDT time-out, POR or SMR. This condition causes the processor to restart the application program at address 000Ch. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFh) immediately before the appropriate sleep instruction, as follows:

FF	NOP	; clear the pipeline
6F	STOP	; enter Stop Mode

or

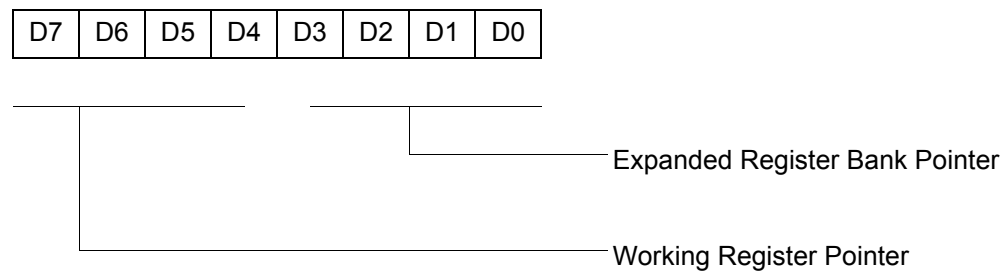
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT Mode

#### R252 Flags(FCH)



**Figure 52. Flag Register (FCH: Read/Write)**

#### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 53. Register Pointer (FDH: Read/Write)**

Table 19. DC Characteristics (Continued)

Symbol	Parameter	T <sub>A</sub> = 0 °C to +70 °C				Units	Conditions	Notes
		V <sub>CC</sub>	Min	Typ <sup>(7)</sup>	Max			
I <sub>IL</sub>	Input Leakage	2.0-3.6	-1		1	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-Up Resistance	2.0	225		675	kΩ	V <sub>IN</sub> = 0 V, Pull-ups selected by mask option	
		3.6	75		275	kΩ		
I <sub>OL</sub>	Output Leakage	2.0-3.6	-1		1	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0		1	3	mA	at 8.0 MHz	1, 2
		3.6		5	10	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0		0.5	1.6	mA	V <sub>IN</sub> = 0V, V <sub>CC</sub> at 8.0	1, 2, 6
		3.6		0.8	2.0		MHz Same as above	1, 2, 6
I <sub>CC2</sub>	Standby Current (STOP Mode)	2.0		1.6	8	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is	3
		3.6		1.8	10	μA	not Running	3
		2.0		5	20	μA	Same as above	3
		3.6		8	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running Same as above	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3 V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.0	V	8 MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VDD and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 °C.

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

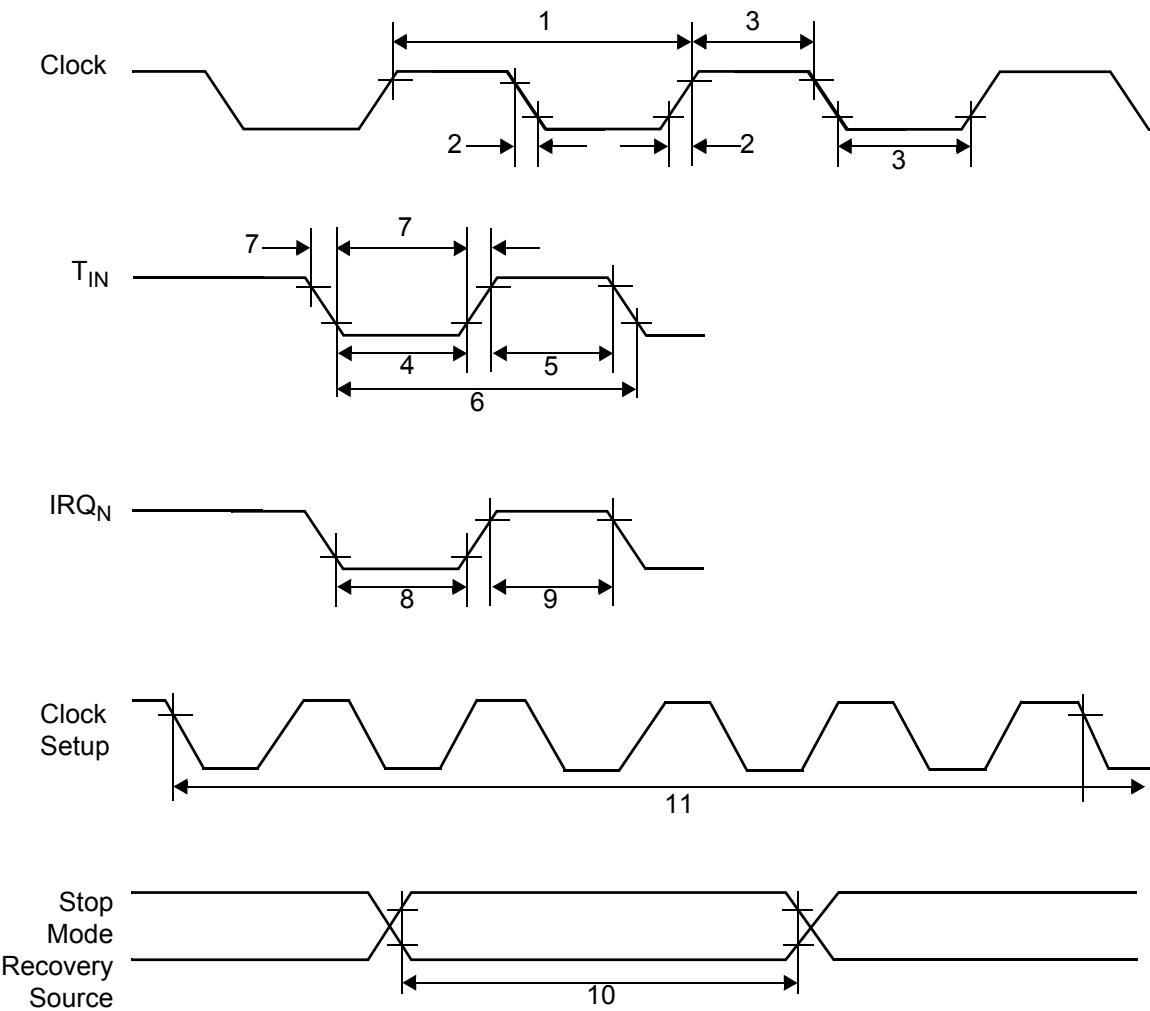


Figure 57. AC Timing Diagram

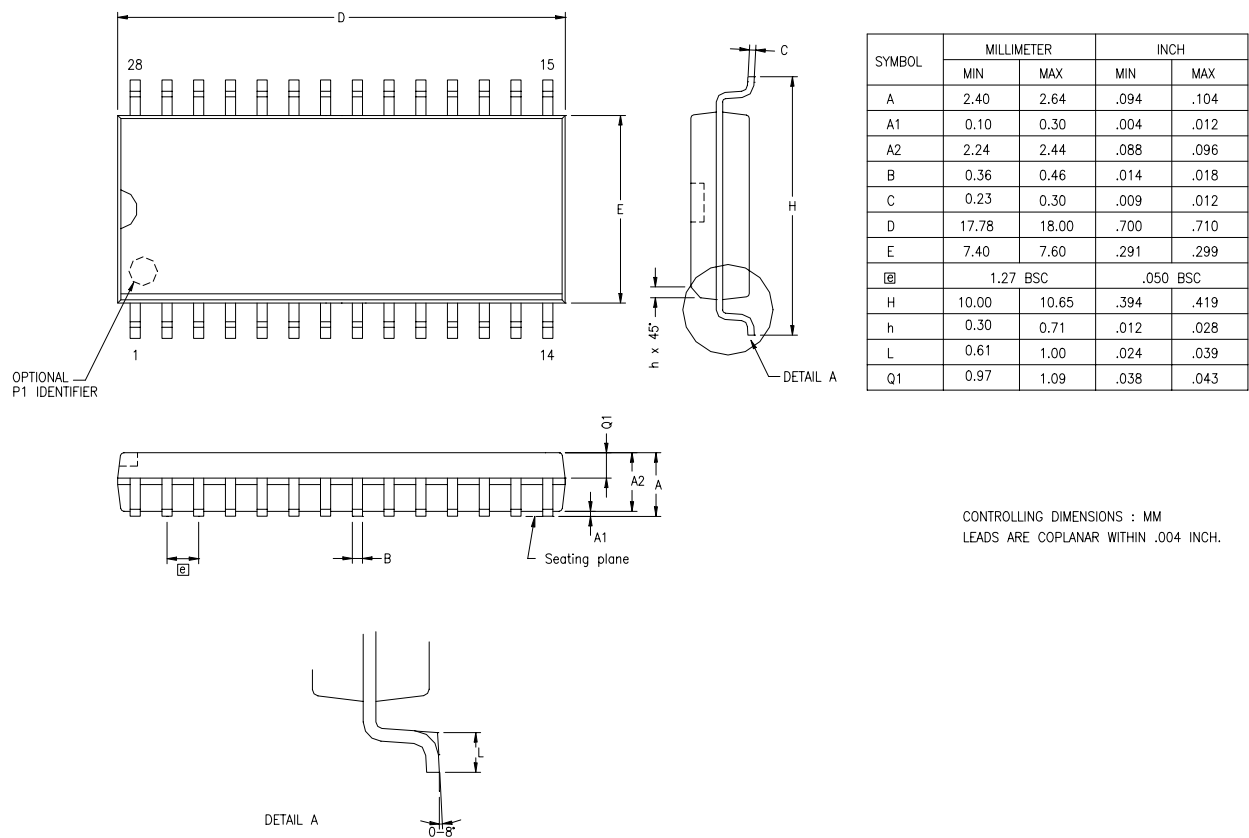


Figure 61. 28-Pin SOIC Package Diagram