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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zlp32300h2808c

Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate link in the table.

Date	Revision Level	Description	Page Number
February 2008	23	Updated Ordering Information section.	87
January 2008	22	Updated Ordering Information section.	87
July 2007	21	Updated Disclaimer section and implemented style guide.	All
February 2007	20	Updated Low-Voltage Detection.	58
May 2006	19	Updated Figure 33 with pin P22 in SMR block input.	52
December 2005	18	Updated Clock and Input/Output Ports sections.	15 and 51

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Architectural Overview

Zilog's Crimzon® ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237 B of general-purpose RAM and 8 KB to 32 KB of OTP, Zilog's CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon ZLP32300 architecture (see Figure 1 on page 3) is based on Zilog's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® CPU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations:

1. Program Memory
2. Register File
3. Expanded Register File

The register file is composed of 256 Bytes of RAM. It includes four I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2 on page 4). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 1.

Table 1. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

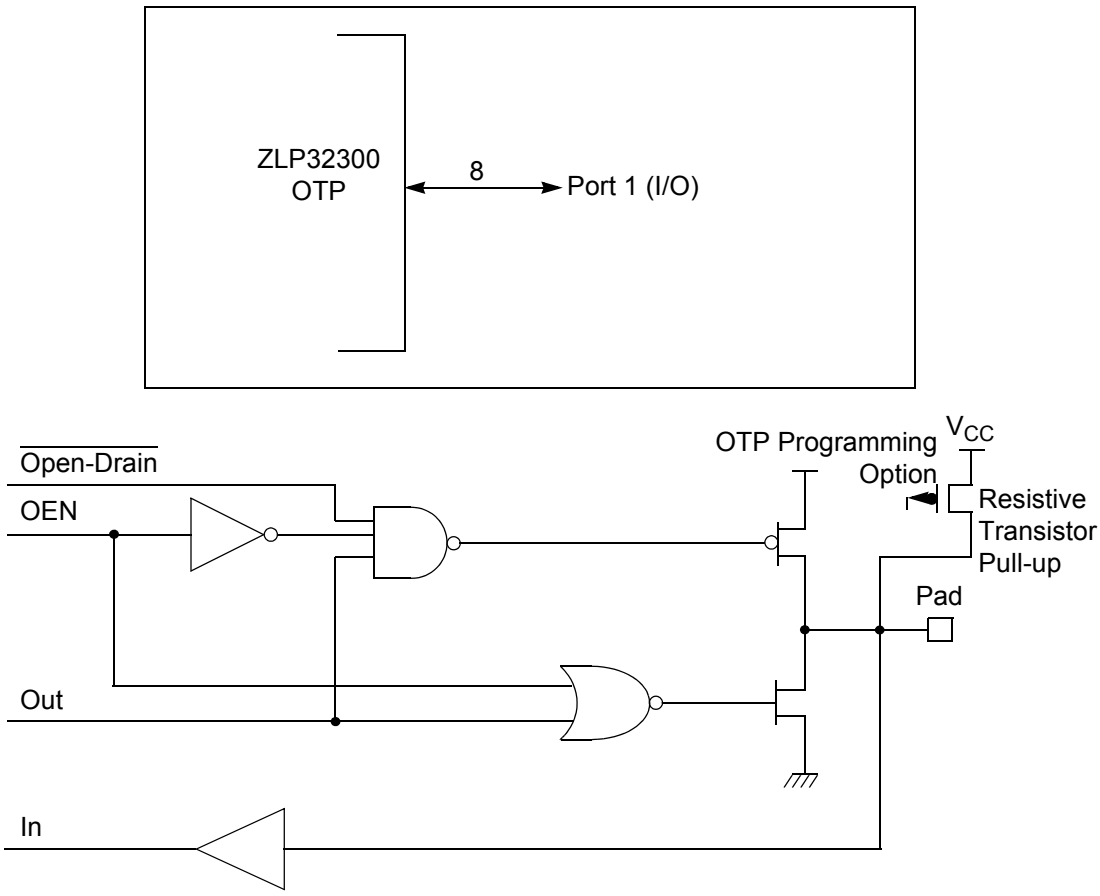


Figure 8. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 9). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.

The upper nibble of the register pointer (see Figure 14) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLP32300 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from `1h` to `Fh` exchanges the lower 16 registers to an expanded register bank.

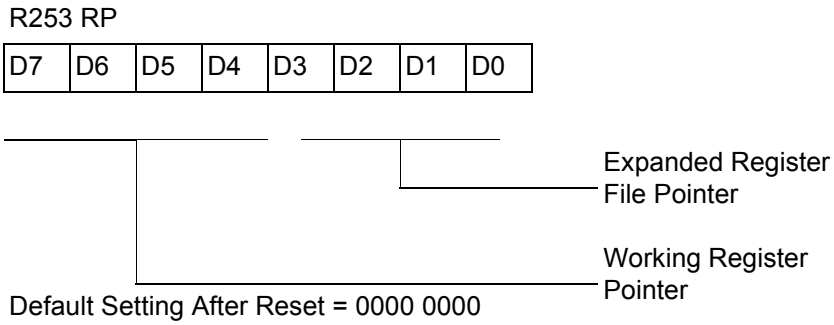


Figure 14. Register Pointer

Example: Crimzon ZLP32300 (see Figure 13 on page 22)

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTR0
R1 = CTR1
R2 = CTR2
R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      R0,#xx                  ; load CTR0
LD                      1, #xx                  ; load CTR1
```

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.

Caution: *Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers. The first clock of T8 might not have complete clock width and can occur any time when enabled.*

Note: *Ensure to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode) when using the OR or AND commands. These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.*

T8 Clock

These bits define the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01h

This register controls the functions in common with the T8 and T16.

Table 8 lists and briefly describes the fields for this register.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03h

Table 10 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Table 10.CTR3 (D)03h: T8/T16 Control Register

Field	Bit Position		Value	Description
T_{16} Enable	7-------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T_8 Enable	-6------	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).

Caution: *Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.*

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see Figure 19 and Figure 20.

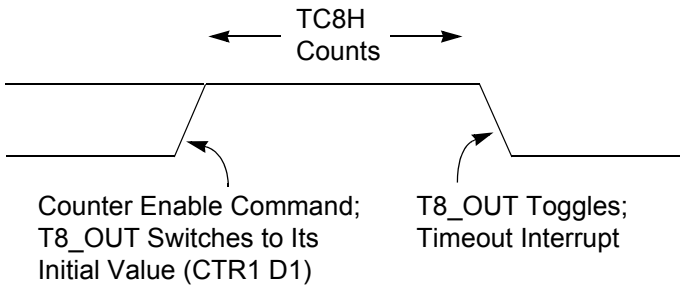


Figure 19. T8_OUT in SINGLE-PASS Mode

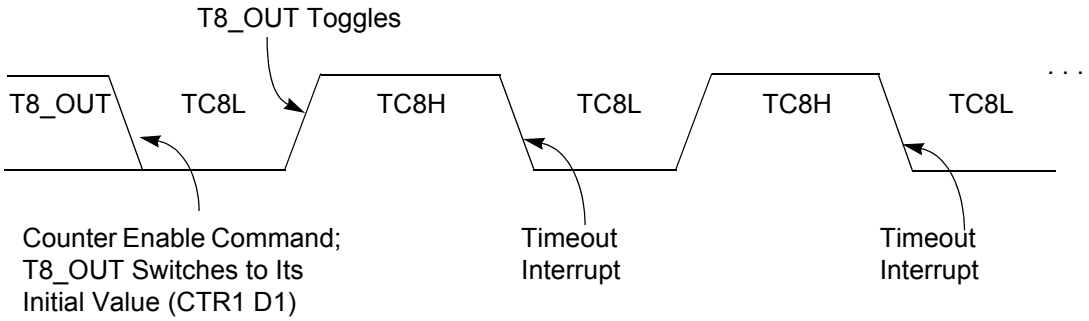


Figure 20. T8_OUT in MODULO-N Mode

T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an

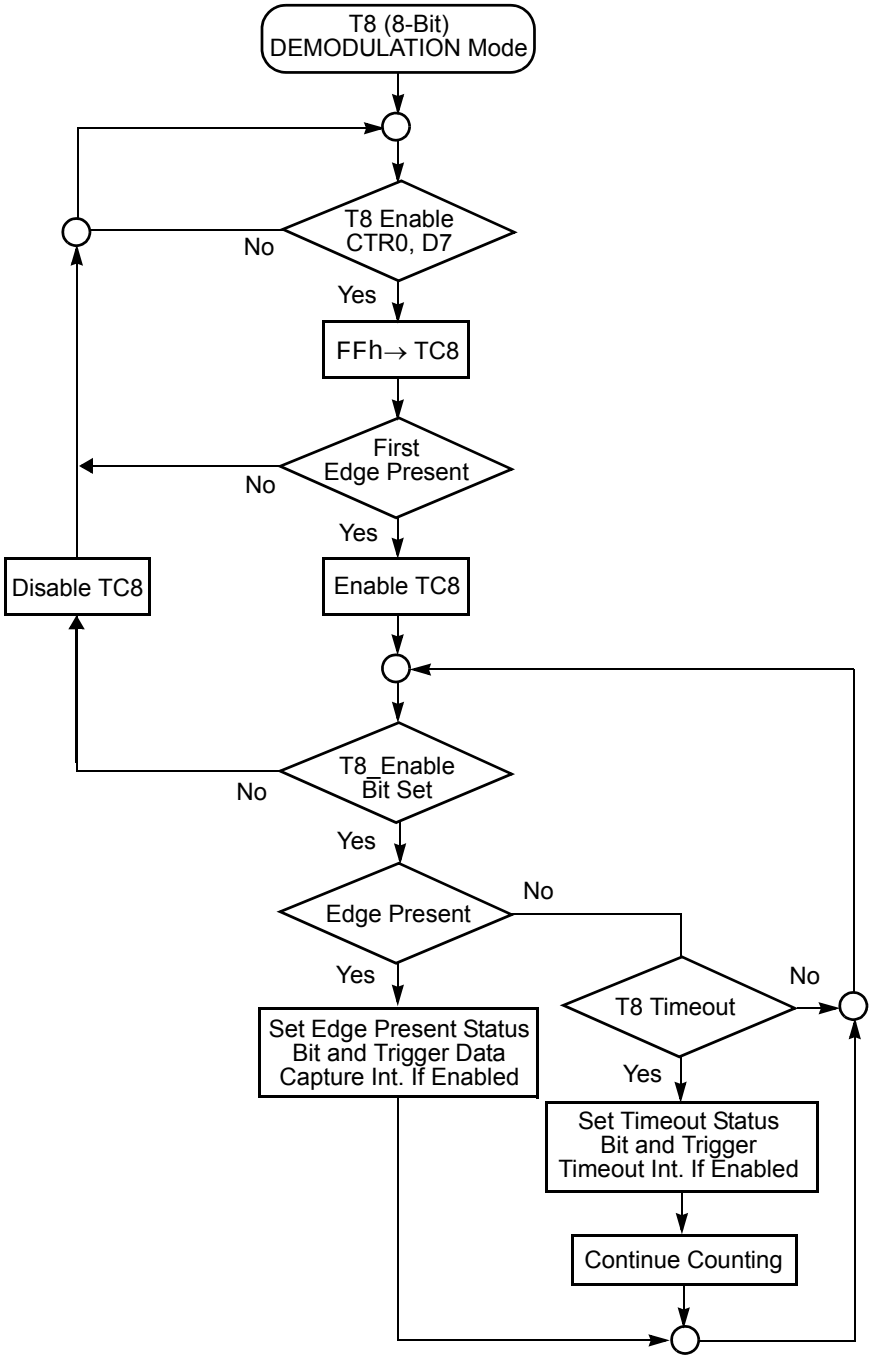


Figure 22. DEMODULATION Mode Flowchart

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see Figure 26.

Note: *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*

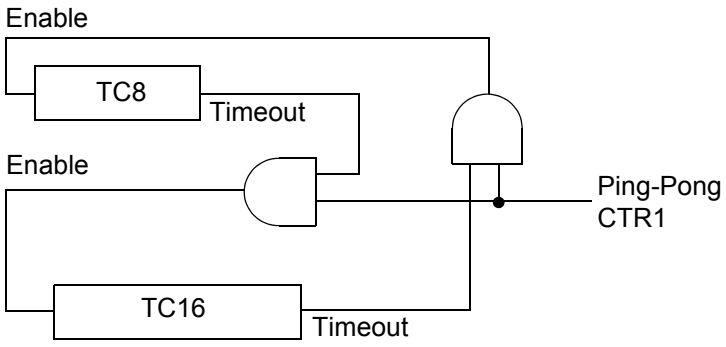


Figure 26. PING-PONG Mode Diagram

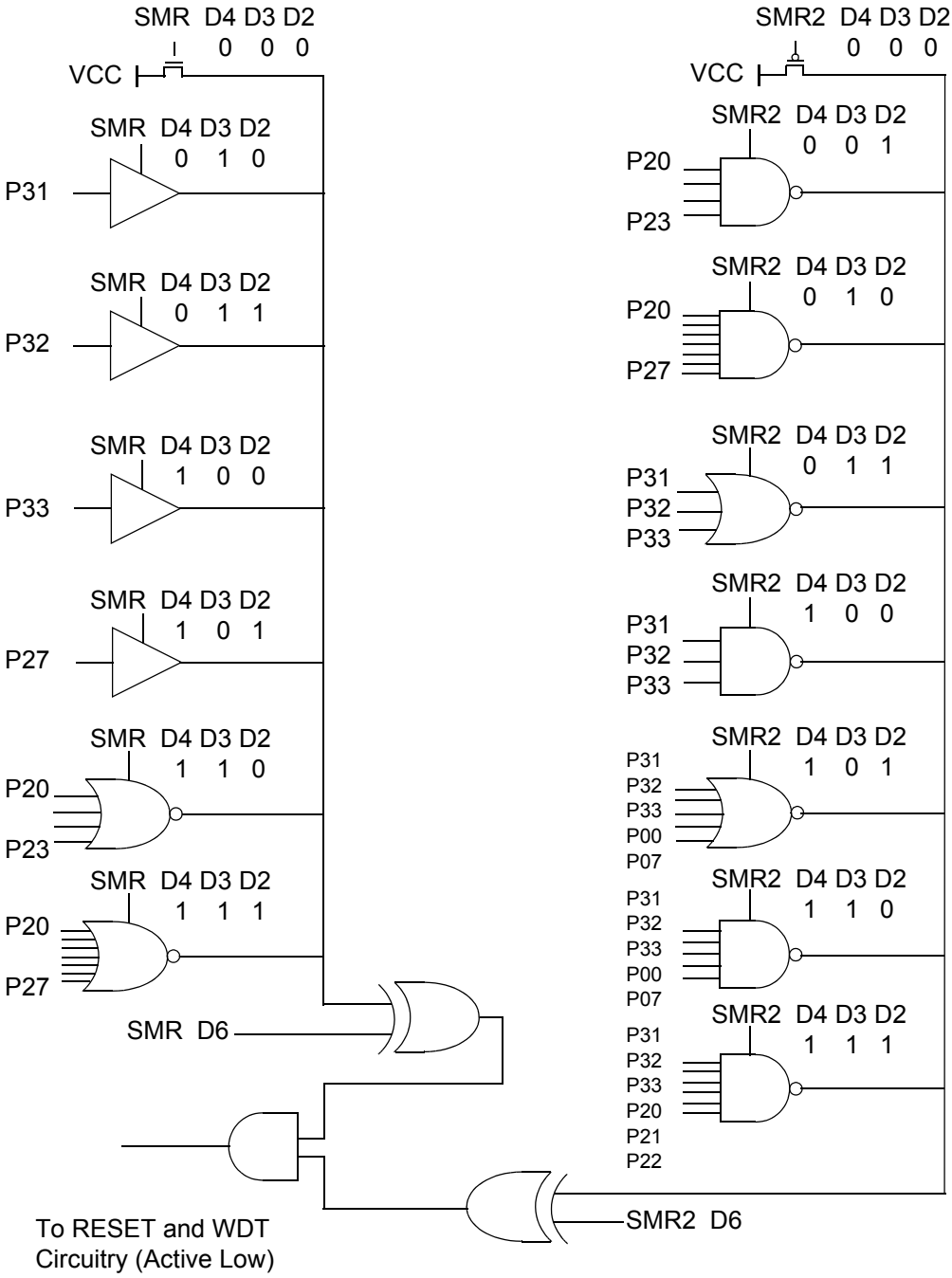


Figure 33. Stop Mode Recovery Source

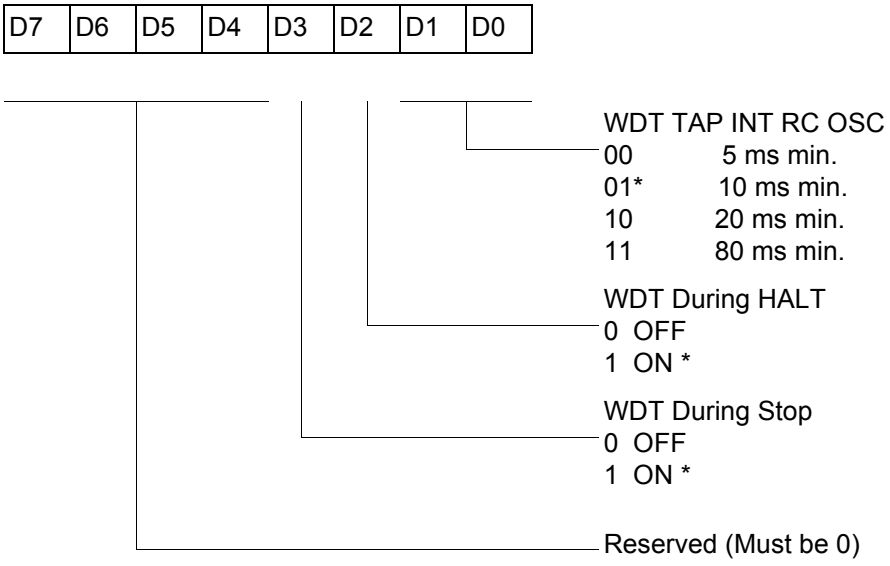
Watchdog Timer Mode

Watchdog Timer Mode Register (WDTMR)

The Watchdog Timer is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) Flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (see Figure 35). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-on reset, Watchdog Reset, or a Stop Mode Recovery (see Figure 34). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 35.

WDTMR(0F)0Fh



*Default setting after reset

Figure 35. Watchdog Timer Mode Register (Write Only)

Table 16. EPROM Selectable Options

Port 00–03 Pull-Ups	ON/OFF
Port 04–07 Pull-Ups	ON/OFF
Port 10–13 Pull-Ups	ON/OFF
Port 14–17 Pull-Ups	ON/OFF
Port 20–27 Pull-Ups	ON/OFF
EPROM Protection	ON/OFF
Watchdog Timer at Power-On Reset	ON/OFF

Voltage Brownout/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection

Low-Voltage Detection Register—LVD(D)0Ch

Note: *Voltage detection does not work at STOP mode.*

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD Flag set HVD Flag reset
	------1-	R	1 0*	LVD Flag set LVD Flag reset
	-------0	R/W	1 0*	Enable VD Disable VD
*Default after POR				

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

Standard Control Registers

The standard control registers are displayed in Figure 46 through Figure 55 on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0

P27–P20 I/O Definition
0 Defines bit as OUTPUT
1 Defines bit as INPUT *

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 46. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0

0: Port 2 Open Drain *
1: Port 2 Push-Pull

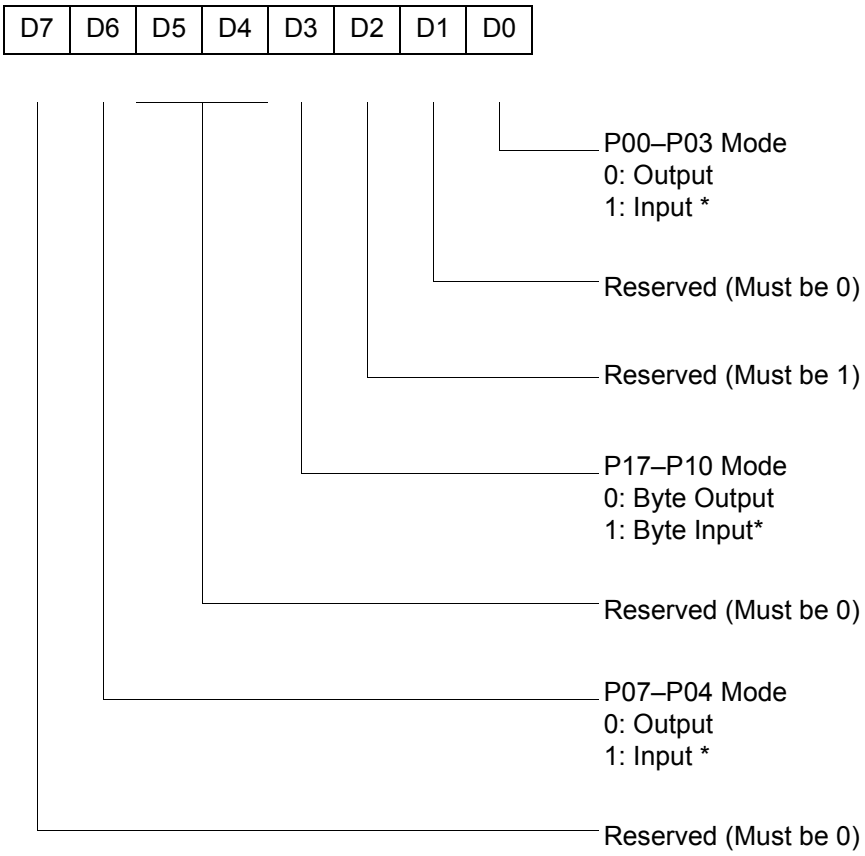
0= P31, P32 DIGITAL Mode*
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 47. Port 3 Mode Register (F7H: Write Only)

R248 P01M(F8H)



*Default setting after reset; only P00, P01 and P07 are available on Crimzon ZLP32300 20-pin configurations.

Figure 48. Port 0 and 1 Mode Register (F8H: Write Only)

R249 IPR(F9H)

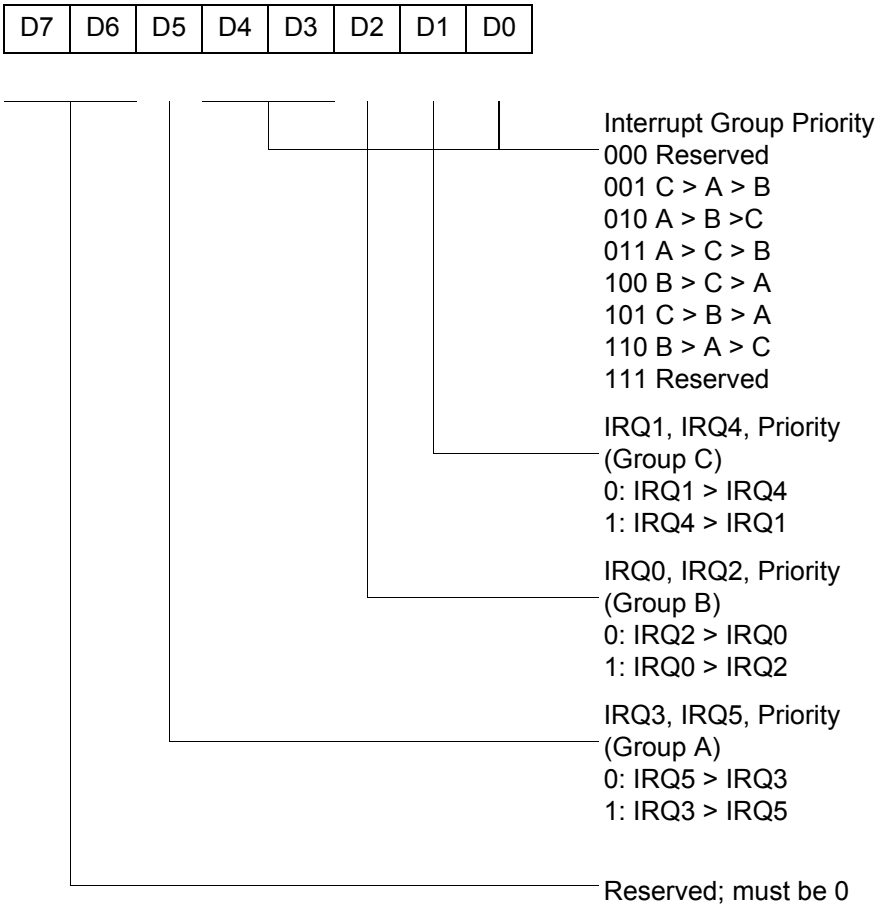


Figure 49. Interrupt Priority Register (F9H: Write Only)

AC Characteristics

Figure 57 and Table 20 describe the Alternating Current (AC) characteristics.

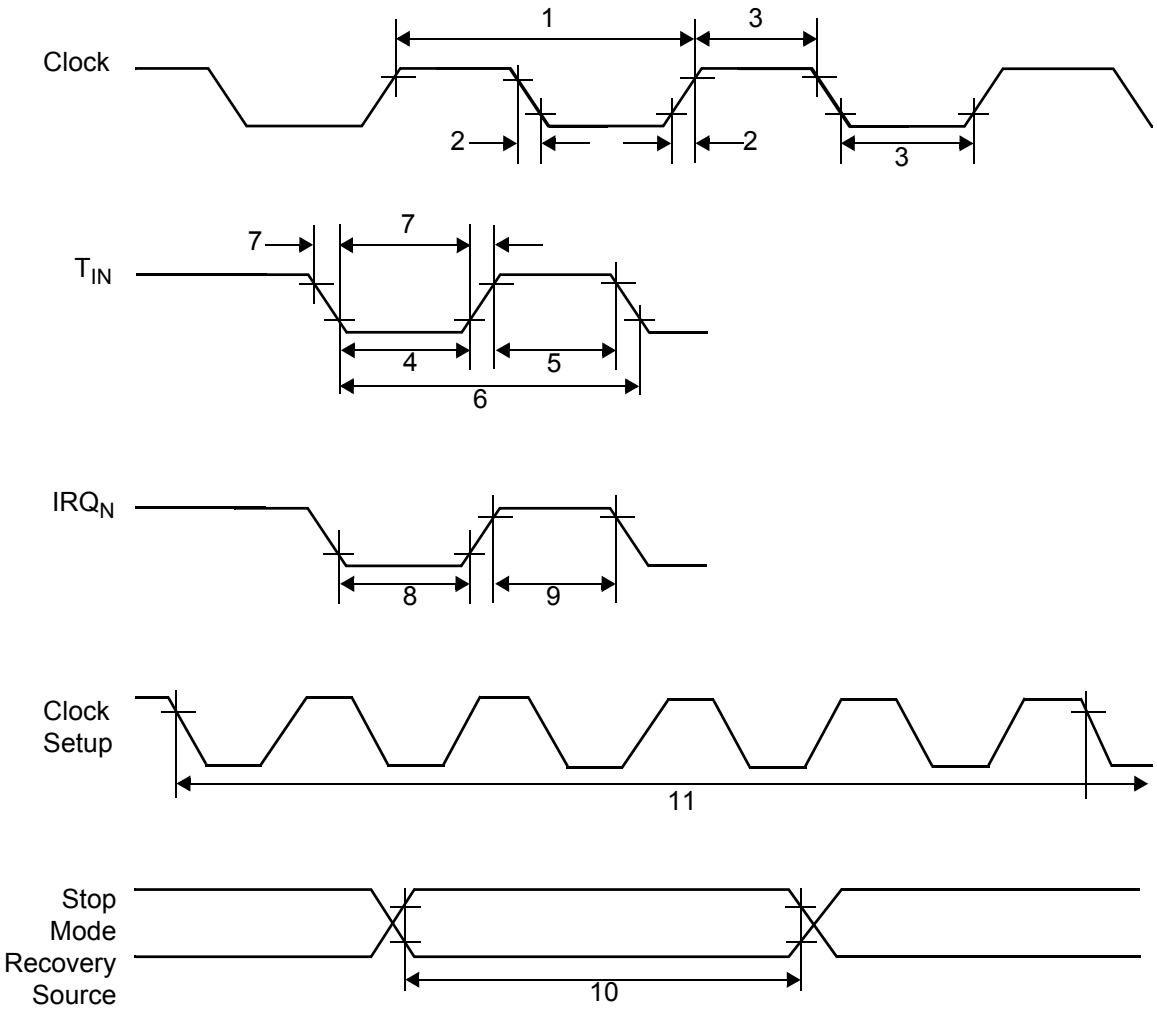


Figure 57. AC Timing Diagram

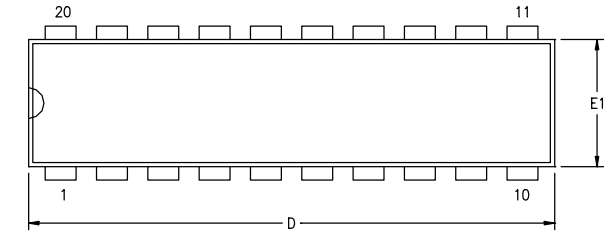
Table 20. AC Characteristics

			T_A=0 °C to +70 °C 8.0 MHz					Watchdog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1	
3	TwC	Input Clock Width	2.0–3.6	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1	
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2	
10	Twsm	Stop Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4	
12	Twdt	Watchdog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-on reset	2.0–3.6	2.5	10	ms		

Notes
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR–D5 = 1.
4. SMR–D5 = 0.

Packaging

Package information for all versions of Crimzon ZLP32300 is displayed in Figure 58 through Figure 65.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 BSC		.100 BSC	
eA	7.87	9.14	.310	.360
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

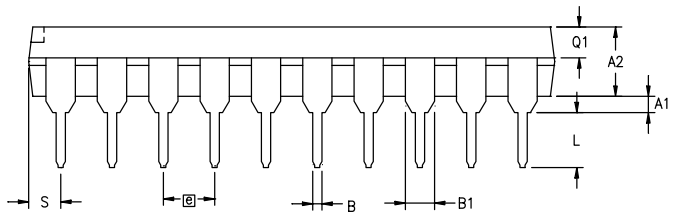
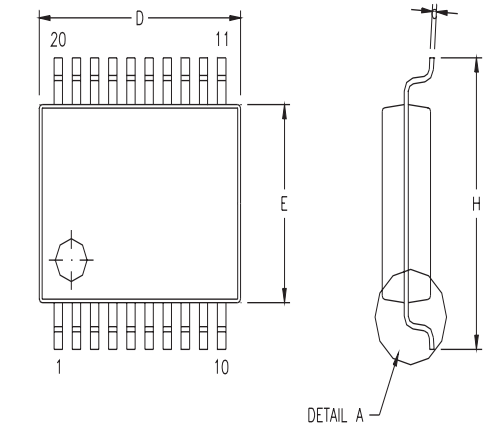
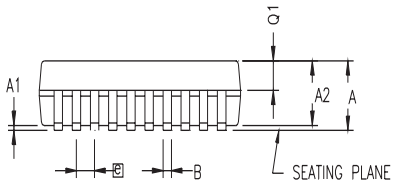
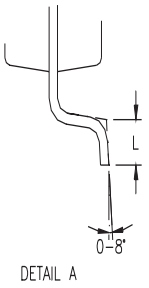


Figure 58. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 60. 20-Pin SSOP Package Diagram