What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2816g

Warning: DO NOT USE IN LIFE SUPPORT

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As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

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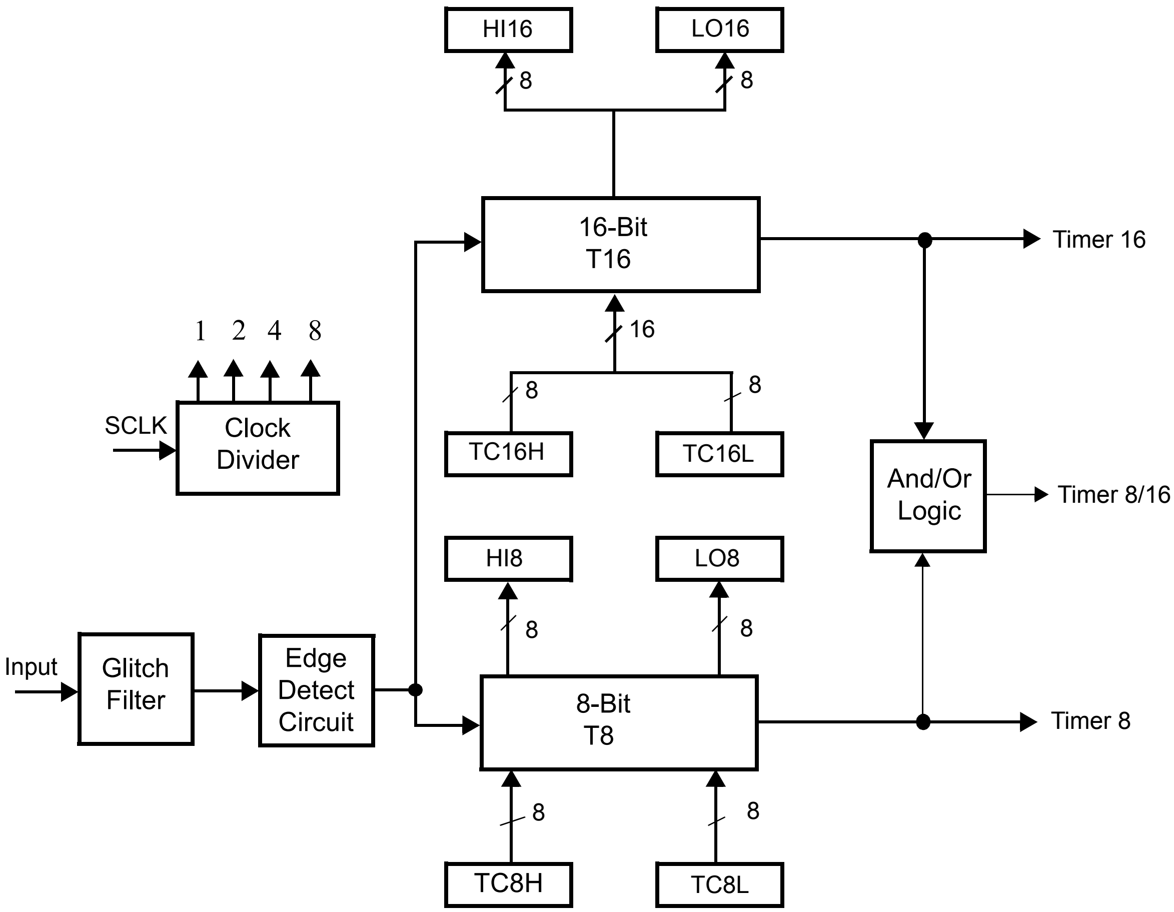


Figure 2. Counter/Timers Diagram

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP No	48-Pin SSOP No	Symbol
32	39	P12
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	$\overline{\text{RESET}}$
15	18	XTAL1
14	17	XTAL2
11	12, 13	V_{DD}
31	24, 37, 38	V_{SS}
25	29	Pref1/P30
	48	NC
	6	NC

Table 5. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP No	48-Pin SSOP No	Symbol
	14	NC
	30	NC
	36	NC

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Input/Output Ports

Caution: *The CMOS input buffer for each Port 0, 1, or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 µA. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.*

Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as

Functional Description

This device incorporates special functions to enhance the Z8 functionality in consumer and battery-operated applications.

Program Memory

This device addresses 32 KB of OTP memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts. See Figure 12.

RAM

This device features 256 B of RAM.

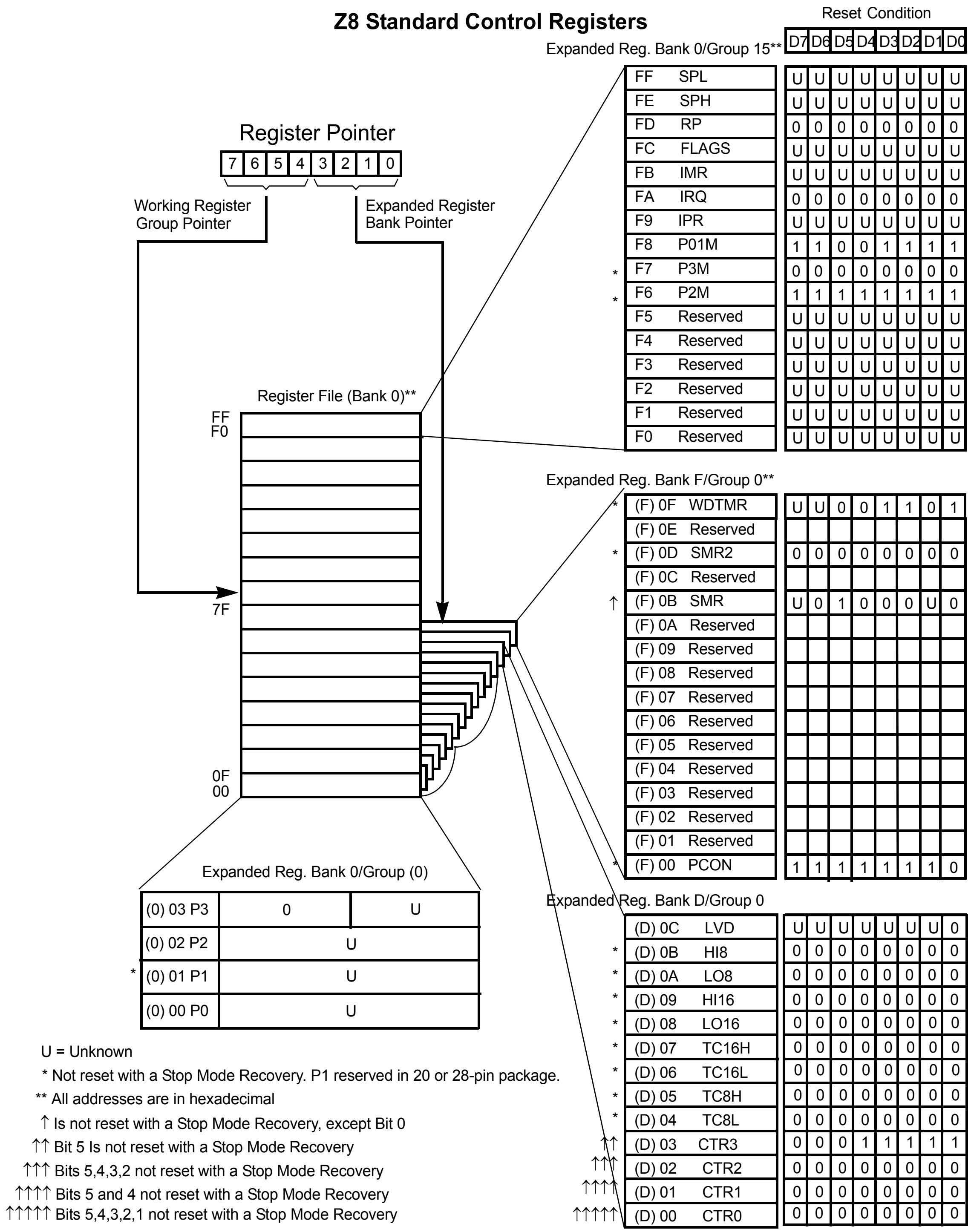


Figure 13. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 14) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Crimzon ZLP32300 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from `1h` to `Fh` exchanges the lower 16 registers to an expanded register bank.

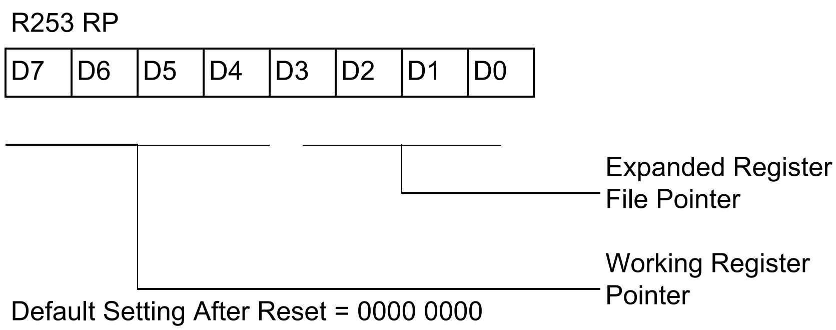


Figure 14. Register Pointer

Example: Crimzon ZLP32300 (see Figure 13 on page 22)

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTR0
R1 = CTR1
R2 = CTR2
R3 = CTR3

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      R0,#xx                  ; load CTR0
LD                      1, #xx                  ; load CTR1
```

T8_Capture_LO—L08(D)0Ah

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data—No Effect

T16_Capture_HI—HI16(D)09h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data—No Effect

T16_Capture_LO—L016(D)08h

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data—No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07h

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06h

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

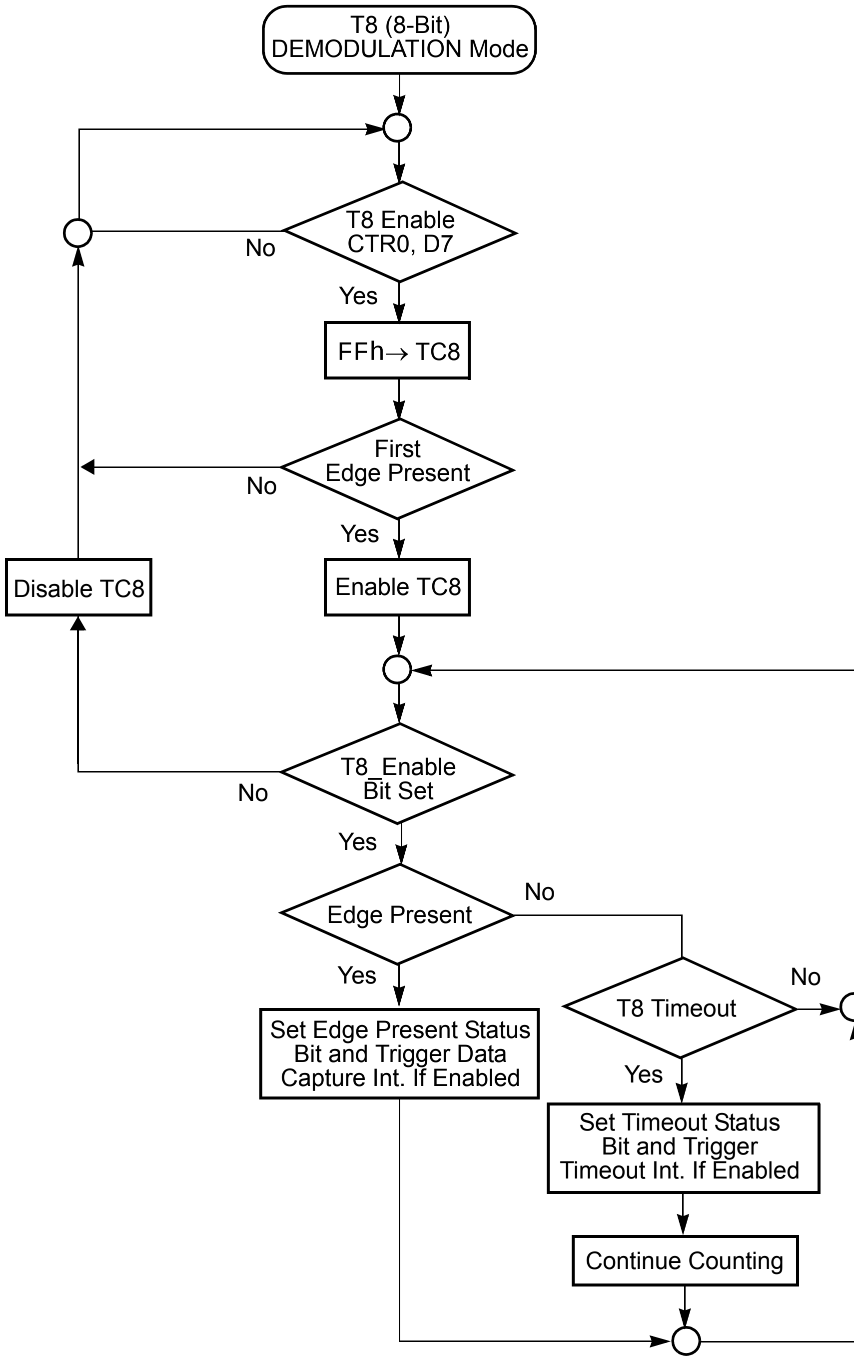


Figure 22. DEMODULATION Mode Flowchart

T16 TRANSMIT Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set, see Figure 23.

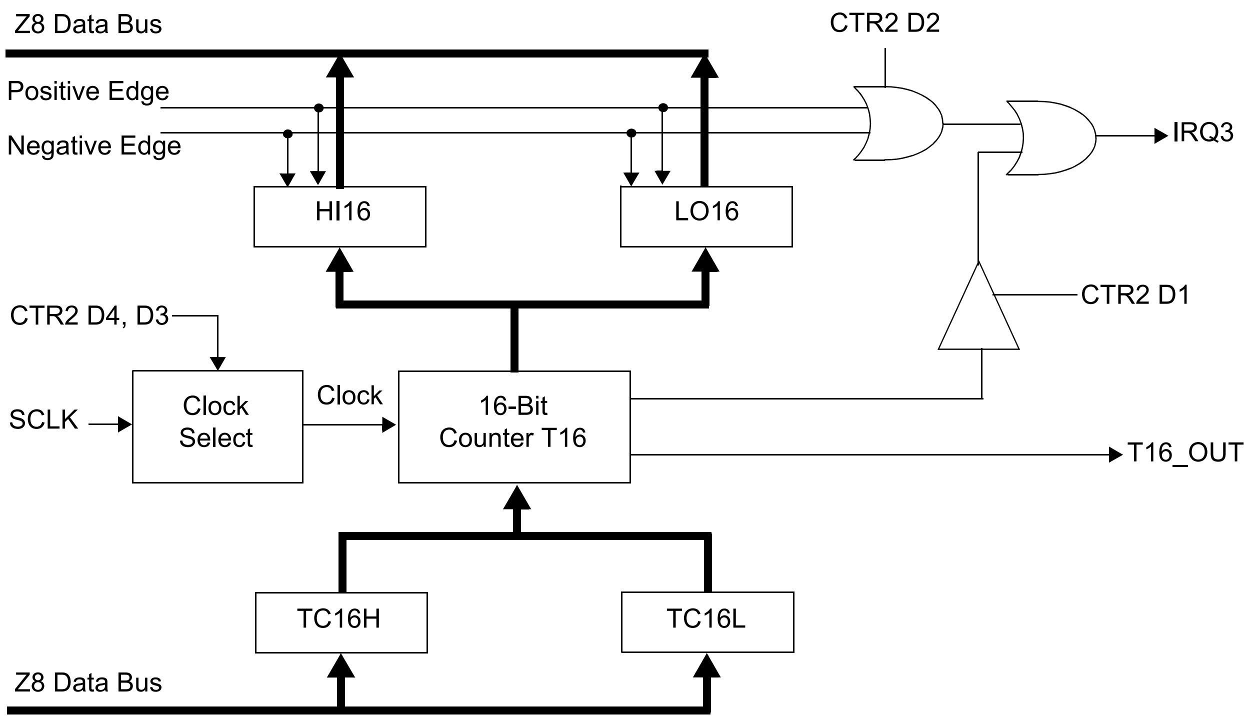


Figure 23. 16-Bit Counter/Timer Circuits

Note: *Global interrupts override this function as described in* Interrupts on page 43.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 24). If it is in MODULO-N mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 25).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

counter/timers (see Table 11 on page 45) and one for low-voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in DIGITAL mode, Pin P33 is the source. When in ANALOG mode, the output of the Stop Mode Recovery source logic is used as the source for the interrupt, see Figure 33 on page 52.

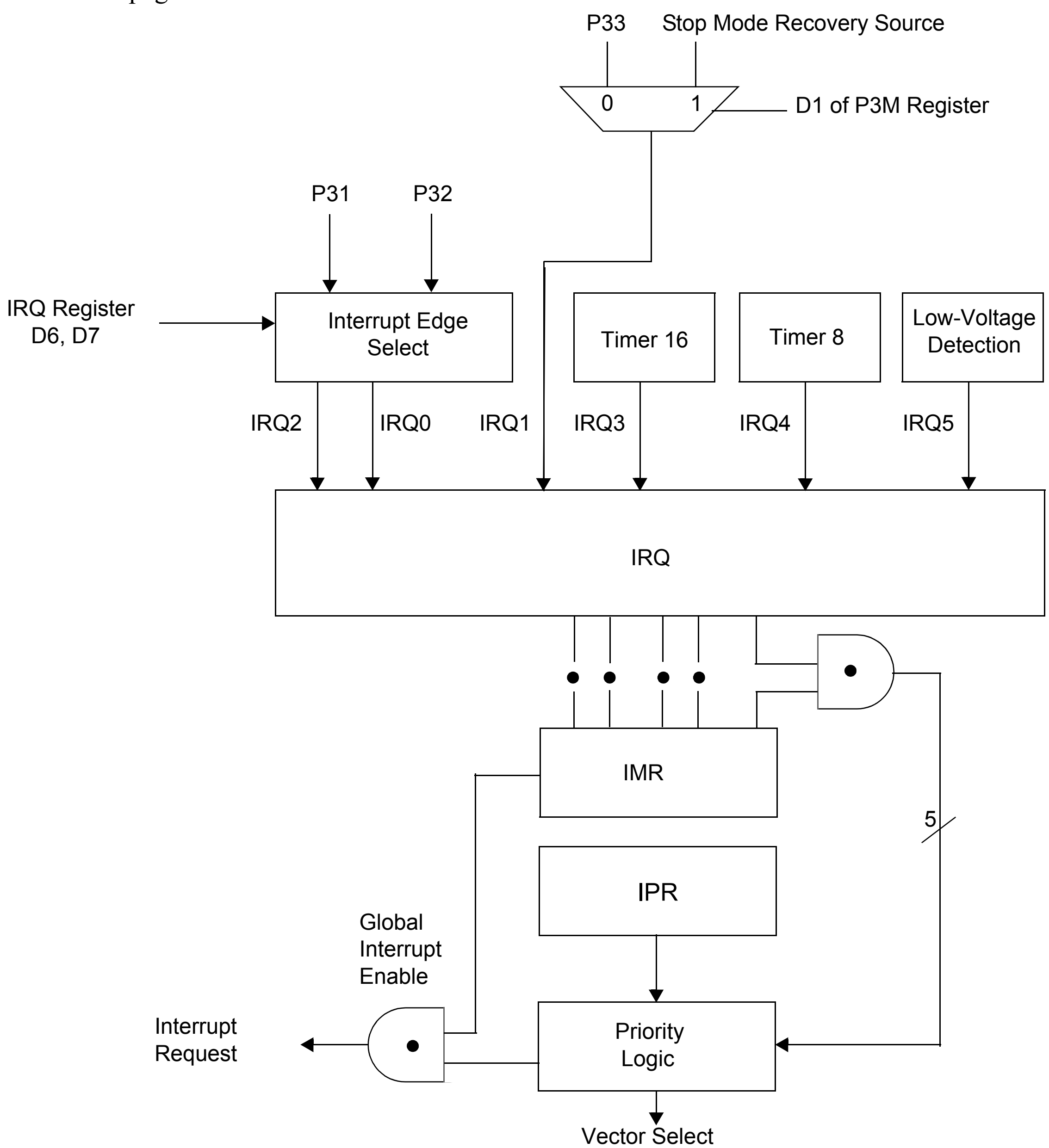


Figure 28. Interrupt Block Diagram

For both resonator and crystal oscillator, the oscillation ground must go directly to the ground pin of the microcontroller. The oscillation ground must use the shortest distance from the microcontroller ground pin and it must be isolated from other connections.

Power Management

Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns OFF the internal clock and external crystal oscillation, reducing the standby current to 10 µA or less. STOP mode is terminated only by a reset, such as WDT time-out, POR or SMR. This condition causes the processor to restart the application program at address `000Ch`. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = `FFh`) immediately before the appropriate sleep instruction, as follows:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter Stop Mode
```

or

```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (see Figure 32). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

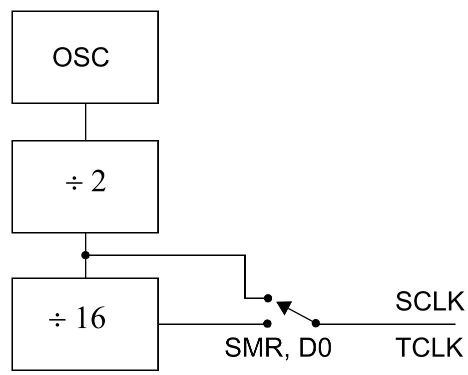


Figure 32. SCLK Circuit

Stop Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (see Figure 33 and Table 14).

Stop Mode Recovery Register 2—SMR2(F)0Dh

Table 13 lists and briefly describes the fields for this register.

Table 13. SMR2(F)0Dh:Stop Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0[†] 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)

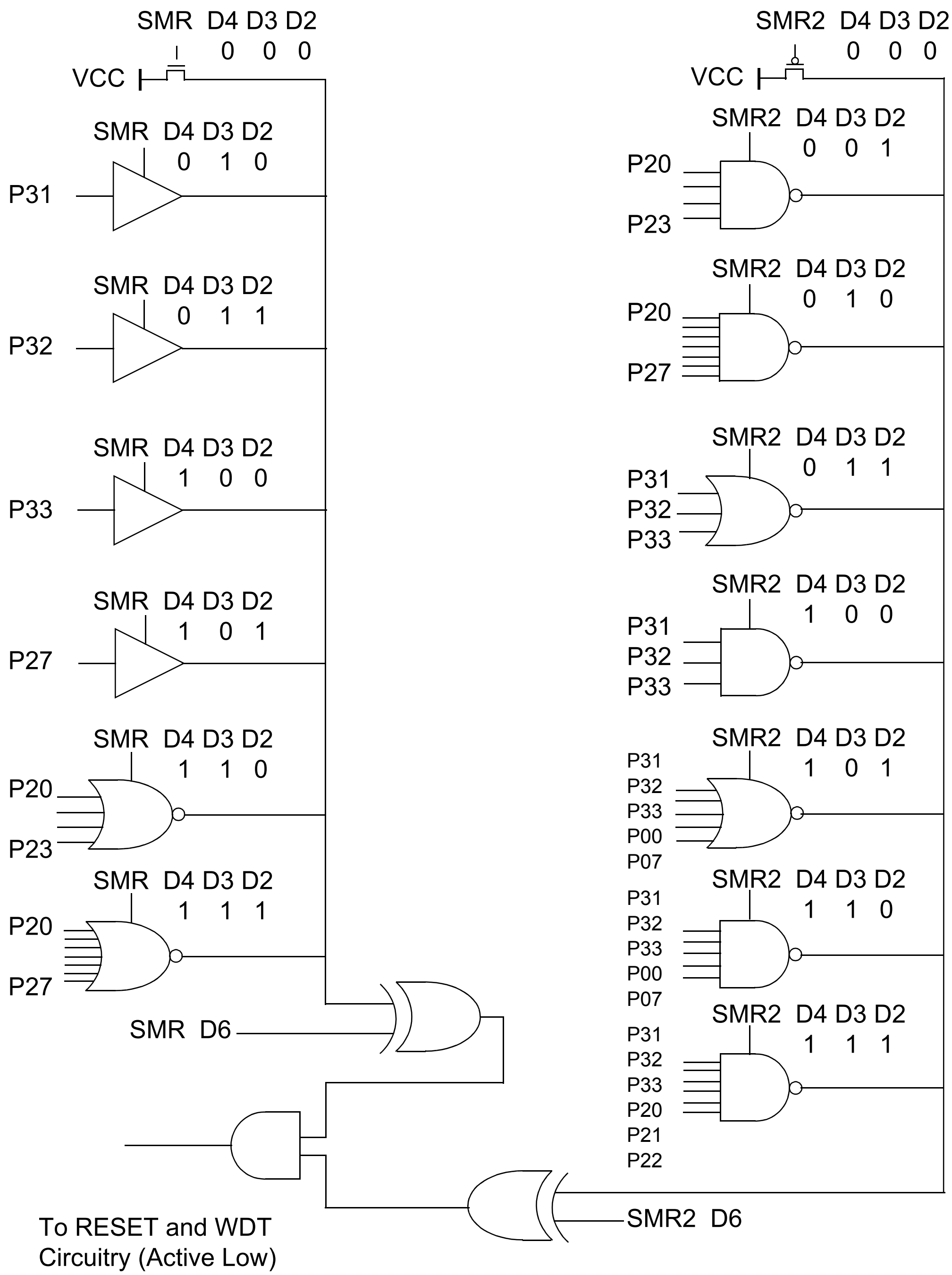


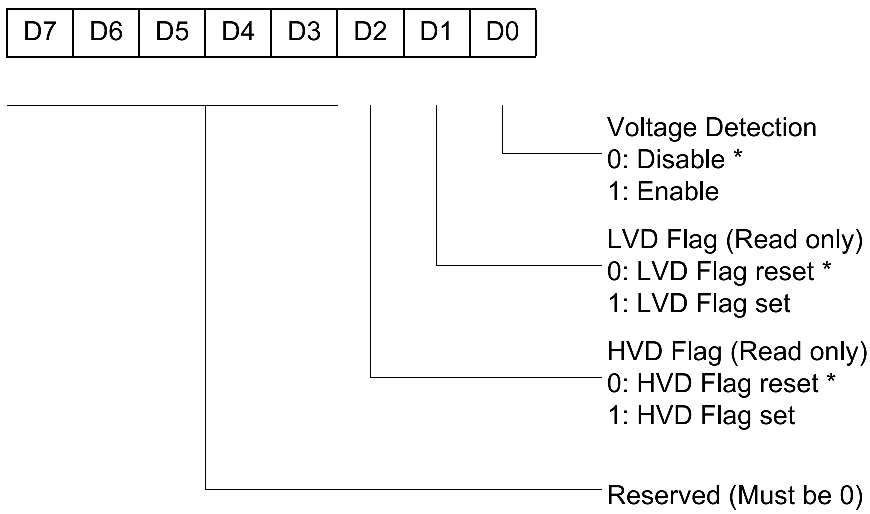
Figure 33. Stop Mode Recovery Source

Voltage Detection and Flags

The Voltage Detection register (LVD, register `0Ch` at the expanded register bank `0Dh`) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the V_{CC} level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD Flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

Note: *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

LVD(0D)0CH



*Default setting after reset.

Figure 41. Voltage Detection Register

Note: *Do not modify register P01M while checking a low-voltage condition. Switching noise of both Ports 0 and 1 together might trigger the LVD Flag.*

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are displayed in Figure 42 through Figure 55 on page 74.

PCON(0F)00H

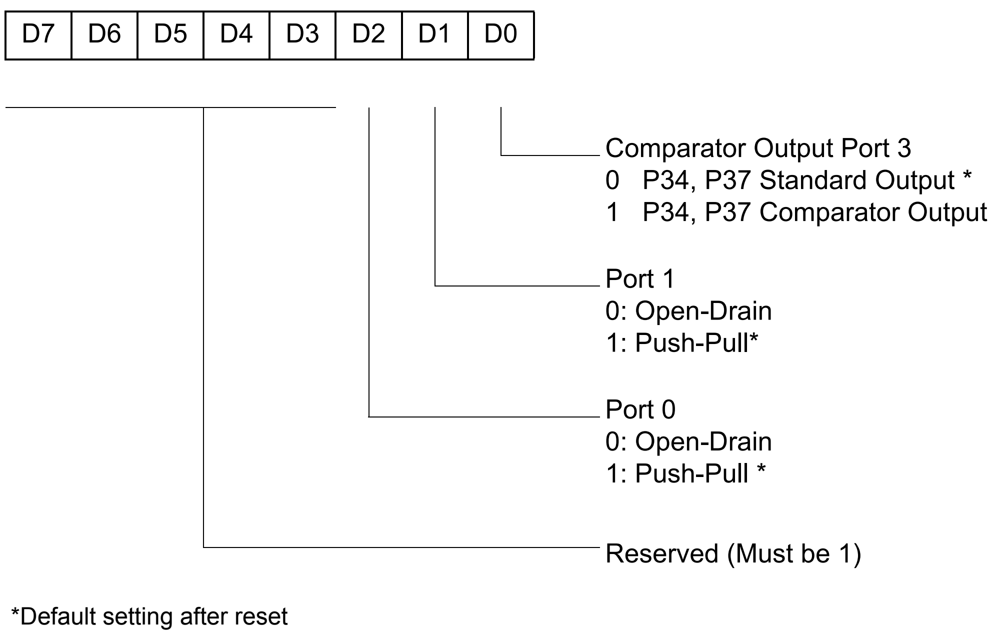


Figure 42. Port Configuration Register (PCON)(0F)00H: Write Only)

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0

WDT TAP INT RC OSC
00 5 ms min.
01* 10 ms min.
10 20 ms min.
11 80 ms min.

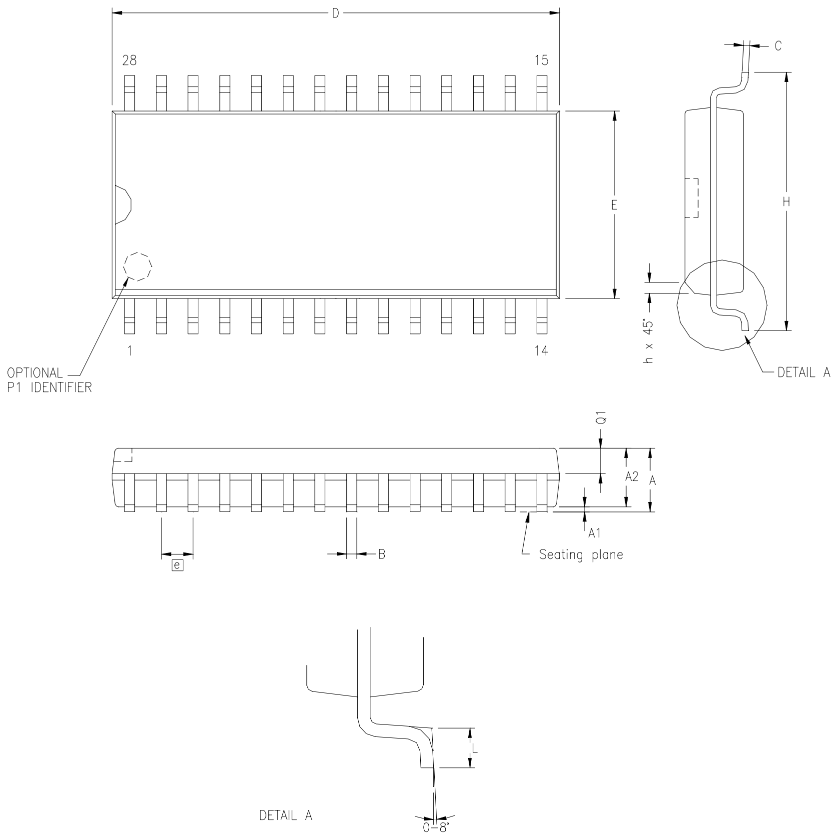
WDT During HALT
0 OFF
1 ON *

WDT During Stop
0 OFF
1 ON *

Reserved (Must be 0)

*Default setting after reset. Not Reset with a Stop Mode Recovery.

Figure 45. Watchdog Timer Register ((0F) 0FH: Write Only)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 28-Pin SOIC Package Diagram

Ordering Information

The Crimzon ZLP32300 is available for the following parts:

Device	Part Number	Description
Crimzon ZLP32300	ZLP32300H4832G	48-pin SSOP 32 K OTP
	ZLP32300P4032G	40-pin PDIP 32 K OTP
	ZLP32300H2832G	28-pin SSOP 32 K OTP
	ZLP32300P2832G	28-pin PDIP 32 K OTP
	ZLP32300S2832G	28-pin SOIC 32 K OTP
	ZLP32300H2032G	20-pin SSOP 32 K OTP
	ZLP32300P2032G	20-pin PDIP 32 K OTP
	ZLP32300S2032G	20-pin SOIC 32 K OTP
	ZLP32300H4816G	48-pin SSOP 16 K OTP
	ZLP32300P4016G	40-pin PDIP 16 K OTP
	ZLP32300H2816G	28-pin SSOP 16 K OTP
	ZLP32300P2816G	28-pin PDIP 16 K OTP
	ZLP32300S2816G	28-pin SOIC 16 K OTP
	ZLP32300H2016G	20-pin SSOP 16 K OTP
	ZLP32300P2016G	20-pin PDIP 16 K OTP
	ZLP32300S2016G	20-pin SOIC 16 K OTP
	ZLP32300H4808G	48-pin SSOP 8 K OTP
	ZLP32300P4008G	40-pin PDIP 8 K OTP
	ZLP32300H2808G	28-pin SSOP 8 K OTP
	ZLP32300P2808G	28-pin PDIP 8 K OTP
	ZLP32300S2808G	28-pin SOIC 8 K OTP
	ZLP32300H2008G	20-pin SSOP 8 K OTP