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## What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "[Embedded - Microcontrollers](#)"

### Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2832c">https://www.e-xfl.com/product-detail/analog-devices/zlp32300h2832c</a>

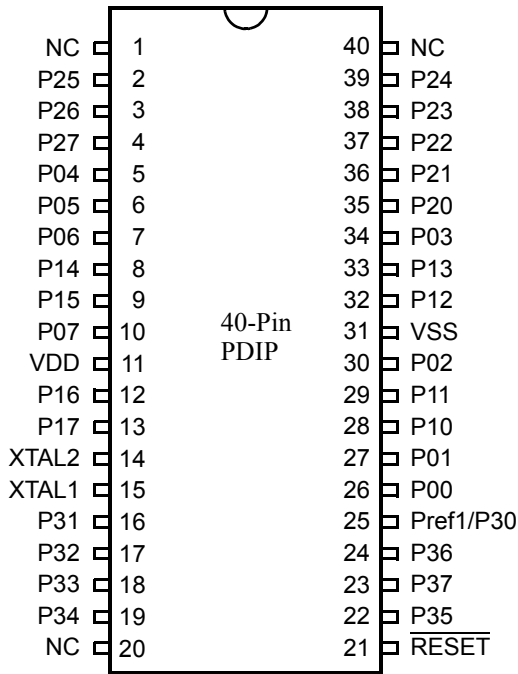


Figure 5. 40-Pin PDIP Pin Configuration

*open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.*

```
AND P0, #%F0
```

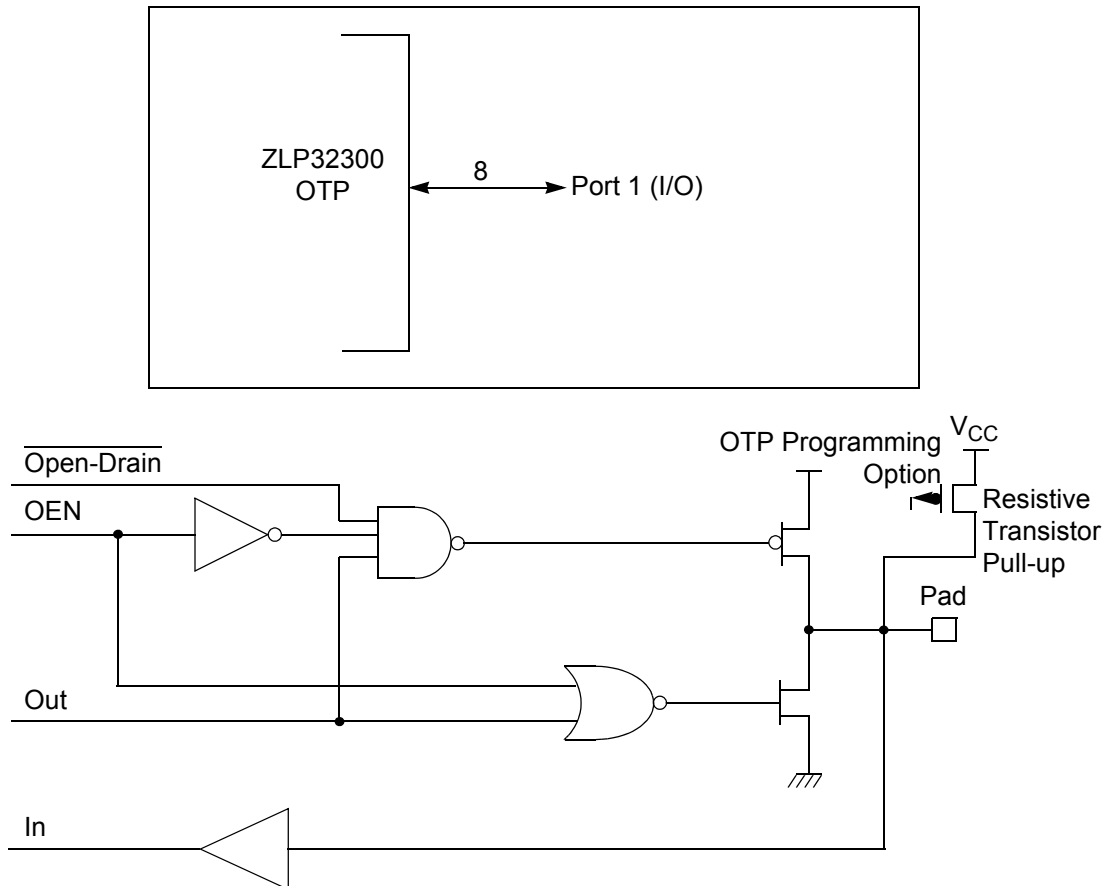
### Port 0 (P00–P07)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 01 mode register (P01M). After a hardware reset or Stop Mode Recovery, Port 0 is configured as an input port.

An optional pull-up transistor is available as a OTP option bit on all Port 0 bits with nibble select.

► **Note:** *The Port 0 direction is reset to be input following an SMR.*

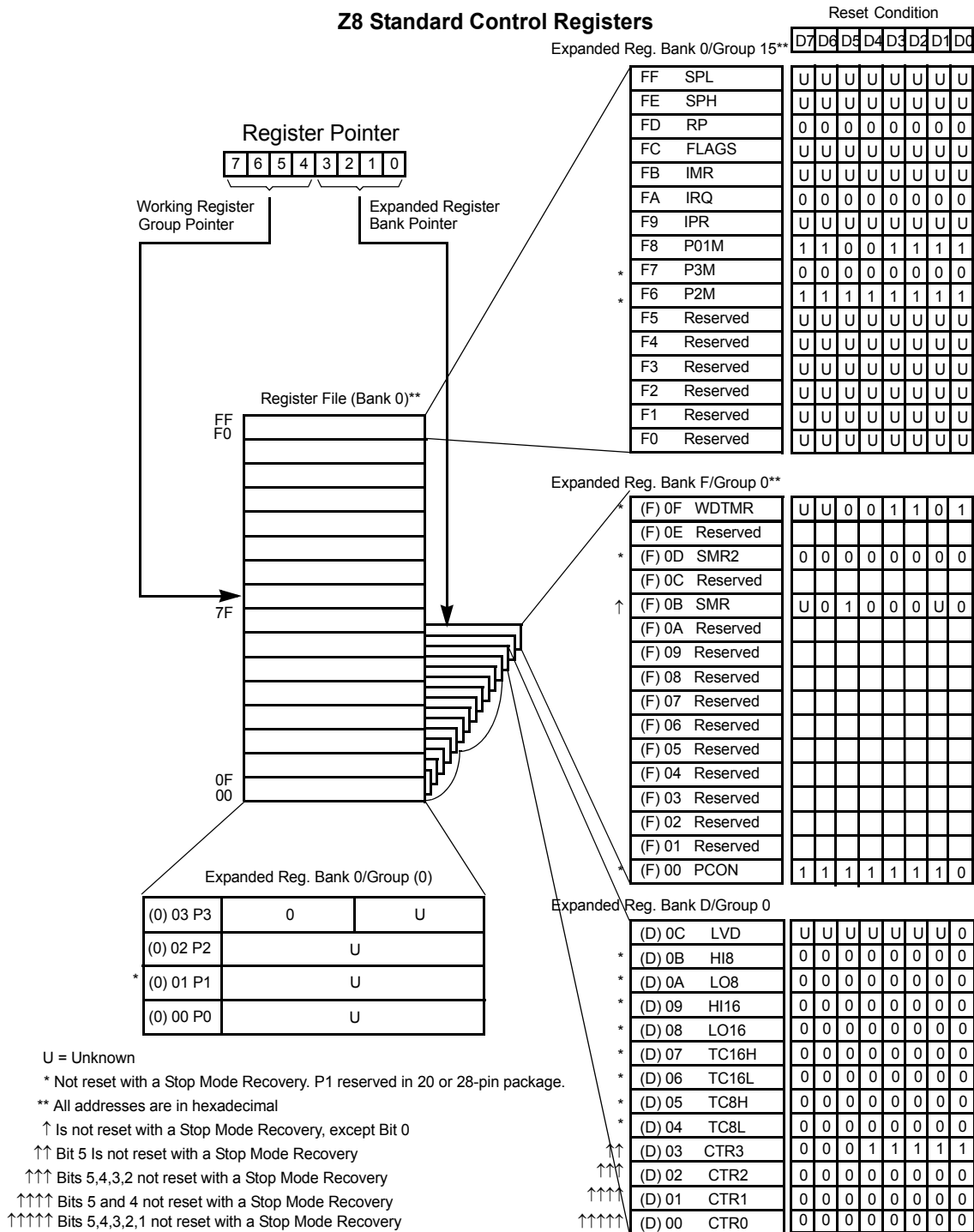


**Figure 8. Port 1 Configuration**

### Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see [Figure 9](#)). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode.



**Figure 13. Expanded Register File Architecture**

**P35\_Out**

This bit defines whether P35 is used as a normal output pin or T16 output.

**CTR3 T8/T16 Control Register—CTR3(D)03h**

Table 10 lists and briefly describes the fields for this register. This register allows the T<sub>8</sub> and T<sub>16</sub> counters to be synchronized.

**Table 10. CTR3 (D)03h: T8/T16 Control Register**

Field	Bit Position		Value	Description
T <sub>16</sub> Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T <sub>8</sub> Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode Recovery.

**Counter/Timer Functional Blocks****Input Circuit**

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 16).

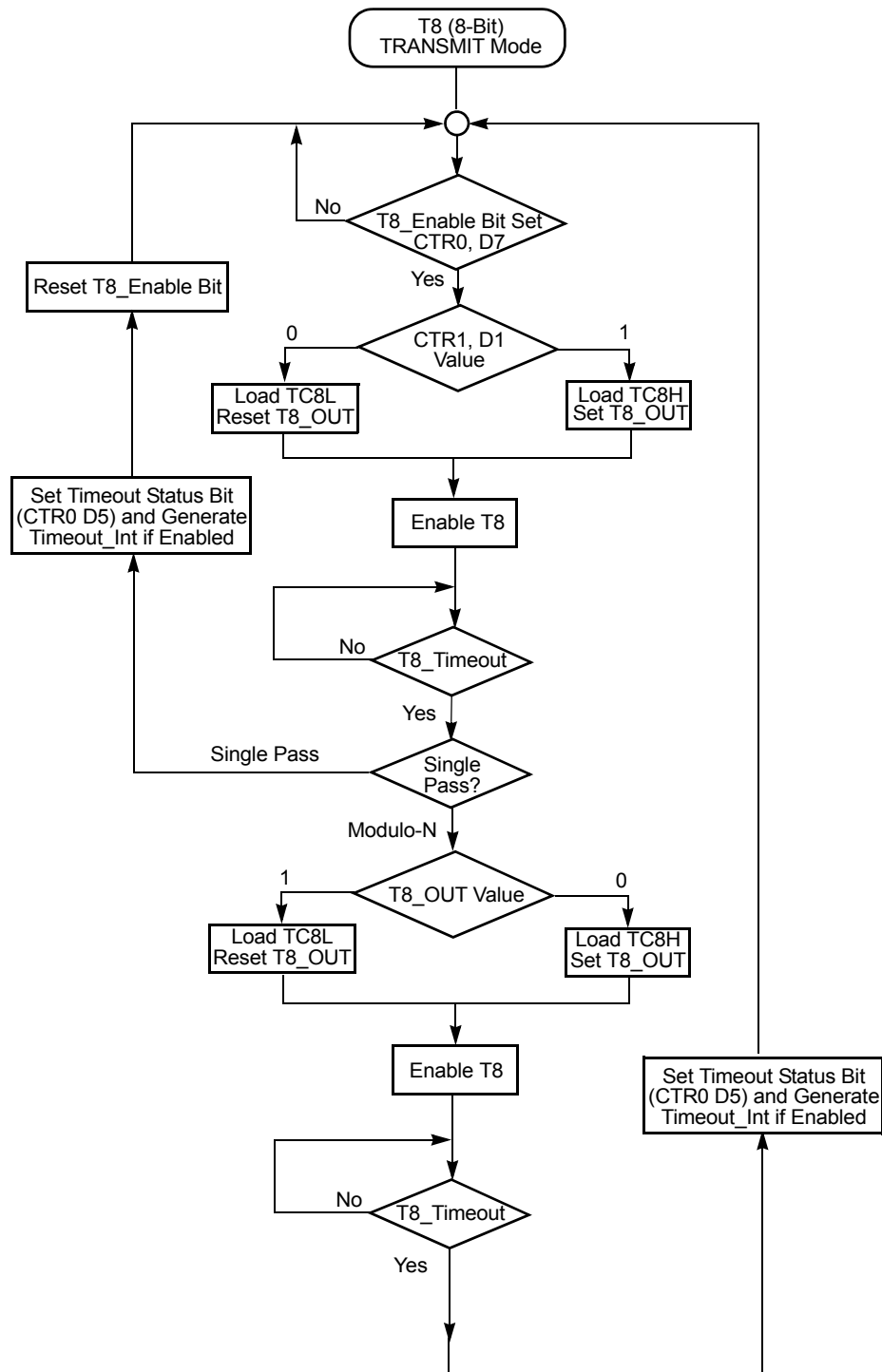
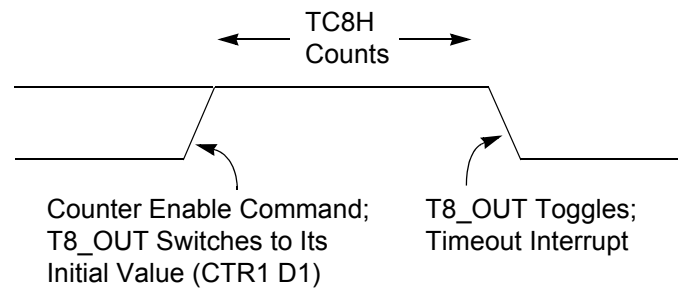


Figure 17. TRANSMIT Mode Flowchart

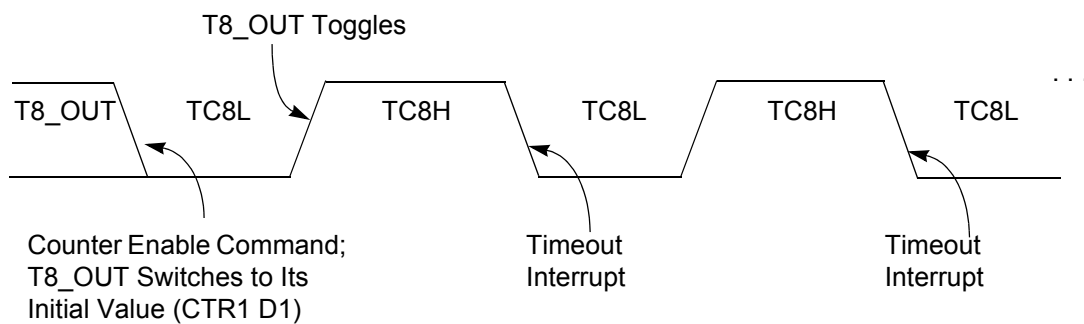


**Caution:** *Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.*

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur, see [Figure 19](#) and [Figure 20](#).



**Figure 19. T8\_OUT in SINGLE-PASS Mode**



**Figure 20. T8\_OUT in MODULO-N Mode**

### T8 DEMODULATION Mode

You must program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) is set, and an



This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

#### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

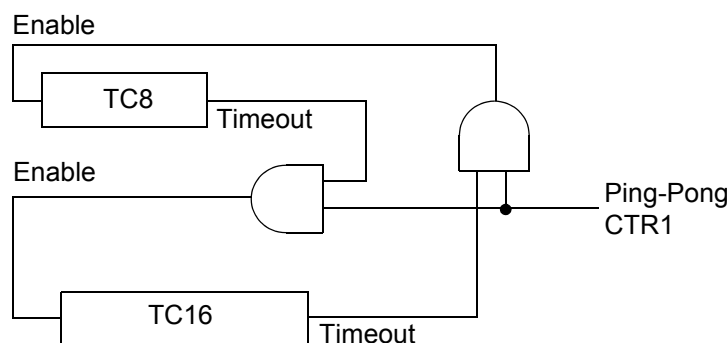
This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from  $FFFFh$ . Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

#### PING-PONG Mode

This operation mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE-PASS mode (CTR0, D6; CTR2, D6), and PING-PONG mode must be programmed in CTR1, D3; D2. You can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1, see [Figure 26](#).

► **Note:** *Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status Flags before instituting this operation.*



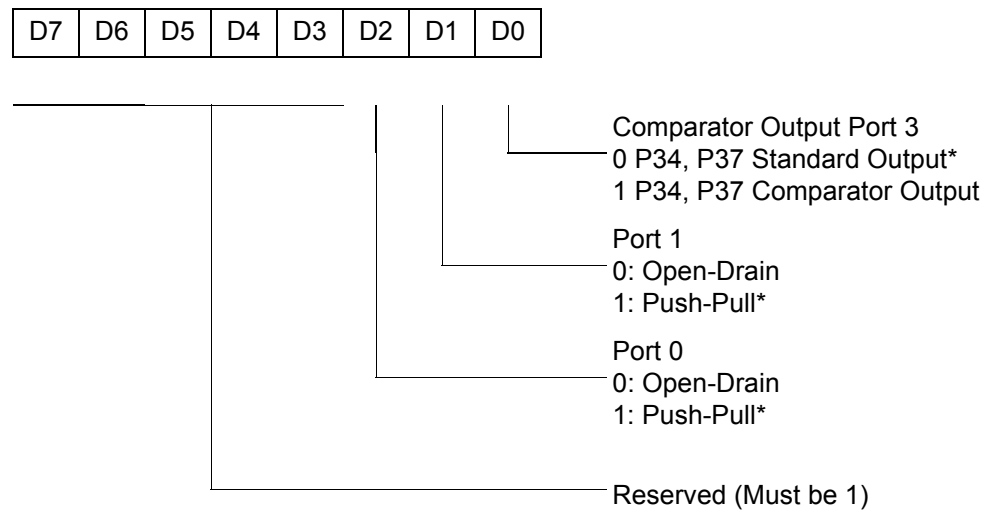
**Figure 26. PING-PONG Mode Diagram**

## Port Configuration

### Port Configuration Register

The Port Configuration (PCON) register (see [Figure 30](#)) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00h



\* Default setting after reset

**Figure 30. Port Configuration Register (PCON) (Write Only)**

### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

### Port 1 Output Mode (D1)

Bit 1 controls the output mode of Port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

**WDT Time Select (D0, D1)**

This bit selects the WDT time period. It is configured as indicated in [Table 15](#).

**Table 15. Watchdog Timer Time Select**

D1	D0	Timeout of Internal RC-Oscillator
0	0	5 ms min
0	1	10 ms min
1	0	20 ms min
1	1	80 ms min

**WDTMR During Halt (D2)**

This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1, see [Figure 36](#).

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0Ch at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The HVD Flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD Flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD Flag also triggers IRQ5. The IRQ bit 5 latches the low-voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a Flag only.

- **Note:** *If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt (EI) instruction prior to enabling the voltage detection.*

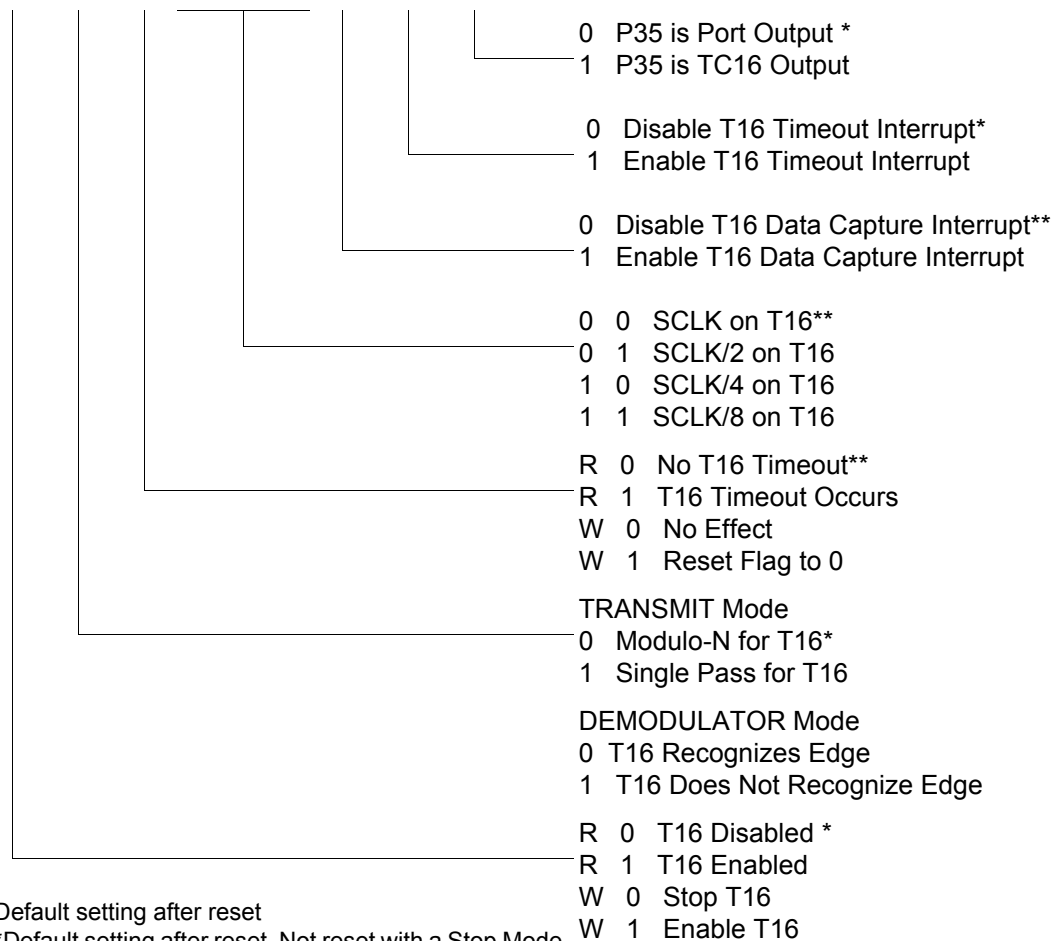


**Notes:**

1. *Ensure to differentiate the TRANSMIT mode from DEMODULATION mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.*
2. *Changing from one mode to another cannot be performed without disabling the counter/timers.*

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



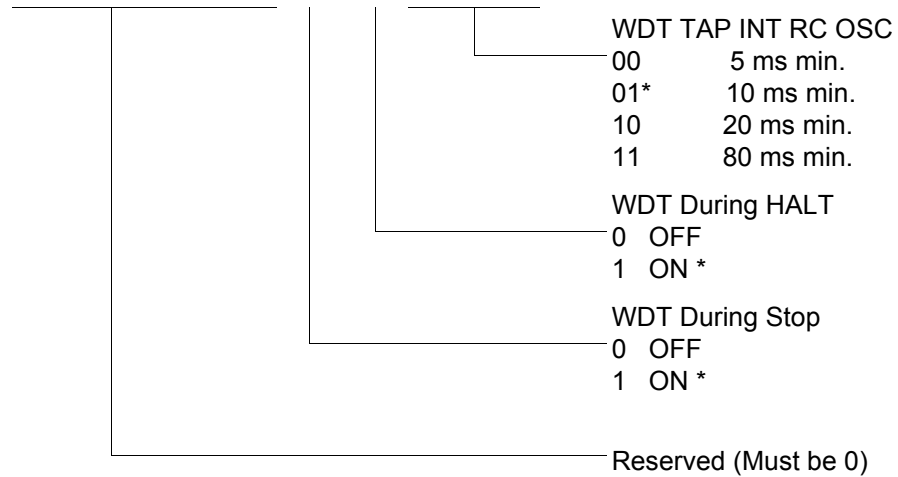
\*Default setting after reset

\*\*Default setting after reset. Not reset with a Stop Mode Recovery.

**Figure 39. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\*Default setting after reset. Not Reset with a Stop Mode Recovery.

**Figure 45. Watchdog Timer Register ((0F) 0FH: Write Only)**

## Standard Control Registers

The standard control registers are displayed in [Figure 46](#) through [Figure 55](#) on page 74.

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



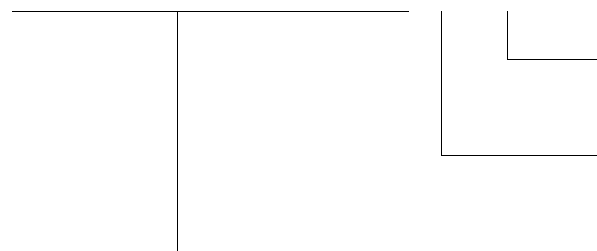
P27–P20 I/O Definition  
0 Defines bit as OUTPUT  
1 Defines bit as INPUT \*

\*Default setting after reset. Not Reset with a Stop Mode Recovery.

**Figure 46. Port 2 Mode Register (F6H: Write Only)**

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



0: Port 2 Open Drain \*  
1: Port 2 Push-Pull  
  
0= P31, P32 DIGITAL Mode\*  
1= P31, P32 ANALOG Mode

Reserved (Must be 0)

\*Default setting after reset. Not Reset with a Stop Mode Recovery.

**Figure 47. Port 3 Mode Register (F7H: Write Only)**

R249 IPR(F9H)

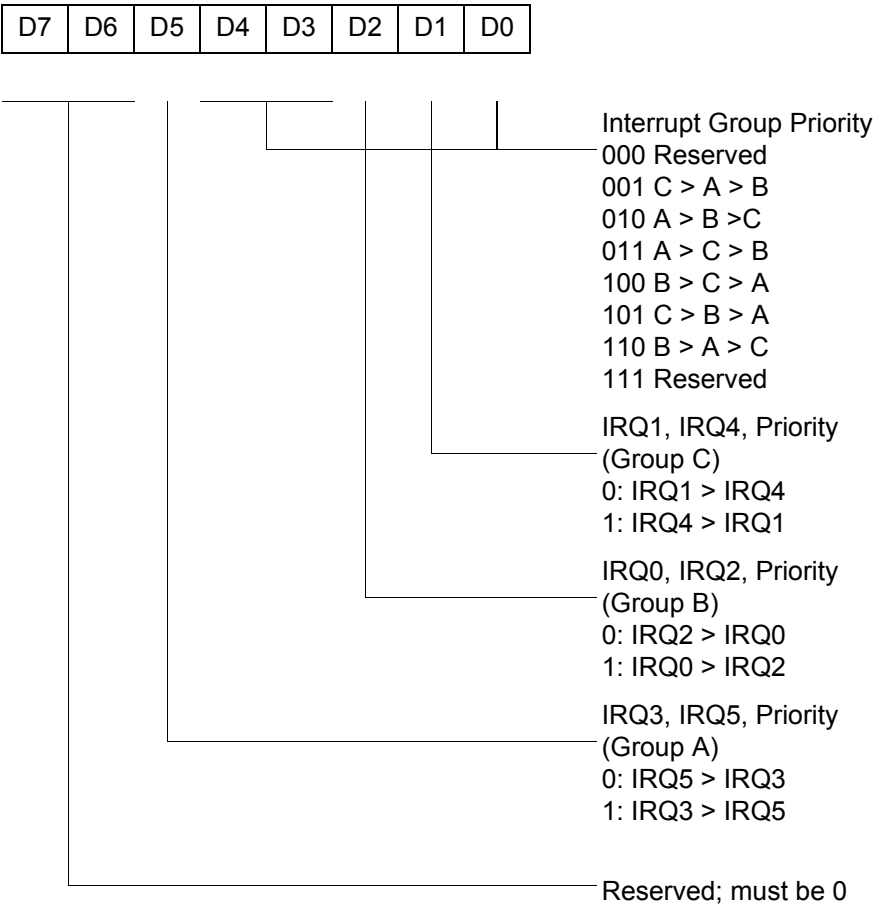
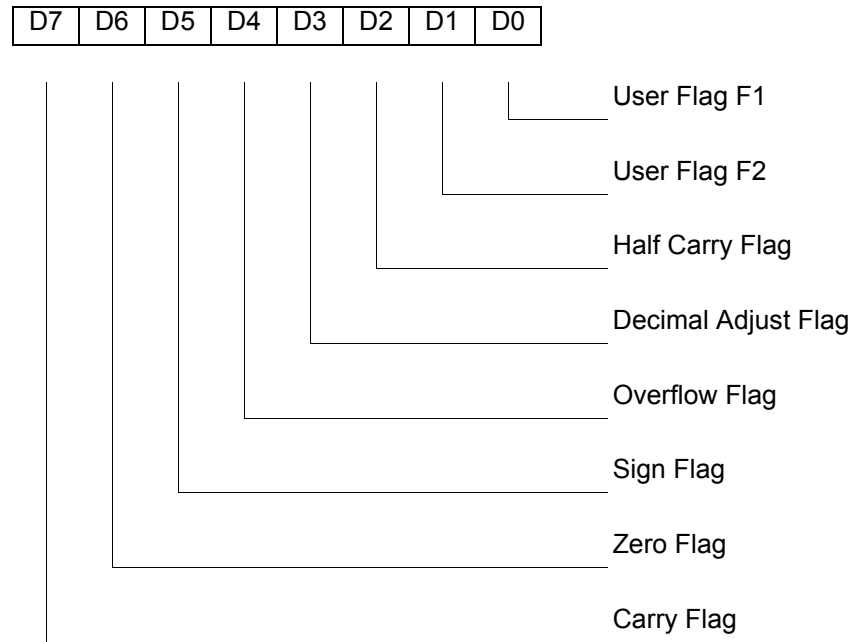


Figure 49. Interrupt Priority Register (F9H: Write Only)

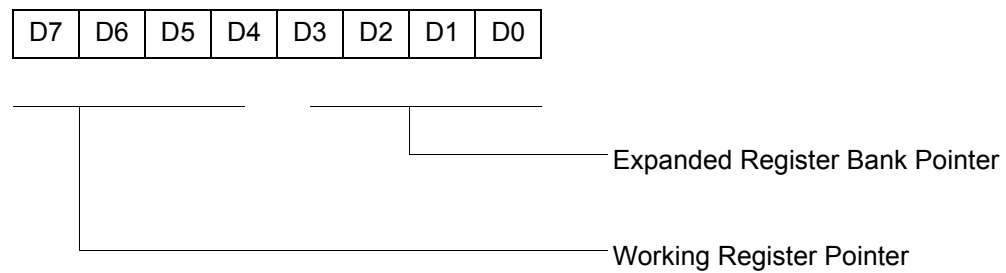


#### R252 Flags(FCH)



**Figure 52. Flag Register (FCH: Read/Write)**

#### R253 RP(FDH)



Default setting after reset = 0000 0000

**Figure 53. Register Pointer (FDH: Read/Write)**

R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

General-Purpose Register

**Figure 54. Stack Pointer High (FEH: Read/Write)**

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low  
Byte (SP7–SP0)

**Figure 55. Stack Pointer Low (FFH: Read/Write)**

## Capacitance

Table 18 lists the capacitances.

**Table 18. Capacitance**

Parameter	Maximum
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF
$T_A = 25\text{ }^{\circ}\text{C}$ , $V_{CC} = \text{GND} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND	

## DC Characteristics

Table 19 describes the DC characteristics.

**Table 19. DC Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$			Units	Conditions	Notes
			Min	Typ <sup>(7)</sup>	Max			
$V_{CC}$	Supply Voltage		2.0		3.6	V	See Notes	5
$V_{CH}$	Clock Input High Voltage	2.0-3.6	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
$V_{CL}$	Clock Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		0.4	V	Driven by External Clock Generator	
$V_{IH}$	Input High Voltage	2.0-3.6	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
$V_{IL}$	Input Low Voltage	2.0-3.6	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
$V_{OH1}$	Output High Voltage	2.0-3.6	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{ mA}$	
$V_{OH2}$	Output High Voltage (P36, P37, P00, P01)	2.0-3.6	$V_{CC}-0.8$			V	$I_{OH} = -7\text{ mA}$	
$V_{OL1}$	Output Low Voltage	2.0-3.6			0.4	V	$I_{OL} = 4.0\text{ mA}$	
$V_{OL2}$	Output Low Voltage (P00, P01, P36, P37)	2.0-3.6			0.8	V	$I_{OL} = 10\text{ mA}$	
$V_{OFFSET}$	Comparator Input Offset Voltage	2.0-3.6			25	mV		
$V_{REF}$	Comparator Reference Voltage	2.0-3.6	0		$V_{CC}$ -1.75	V		

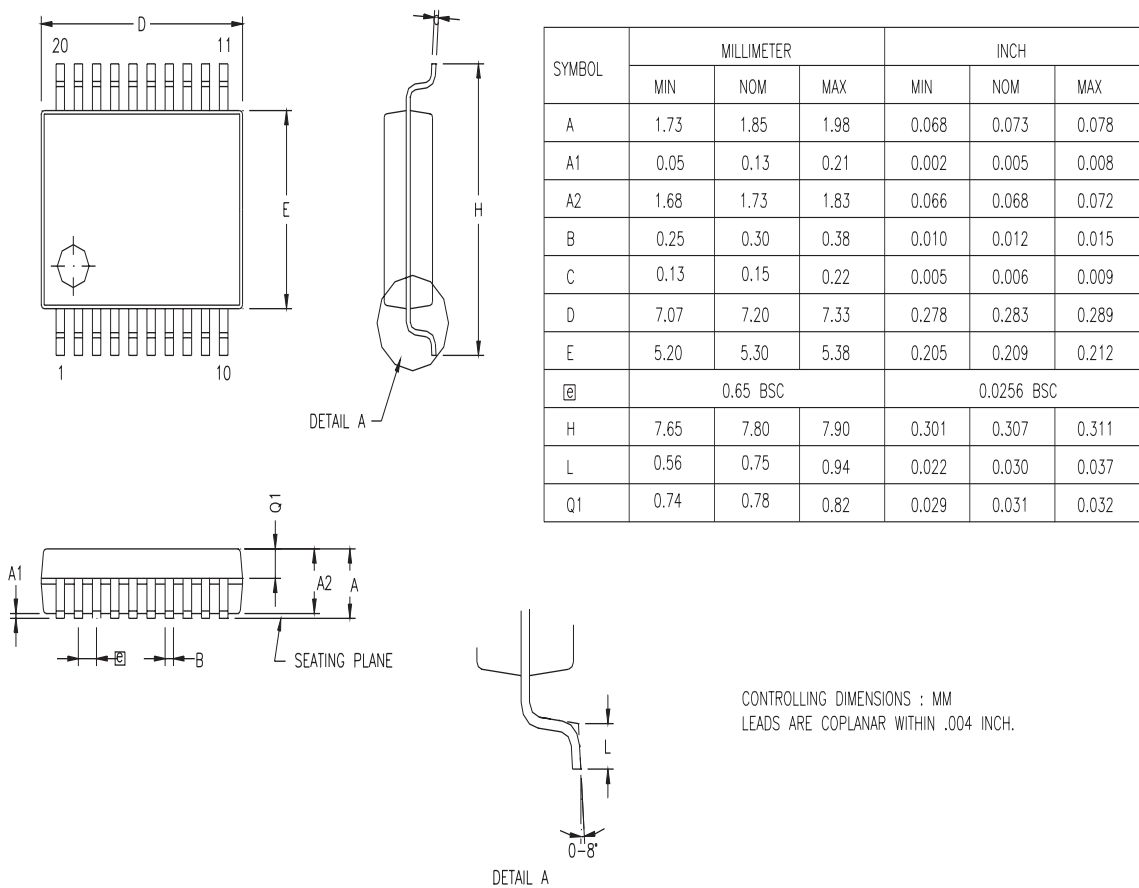


Figure 60. 20-Pin SSOP Package Diagram

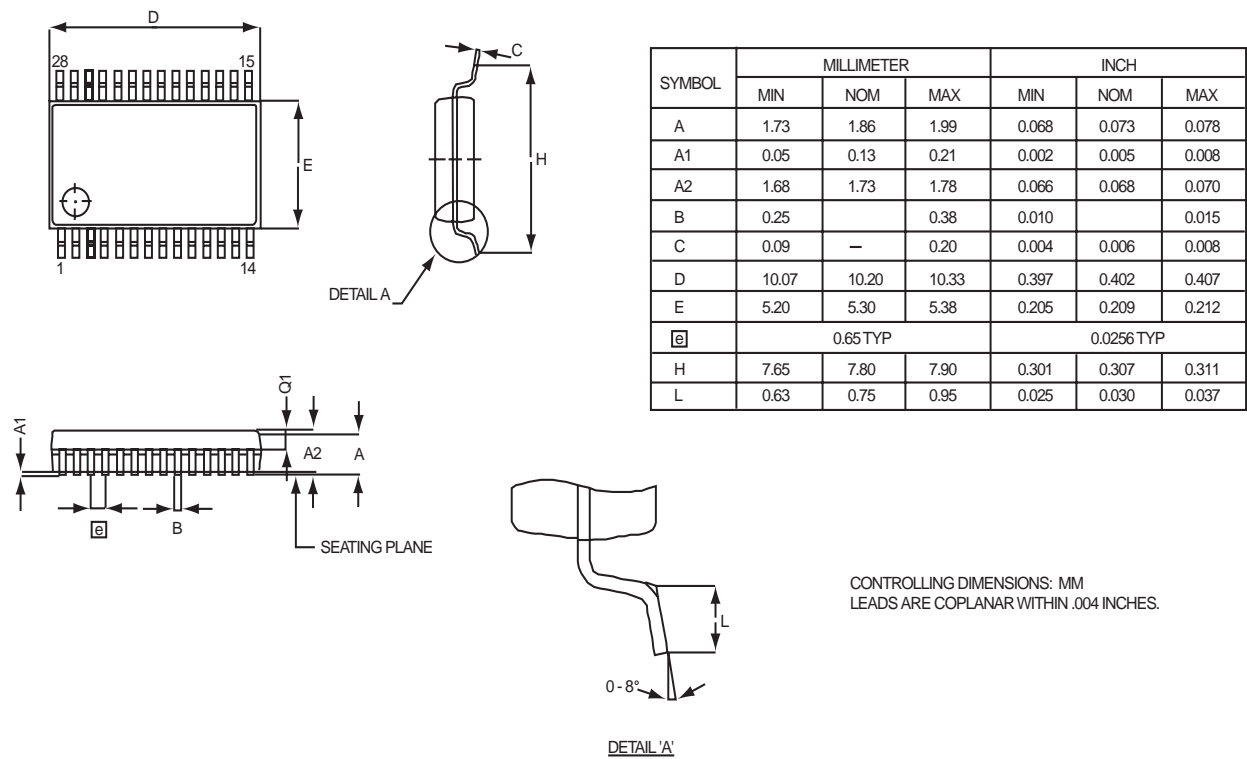


Figure 63. 28-Pin SSOP Package Diagram

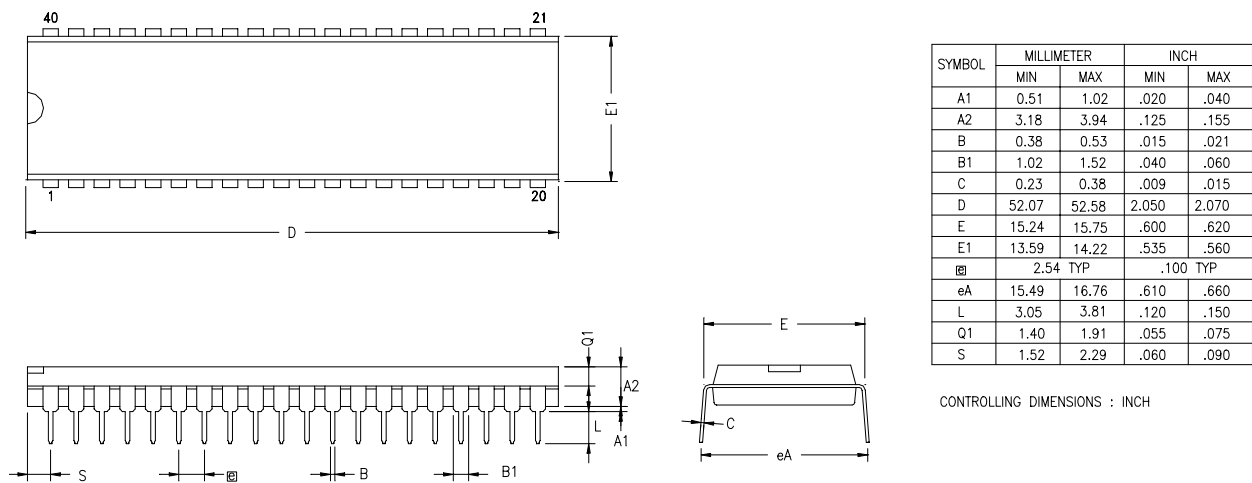


Figure 64. 40-Pin PDIP Package Diagram